A High Purity Integer-*N* Frequency Synthesizer in 0.35μm SiGe BiCMOS*

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Abstract: An integer-*N* frequency synthesizer in 0.35μm SiGe BiCMOS is presented. By implementing different building blocks with different types of devices, a high purity frequency synthesizer with excellent spur and phase noise performance has been realized. All the building blocks are implemented with differential topology except for the off-chip loop filter. To further reduce the phase noise, bonding wires are used to form the resonator in the LC-VCO. The frequency synthesizer operates from 2.39 to 2.72GHz with output power of about 0dBm. The measured closed-loop phase noise is −95dBc/Hz at 100kHz offset and −116dBc/Hz at 1MHz offset from the carrier. The power level of the reference spur is less than −72dBc. With a 3V power supply, the whole chip including the output buffers consumes 60mA.

Key words: SiGe BiCMOS; phase-locked loop; high purity; loop bandwidth
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1 Introduction

Phase-locked loop (PLL) frequency synthesizers for radio frequencies are one of the key components of wireless communication systems. There is a strong demand for high frequency and high purity PLLs for both novel wireless data transmission standards[1] and direct conversion mobile phone architectures[2]. The spectrum purity of a PLL frequency synthesizer is generally defined with two parameters, spur and phase noise. Spur suppression is inversely proportional to the PLL loop bandwidth[3]. For phase noise, the situation is much more complicated. With a certain loop bandwidth, phase noise is dominated by the divider and charge pump at frequency offset lower than loop bandwidth and by VCO at frequency offset higher than loop bandwidth. Design techniques for reducing the PLL phase noise have been studied extensively. While CMOS PLL generally needs deliberate loop design to compromise the noise contribution from each building block[3], PLL design in SiGe BiCMOS is much more flexible because of the different noise characteristics of bipolar transistors from CMOS. Bipolar devices with lower flicker noise corner frequency are more suitable to realize VCO than CMOS, especially in low bandwidth PLLs.

This paper presents a PLL in 0.35μm SiGe Bi CMOS and introduces the process. Detailed system and circuit designs for high purity operation are discussed.

2 Technology

The PLL was implemented in the commercially available Chartered 0.35μm 2P4M SiGe BiCMOS Process. The technology offers 3V and 5V n-p-n transistors with SIC implant, lateral and vertical p-n-p transistors, 65Ω/□ unsolicited poly SiGe and 1000Ω/□ high sheet Rho poly resistors, accumulation-mode nMOS and p-n junction varactor, MOS, MIM and poly/n^+ sinker capacitors, electrostatic discharge protection devices, and CMOS transistors with a minimum gate length of 0.35μm. The n-p-n transistors have a transit frequency of 75GHz. It also provides spiral inductors implemented using a low series resistance (4μm thick) top metal.

3 Circuit design

The block diagram of the presented PLL is shown in Fig. 1. It is of integer-*N* architecture and comprises a tri-state PFD, a current-steering charge pump, a cross-coupled LC-VCO, an output buffer, a 4/5 prescaler and a multi-modulus asynchronous divider. For applications where settling time is not a primary consideration, low loop bandwidth is generally advantageous since it can greatly suppress the reference spurs[3], which is the major impurity in integer-*N* PLL output spectra. Large capacitors, which are not practical in on-chip implementations, are thus needed.

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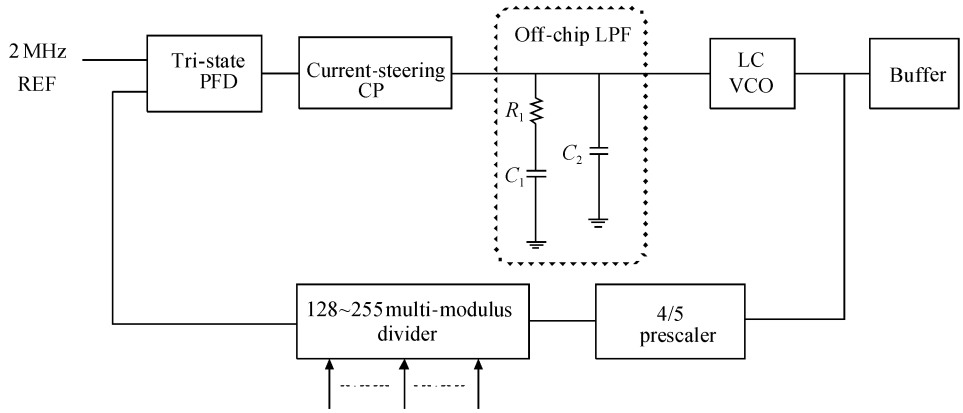

Fig. 1 Block diagram of the presented SiGe BiCMOS frequency synthesizer

In this PLL, the second-order loop filter is implemented with off-chip discrete components, providing more flexibility than an on-chip solution. Equation (1) is used to calculate the component values of the loop filter. The final parameters are listed in Table 1.

$$R_1 = \frac{Nw}{I_{cp}K_{VCO}} \times \frac{1}{2\tan\varphi(\sec\varphi - \tan\varphi)}$$
$$C_1 = \frac{I_{cp}K_{VCO}}{Nw^2} \times 2\tan\varphi$$
$$C_2 = \frac{I_{cp}K_{VCO}}{Nw^2}(\sec\varphi - \tan\varphi) \quad (1)$$

Phase noise is another important parameter to evaluate the output spectrum purity. All the building blocks contribute to the PLL output phase noise with different noise transfer functions. The VCO noise experiences a high-pass filter transfer function with a corner frequency near the PLL loop bandwidth. With CMOS VCO, low loop bandwidth leads to large close-in phase noise because of the high flicker noise corner frequency. In contrast, the BJT device has a much lower corner frequency of flicker noise, which makes it a proper candidate for implementing the VCO in low bandwidth PLL. Other components, which are essentially digital blocks, are more suitably implemented with CMOS devices for high integration density. The low-pass noise transfer function of these components makes their flicker noise less harmful in low bandwidth PLL. To enhance the common-mode noise immunity, differential topologies are used throughout the PLL loop, except for the off-chip loop filter.

Table 1 Summary of the PLL parameters

Loop bandwidth, w	30kHz
I_{cp}	200μA
K_{VCO}	30MHz/V
Phase margin, φ	60°
R_1	42.5kΩ
C_1	355pF
C_2	36pF

3.1 PFD and charge pump design

The charge pump used in this PLL is of the current-steering type, as shown in Fig. 2[4]. Cascoded current sources are used since their output resistance is much higher than that of their common-source counterpart. The topology of the current source, including the biasing circuit, is shown in Fig. 3. The biasing circuit employed also enables a large output voltage range, which is simulated to be 0.4V to 2.6V for a 3V supply.

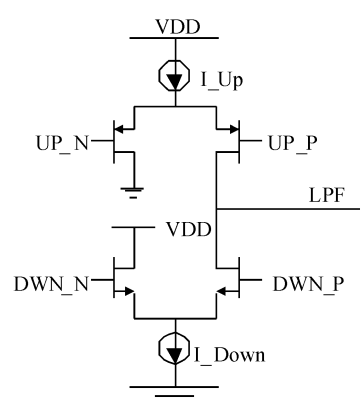

Fig. 2 Charge pump with current-steering switches

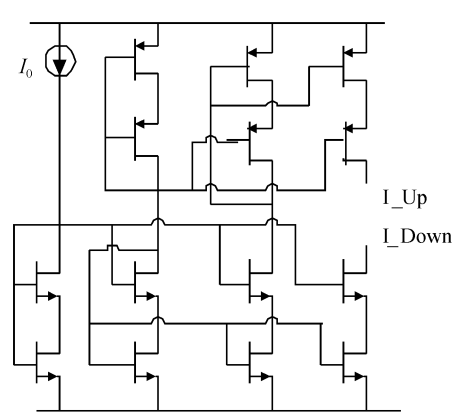

Fig. 3 Cascoded current source used in charge pump

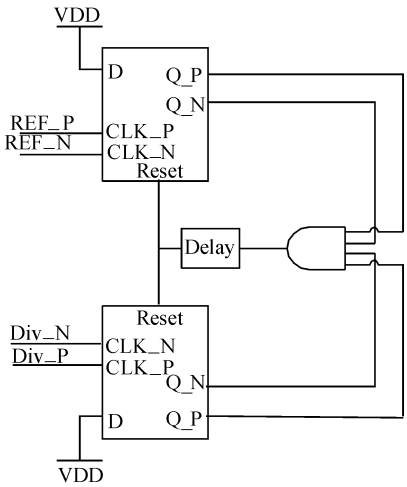

Fig. 4　Topology of differential PFD

To switch such a charge pump, differential control signals are needed. A NOT gate is generally used to produce the complementary signal[5]. This approach inevitably induces timing mismatch even when additional transmission gates are used. When the delay mismatch, Δt_{d}, is much smaller than the turn-on time of the PFD, Δt_{on}, the amount of the spur is approximately given by

$$P_{\mathrm{spur}} \cong 20\lg\left(\frac{f_{\mathrm{BW}}}{f_{\mathrm{ref}}} \times N \times \frac{(2\pi)^2}{\sqrt{2}} \times f_{\mathrm{ref}}^2 \Delta t_{\mathrm{d}} \Delta t_{\mathrm{on}}\right) - 20\lg\left(\frac{f_{\mathrm{ref}}}{f_{\mathrm{P1}}}\right)[\mathrm{dbc}] \quad (2)$$

where f_{BW} is the loop bandwidth, f_{ref} is the reference frequency, N is the division ratio, and f_{P1} is the first pole frequency of the loop filter, respectively[4]. For a turn-on time of 2ns and a desired spur of -70dBc, the delay mismatch is calculated to be less than 0.3ns. Effectiveness is enhanced by using the differential instead of the single-ended PFD, as shown in Fig. 4. With this kind of PFD, the complementary control signals at the charge pump input can be perfectly matched by a symmetrical layout. The phase noise and spurs are hence greatly reduced. Figure 5 shows the topologies of the NAND and OR gates, which are the basic building blocks of the PFD, implemented with differential cascaded voltage switching logic (DCVSL).

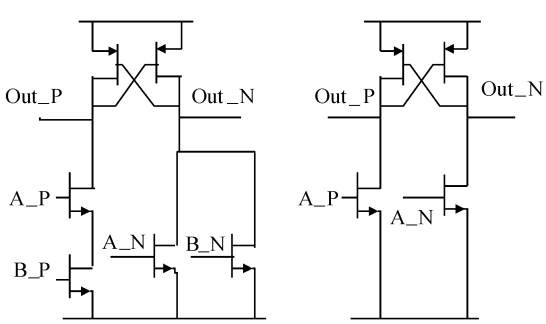

Fig. 5　DCVSL NAND and OR gates

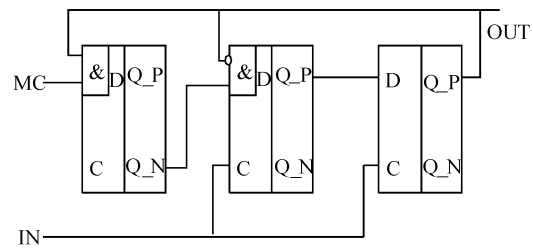

Fig. 6　Logic diagram of divided by 4/5 prescaler

3.2　Prescaler and multi-modules divider design

The prescaler is a crucial block in the PLL since it works at the highest frequency. We use master-slave D flip-flops and AND gates to form the divided by 4 or 5 prescaler. The logic diagram of the circuit is shown in Fig. 6. MC is the mode control signal. The prescaler is programmed to divide-by-4 when MC is low and divide-by-5 when MC is high. Current mode logic (CML)[6] is used in the D flip-flops for high speed and low noise operation. To save power consumption, the AND gate is incorporated into the CML D latch, as shown in Fig. 7.

The divider chain also includes 7 stages of $\div 2/3$ dividers, as shown in Fig. 8[7]. The total division ratio is given by $R = 2^7 + P_7 \times 2^6 + P_6 \times 2^5 + \cdots + P_1 \times 2 + P_0$ and can produce any integer division ratio ranging from 128 to 255. Since these dividers operate at the frequency much lower than that of the prescaler, they are less crucial and the design is quite straightforward.

The whole divider chain is implemented with differential signaling, which is necessary for correct PFD operation.

3.3　VCO design

A VCO with low phase noise is the most challenging block in the PLL frequency synthesizer[8]. Compared to a CMOS device in this process, BJT has much higher transit frequency, larger transconduc-

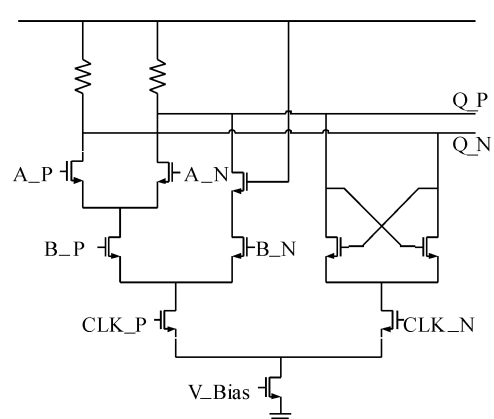

Fig. 7　D latch incorporated with AND gate

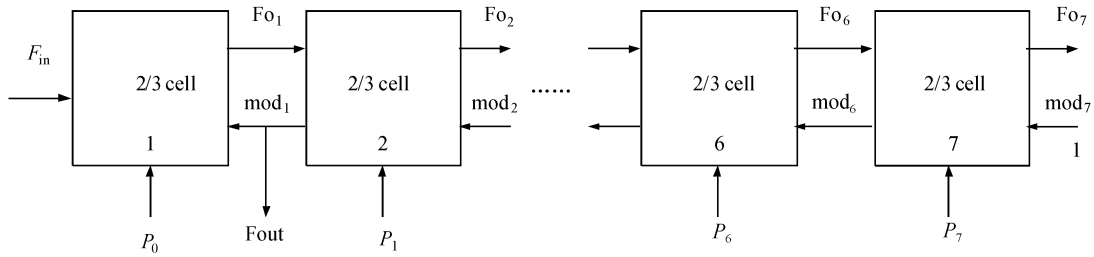

Fig. 8 Block diagram of the fully programmable multi-modulus frequency divider

tance, smaller parasitic originating from smaller transistor size, and more accurate simulated oscillation frequency. Most importantly, the BJT device has much lower flicker noise, which makes it suitable for low-bandwidth PLL applications. The VCO topology employed in this PLL is a cross-coupled pair based differential structure, as shown in Fig. 9. The schematic shows that capacitor banks are used to maintain a certain output frequency range without using large varactors, which are commonly considered as the main source of $1/f$ noise up-conversion[9].

Lesson originally postulated that thermally induced phase noise in any oscillator takes the form:

$$l(w_m) = \frac{4FkTR}{V_o^2}\left(\frac{w_0}{2Qw_m}\right)^2$$

where F is an unspecified noise factor. High-Q inductors are needed to improve the VCO phase noise performance. Compared to on-chip integrated inductors, bonding wires typically have quality factors at least an order of magnitude higher. Since low phase noise is the primary design goal of this VCO, bonding wires are used to resonate with on-chip accumulation-mode varators. This also leads to a compact layout and reduced power consumption. By careful operation and adjusting, the golden wires can be bonded to the pad with tolerable length variation. This variation does not change the synthesizer's output frequency for the feedback operation in the PLL.

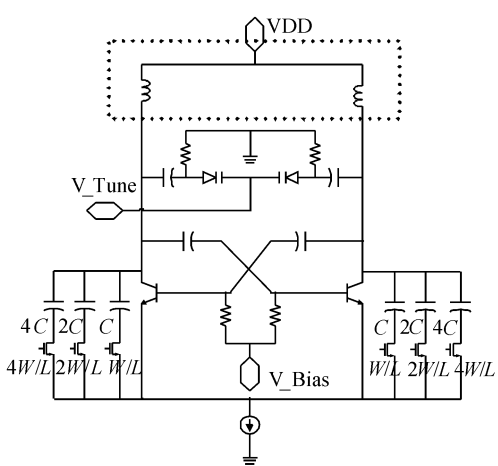

Fig. 9 VCO topology with off-chip bonding wires

4 Test results

An integer-N frequency synthesizer PLL has been fabricated in 0.35μm SiGe BiCMOS technology. The photograph of the fabricated chip is shown in Fig. 10, and its active area including PADs and ESDs is about 1.3mm × 1.1mm. The chip was mounted on the printing circuit board for testing. The golden wires were then bonded onto the chip to form the high-Q resonator. The optimized wire length can be obtained by repeated adjusting. A 2MHz crystal oscillator with phase noise of −148dBc/Hz at 10kHz offset was used as the input reference signal. The output signal spectrum is shown in Fig. 11 with a 1MHz span and in Fig. 12 with a 3MHz span. It can be calculated

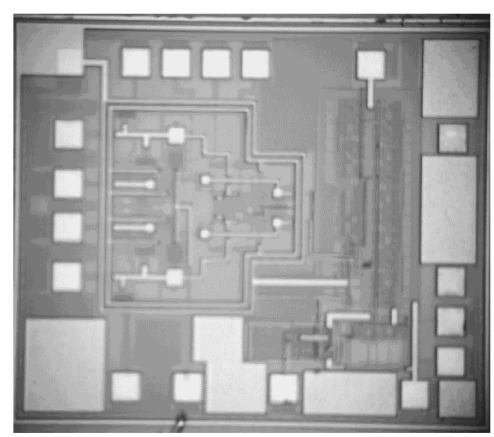

Fig. 10 Photograph of the SiGe BiCMOS PLL chip

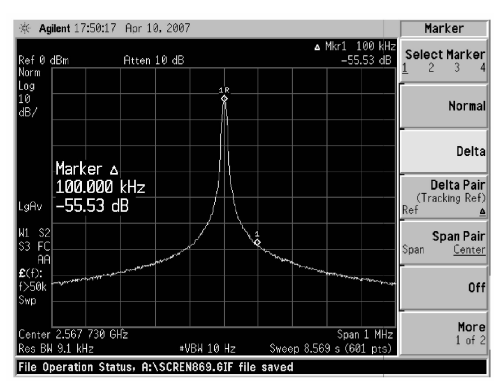

Fig. 11 Output spectrum with 1MHz span

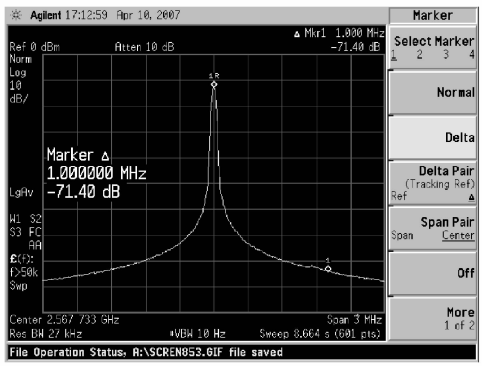

Fig. 12　Output spectrum with 3MHz span

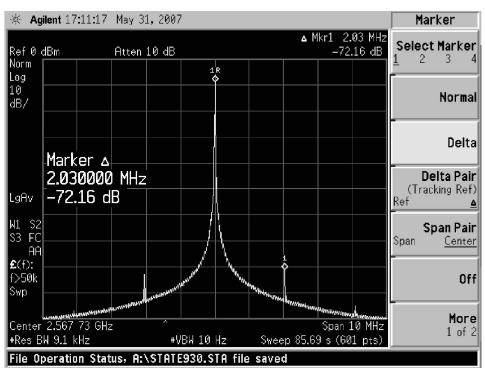

Fig. 13　Output spectrum with 10MHz span

from the spectrum that the phase noise is about −95dBc/Hz at 100kHz offset and −116dBc/Hz at 1MHz offset. Figure 13 shows the reference spur at 2MHz offset. It is about −72.16dB below the carrier power.

5　Conclusion

An integer-*N* PLL frequency synthesizer in 0.35μm SiGe BiCMOS is presented. Based on the different noise characteristics of the available devices and the different noise transfer functions of the PLL building blocks, different devices are used to implement building blocks in the PLL. Several design techniques are employed to optimize the spur and phase noise performance. The test results validate the feasibility of these techniques. At an offset of 100kHz and 1MHz from the carrier, the measured phase noise is −95dBc/Hz and −116dBc/Hz, respectively. The reference spur is less than −72dBc.

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基于 0.35μm SiGe BiCMOS 的高纯度频率综合器*

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摘要：介绍了一个基于 0.35μm SiGe BiCMOS 的整数 *N* 频率综合器. 通过采用不同工艺来实现不同模块，实现了一个具有良好的杂散和相噪性能的高纯度频率综合器. 除环路滤波器外所有的部件均采用差分电路结构. 为了进一步减小相位噪声，压控振荡器中采用绑定线来形成谐振. 该频率综合器可在 2.39～2.72 GHz 的频率范围内输出功率 0dBm. 在 100kHz 频偏处测得的相位噪声为 −95dBc/Hz，在 1MHz 频偏处测得的相位噪声为 −116dBc/Hz. 参考频率处杂散小于 −72dBc. 在 3V 的工作电压下，包括输出驱动级在内的整个芯片消耗 60mA 电流.

关键词：SiGe BiCMOS；锁相环；高纯度；环路带宽

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