Design of a 2.5GHz Low Phase-Noise LC-VCO in 0.35μm SiGe BiCMOS*

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Abstract: This paper introduces a 2.5GHz low phase-noise cross-coupled LC-VCO realized in 0.35μm SiGe BiCMOS technology. The conventional definition of a VCO operating regime is revised from a new perspective. Analysis shows the importance of inductance and bias current selection for oscillator phase noise optimization. Differences between CMOS and BJT VCO design strategy are then analyzed and the conclusions are summarized. In this implementation, bonding wires form the resonator to improve the phase noise performance. The VCO is then integrated with other components to form a PLL frequency synthesizer with a loop bandwidth of 30kHz. Measurement shows a phase noise of −95dBc/Hz at 100kHz offset and −116dBc/Hz at 1MHz offset from a 2.5GHz carrier. At a supply voltage of 3V, the VCO core consumes 8mA. To our knowledge, this is the first differential cross-coupled VCO in SiGe BiCMOS technology in China.

Key words: SiGe BiCMOS; VCO; inductance; phase noise
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1 Introduction

The recent exponential growth in wireless communication has increased the demand for more available channels in mobile communication applications. In turn, this demand has imposed more stringent requirements on the phase noise of local oscillators. The study of low phase noise voltage controlled oscillators has attracted a great deal of attention in the solid-stage community, leading both to a deeper understanding of theoretical issues[1,2] and to a considerable advancement in the state-of-the-art of the design of integrated VCO's[3,4].

Low phase noise VCOs may be implemented using various technologies. Previous works in this area included realizations with GaAs HBT[4], SiGe BiCMOS, Si CMOS[3], and silicon-on-insulator CMOS. Among these technologies, SiGe BiCMOS leads others from an application point of view because it combines the cost and integration advantages of silicon material systems with the performance advantage of SiGe HBTs. Compared to CMOS devices, BJT generally has a much higher transit frequency, larger transconductance, and smaller parasitics originating from smaller transistor size, and, hence, more accurate simulated oscillation frequency. Most of all, BJT devices have much lower flicker noise, making them suitable for low phase noise applications.

This paper introduces a 2.5GHz low phase-noise cross-coupled LC-VCO in a 0.35μm SiGe BiCMOS process.

2 Technology

The VCO was implemented in the commercially available Chartered 0.35μm 2P4M SiGe BiCMOS Process. The technology offers 3V and 5V n-p-n transistors with SIC implant, lateral and vertical p-n-p transistors, 65Ω/□ unsolicited poly SiGe and 1000Ω/□ high sheet R_{ho} poly resistors, accumulation-mode nMOS and p-n junction varactor, MOS, MIM and poly/n^+ sinker capacitors, electrostatic discharge protection devices, and CMOS transistors with a minimum gate length of 0.35μm. The n-p-n transistors have a transit frequency of 75GHz. It also provides spiral inductors implemented using a low series resistance (4μm thick) top metal.

3 Design strategy of BJT VCO

3.1 Importance of tank inductance selection

Lesson originally postulated that thermally induced phase noise in any oscillator takes the form of $L(\omega_m)=\frac{4FkTR}{V_0^2}\left(\frac{\omega_0}{2Q\omega_m}\right)^2$, where F is an unspecified noise factor. This formula holds well for both CMOS and BJT VCO. This formula indicates the phase noise is inversely proportional to the square of the signal oscillation amplitude and of the tank quality factor.

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Since the latter mainly depends on the available inductors and varactors, many design efforts focus on maximizing the oscillation amplitude without driving the active device into saturation.

Conventionally, two modes of operation, current- and voltage-limited regimes, can be identified by the oscillation amplitude for a typical LC oscillator[5]. In the current-limited regime, the tank amplitude V_{tank} linearly grows with the bias current according to $V_{\text{tank}} = I_{\text{bias}}/g_{\text{tank}}$, where g_{tank} is the equivalent conductance of the resonator. As the current increases, the oscillator enters the voltage-limited regime and the amplitude is limited to $V_{\max}$, which is determined by the supply voltage or a change in the operation mode of active devices. The boundary between the two regimes of operation represents an optimum point in terms of phase noise performance[1,5]. Generally, bias current is considered as the only independent variable determining the operation mode[1]. This leads to the ignoring of other design parameters, such as the tank inductance.

These two operation regimes can be reviewed from a different perspective, with tank inductance and tank current as the independent variables. For inductance L, the voltage swing resulting from a sinusoidal current stimulus $i(t) = I_{\text{tank}} \sin(wt + \varphi)$ can be expressed as $v(t) = L\dfrac{\mathrm{d}i(t)}{\mathrm{d}t} = wLI_{\text{tank}}\cos(wt + \varphi)$. The two operation regimes can now be redefined as follows: in the current-limited regime, the tank amplitude V_{tank} linearly grows with the product of tank inductance and tank current LI_{tank}. As LI_{tank} increases, the oscillator enters the voltage-limited regime with the amplitude limited to $V_{\max}$. This treatment emphasizes the role of tank inductance on operation mode and, thus, phase noise. For the required oscillation amplitude V_{req}, the tank current amplitude can be expressed with $I_{\text{tank}} = \dfrac{V_{\text{req}}}{wL}$. Since the tank current is proportional to the bias current, the optimization of phase noise depends on a deliberate compromise between bias current and tank inductance.

Figure 1 shows the simulated phase noise performance of a simplified cross-coupled oscillator with different bias current and tank inductance. The oscillator is designed to have a fixed oscillation frequency of 2GHz by adjusting tank capacitance. As can be seen from Fig. 1, the oscillator enters the voltage-limited mode, which is implied by the phase noise degradation, under smaller bias current when larger inductance is used. This observation verifies the role of tank inductance on operation mode. Figure 1 also suggests that smaller inductance generally leads to better optimum phase noise performance at the cost of more power consumption.

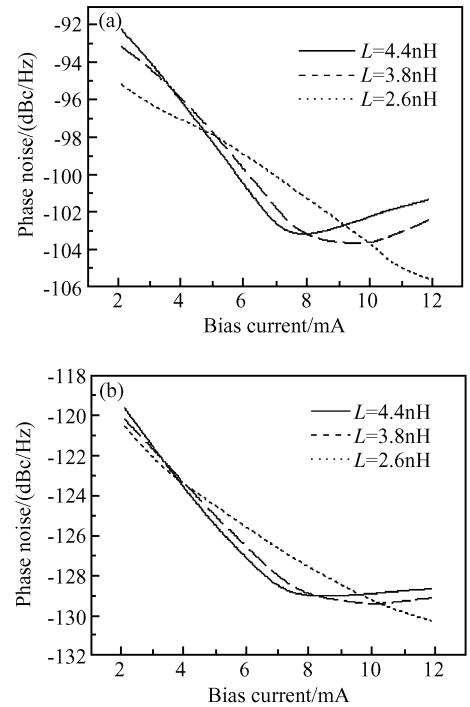

Fig. 1 Simulated phase noise versus bias current and inductance (a) At 100kHz offset; (b) At 1MHz offset

3.2 Design strategies for BJT and CMOS VCO

Distinct differences between CMOS and BJT VCO topologies are shown in Fig. 2. To keep the base-collector junction inverse biased, a voltage divider formed by two capacitors C_1 and C_2 is used in BJT VCO, as shown in Fig. 2 (a). The voltage feedback ratio is dependent on the capacitor ratio $\dfrac{C_1}{C_1 + C_2 + C_{\text{BE}}}$. Since no DC paths exist between the collector and base nodes, two extra resistors R_1 and R_2 are needed. The topology is much simpler for CMOS VCO, as shown in Fig. 2 (b). While most design attention is paid to the suppression of flicker noise up-conversion in CMOS VCO, it is reasonable for the BJT VCO design to concentrate on the thermal noise reduction.

Thermal noise from BJT base resistors is the most dominant noise source for BJT VCO. Transistors with large base areas are preferred for minimizing their noise contribution. Another factor affecting the noise contribution of base thermal noise is the voltage feedback ratio in BJT cross-coupled VCOs. Larger division ratios lead to better $1/f^2$ phase noise performance[6].

Parasitic resistance series with tank inductors is also a main thermal noise source. High-Q inductors are needed to reduce its noise contribution. High-Q inductors are also beneficial for saving power since they reduce the parallel parasitic equivalent resist-

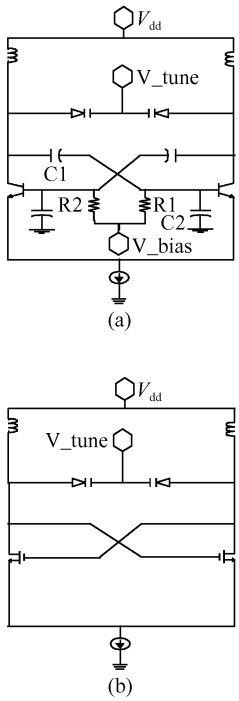

Fig.2　Topologies for CMOS (a) and BJT (b) VCOs

ance, which needs to be compensated by active devices. Compared with on-chip integrated inductors, bonding wires typically have quality factors at least an order of magnitude higher.

Design criteria derived for suppressing flicker noise up-conversion in CMOS VCOs do not apply to BJT VCO. In CMOS VCO, large cross-coupled device size generally leads to large flicker noise up-conversion because of the poor linearity and large parasitic[7]. Smaller CMOS devices are thus preferred. The situation is different for BJT VCO design. The linearity of the BJT cross-coupled pair is less independent of device size and thus no special attention needs to be paid to a BJT device size's role in flicker noise up-conversion. This property leads to relatively large device sizes in BJT VCO, which coincides with the reduction of thermal noise from BJT base resistor as discussed previously.

4　VCO implementation

The topology of the BJT VCO core is shown in Fig.3. The two varactors are DC grounded at the anodes to form a positive voltage-versus-frequency relationship. The tank inductors are implemented with bonding wires. Optimum length can be found by repeated adjusting. To compensate the inductance variation, capacitor banks are employed. The bias current of the VCO core is 8mA and the tank inductance is set to about 1.5nH. Two 10kΩ resistors realized with 1000Ω/□ high sheet R_{ho} poly resistors bias the BJT

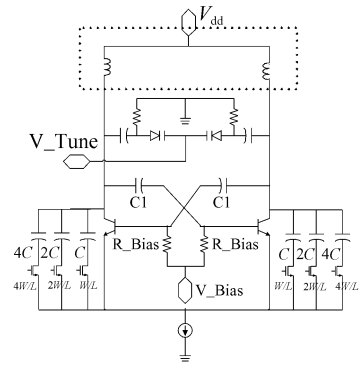

Fig.3　VCO core topology used in this design

devices with minimized degradation on phase noise. A high-Q accumulation-mode nMOS with a 0.58pF capacitance is used as the tank varactor. To increase the voltage division ratio, there is no capacitor in parallel with the BE junction of the BJT device. This leads to a maximal division ratio of $\frac{C_1}{C_1 + C_{BE}}$. C_1 is set to 0.2pF to ensure the base-collector junction does not become forward biased in the presence of a 600mV peak-to-peak swing. The base size of the BJT device is set to $2 \times 18.8\mu m \times 1.5\mu m$, which is a compromise between base and parasitic resistance. Four output buffers drive the differential prescaler and mixer inputs.

5　Test results

The cross-coupled differential VCO was integrated with other components to form an integrated-N PLL frequency synthesizer. The chip was fabricated in 0.35μm SiGe BiCMOS technology. The photograph of the fabricated chip is shown in Fig.4, and the active area of the VCO is about 0.6mm × 0.6mm. The chip was mounted on a printing circuit board for testing. Golden wires were then bonded onto the chip to form the high-Q resonator. The optimized wire length can be obtained by repeated adjusting. The output spectra of the frequency synthesizer with a centre frequency of about 2.5GHz are shown in Figs.5 and 6. The phase noise is −95dBc/Hz at 100kHz offset

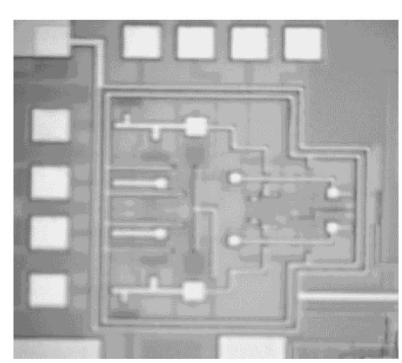

Fig.4　Photograph of the SiGe BiCMOS PLL

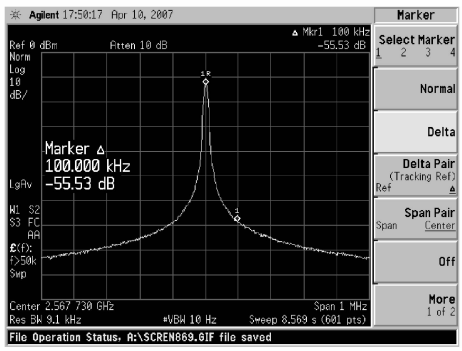

Fig. 5 Output spectrum with 1MHz span

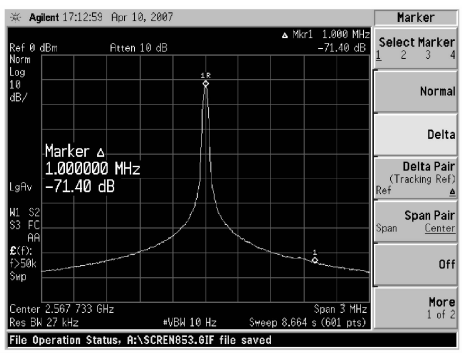

Fig. 6 Output spectrum with 3MHz span

and −116dBc/Hz at 1MHz offset. Since the loop bandwidth of the PLL is only 30kHz, the measurement results at offsets of 100kHz and 1MHz give good approximations of the VCO phase noise performance. The comparisons of this VCO and previous works in 0.35μm SiGe BiCMOS in terms of phase noise, power consumption, and chip size are summarized in Table 1.

Table 1 Comparison of various VCOs in 0.35μm SiGe BiCMOS

	Frequency /GHz	Phase noise /(dBc/Hz)	Power /(V×mA)	Chip size /(mm×mm)
This work	2.5	−95@100kHz −116@1MHz	3×8	0.6×0.6
Ref.[8]	2.45	−106@600kHz −110@1MHz	3×6.8	0.72×0.61
Ref.[9]	3	−95@25kHz −129@1MHz	2.5×9	0.4×0.4
Ref.[10]	2.7	−142@3MHz	2.8×10	NA
Ref.[11]	1.8	−98@100kHz	3×16	1.2×1.6
Ref.[12]	4.2	−113@1MHz	3.3×2	0.6

6 Conclusion

Design considerations for BJT VCO are studied in this paper. The role of inductance on VCO operation mode and phase noise performance is analyzed from a new perspective. Differences between BJT and CMOS VCO design are studied and techniques of phase noise reduction for cross-coupled BJT VCO are proposed. A SiGe BiCMOS differential VCO is then implemented and good phase noise performance is achieved. To our knowledge, this is the first differential VCO in SiGe BiCMOS technology in China.

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基于 0.35μm SiGe BiCMOS 的 2.5GHz 低相位噪声 LC 压控振荡器的设计*

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摘要：介绍了一个基于 0.35μm SiGe BiCMOS 工艺的 2.5GHz 低相位噪声 LC 压控振荡器.文章重新定义了压控振荡器工作区域.分析表明谐振回路的电感值和偏置电流对振荡器的相噪优化有重要的影响.本文同时分析了 CMOS 和 BJT 压控振荡器设计思路的不同.本设计中,采用键合线来实现谐振回路中的电感来进一步提高相噪性能.该 VCO 和其他模块集成在一起实现了一个环路带宽为 30kHz 的频率综合器.测试结果表明,当中心频率为 2.5GHz 时,在 100kHz 和 1MHz 的频偏处相噪分别为 -95dBc/Hz 和 -116dBc/Hz.工作电压为 3V 时,VCO 核心电路的电流消耗为 8mA.据我们所知,这是国内第一个采用 SiGe BiCMOS 工艺的差分压控振荡器.

关键词：SiGe BiCMOS；压控振荡器；电感值；相位噪声

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