A C-Band Monolithic GaAs PIN Diode SPST Switch*

Wu Rufei†, Zhang Jian, Yin Junjian, and Zhang Haiying

(*Institute of Microelectronics, Chinese Academy of Sciences, Beijing* 100029, *China*)

Abstract: A monolithic single pole single throw (SPST) switch is developed with GaAs PIN diode technology from IMECAS. A novel small signal model of a GaAs PIN diode is developed for circuit simulation. The switch features an on-state insertion loss of less than 1.6dB and a return loss of greater than 10dB while maintaining an off-state isolation of greater than 23dB from 5.5 to 7.5GHz. The measured 1dB power gain compression point is about 20dBm.

Key words: C-band; SPST; switches; GaAs; PIN diodes
PACC: 3220D; 7280E **EEACC**: 1350H; 2520D; 2570A
CLC number: TN454 **Document code**: A **Article ID**: 0253-4177(2008)05-0879-04

1 Introduction

In recent years, there has been a steady advance in implementing microwave systems in monolithically integrated circuits. These circuits will be the key for low cost, small size, and high volume production. Monolithic switches are widely used in transmit/receive communication systems. Monolithic GaAs PIN diodes have demonstrated superior performance in a number of switching and control circuits[1,2]. The low on-state resistance and low off-state capacitance of GaAs PIN diodes, coupled with their small physical size, allow circuit topologies not possible with field effect transistor (FET)-based technology.

This paper presents C-band monolithic GaAs PIN diode SPST switches. Different from the previously reported monolithic switches that employ planar PIN structures[3] or MESFET devices[4], the switches presented here employ epitaxial vertical PIN diode structures[5] in a shunt configuration optimized for low loss and high isolation under high-power signal conditions. The vertical epitaxial structure is expected to provide lower RF impedance under forward bias than planar ion-implanted PIN structures[6] and to have power handling capability superior to that of MESFET's.

The GaAs PIN diode process and small-signal model are described. The design of the SPST switch is presented. Finally, measurements of the SPST switch demonstrate an insertion loss of less than 1.6dB, an isolation of greater than 23dB, and a return loss of greater than 10dB from 5.5 to 7.5GHz.

2 GaAs PIN diode process and model

The diodes were manufactured on a wafer grown by molecular beam epitaxy (MBE), which provided by the Institute of Physics of Chinese Academy of Sciences. The vertical epitaxial structure results in minimized intrinsic resistance and increased carrier injection efficiency compared to a planar structure. The 25μm-radius diode has a 0.4μm-thick p^+ top layer with a hole concentration of $1\times10^{18}\sim5\times10^{19}\,cm^{-3}$. The hole concentration changes gradually in the p^+-layer, at the surface of which the hole concentration is $5\times10^{19}\,cm^{-3}$. The p^+-layer was followed by a 3-μm-thick intrinsic layer, which has a unintentional n-type doping of $1\times10^{15}\,cm^{-3}$. At the bottom is a 1μm, $3\times10^{18}\,cm^{-3}$ n^+-layer. The shape of the n^+-layer is semicircular, resulting in the elimination of a MIM parasitic capacitor. The diodes were fabricated on circular mesas using wet etching with $H_3PO_4:H_2O_2:H_2O=2:3:30$ solution. The p-type metal contact was made of Pt/Ti/Au. A Ni/Ge/Au/Ge/Ni/Au contact was then deposited on the n^+-layer. The contacts were concurrently annealed at 375℃ for 1min. The diodes were passivated with 0.5μm Si_3N_4. Electroplating was used to implement the electrode down-leads instead of evaporation since the evaporation is anisotropic and cannot cover the p^+- and i-layer step tightly, whereas the electroplating is isotropic. The diode structure is shown in Fig. 1. Table 1 demonstrates the main parameters of each layer. DC characterization of the diodes demonstrated turn-on voltage $V_{on}=1.1$V and reverse breakdown voltage $V_{BD}=-78$V.

* Project supposed by the National Natural Science Foundation of China (No. 10002909)
† Corresponding author. Email: rfwu04@mails.gucas.ac.cn
Received 29 October 2007, revised manuscript received 16 December 2007

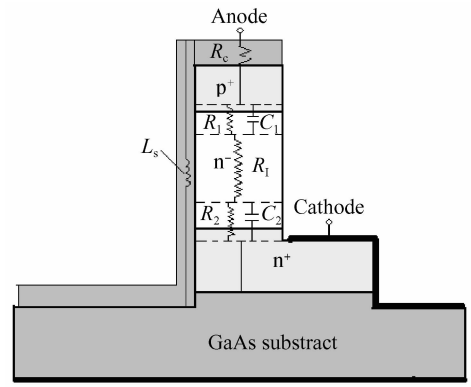

Fig. 1 Cross-sectional view

Table 1 GaAs PIN diode structure

Layer	Doping/cm^{-3}	Width/μm	Shape
p$^+$	$1\times10^{18}\sim5\times10^{19}$	0.4	Circular
i	1×10^{15}	3	Circular
n$^+$	3×10^{18}	1	Semicircular

The small novel signal equivalent circuit model for the GaAs PIN diodes was proposed by IMECAS[7], as shown in Fig. 2. The GaAs PIN diode is divided into three parts, namely the p$^+$n$^-$ junction, the i-layer, and the n$^-$n$^+$ junction, and modeled separately. The entire model of the PIN diode is then formed by combining the three sub-models. In this way, model accuracy is greatly enhanced. In this model, R_1 is the p$^+$n$^-$ junction intrinsic resistor, C_1 is the p$^+$n$^-$ junction capacitor, R_I is the i-layer resistor, R_2 is the n$^-$n$^+$ junction intrinsic resistor, C_2 is the n$^-$n$^+$ junction capacitor, L_s is the parasitic inductor, and R_c is the parasitic contact resistor. L_s and R_c both exist in anode and cathode, although Figure 1 is simplified and shows L_s and R_c only in anode. Excellent agreement is found between experiment measurement and model simulation. Figure 3 demonstrates the comparison between measurement and simulation under forward +10mA bias and reverse −10V bias.

3 Circuit design

A single pole single throw (SPST) switch circuit is designed with the GaAs PIN diodes presented in Section 2. The schematic of SPST switches with bias network is shown in Fig. 4. A shunt switch configuration is chosen to minimize the through insertion loss

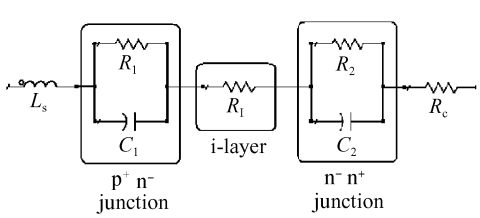

Fig. 2 Equivalent circuit model of GaAs PIN diodes

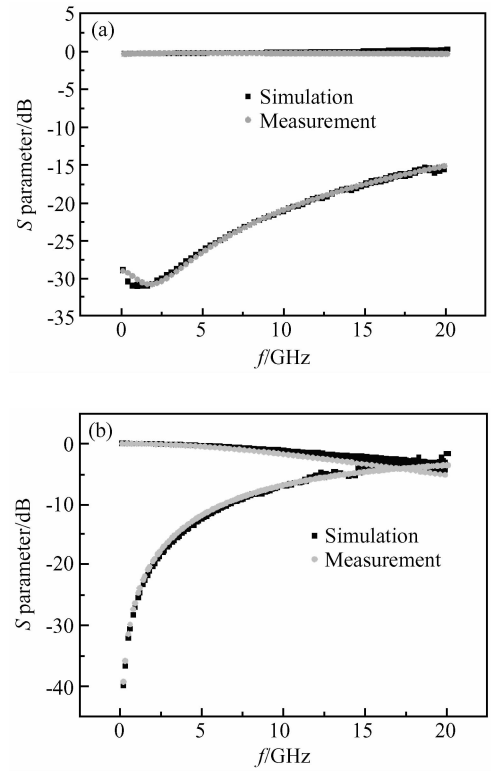

Fig. 3 Comparison between measurement and simulation (a) Under I_{on} = 10mA, radius of p$^+$ layer = 25μm; (b) Under V_{off} = −10V, radius of p$^+$ layer = 25μm

and maximize the isolation. The maximum achievable isolation and the minimum achievable insertion loss of the investigated switch are given in Eqs. (1) and (2)[8]. R_{on} is the on-state resistance of diodes, which is composed of i-layer small signal resistance, junction resistance, and parasitic contact resistance. C_{off} is the off-state capacitance of the diodes, which comprises junction capacitance and parasitic capacitance. In the switch circuits, the on-state resistance R_{on} is 1.3Ω at +10mA forward bias and the off-state capacitance C_{off} is 80fF at zero bias. Equations (1) and (2) indicate the diode off-state capacitance C_{off} plays an important role in determining the thorough insertion loss. At the same time, the isolation of the SPST switch can be improved by reducing the diode on-state resistance R_{on}.

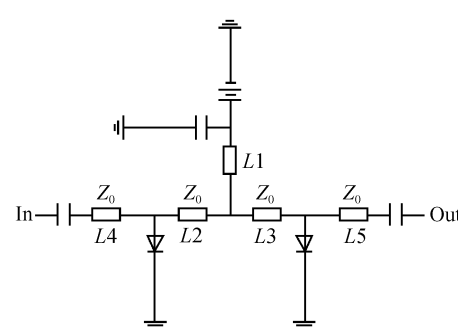

Fig. 4 Single pole single throw switch schematic

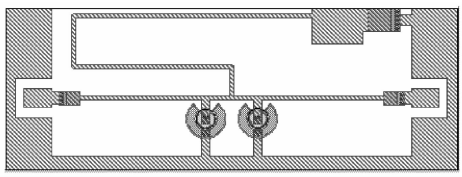

Fig. 5　Layout of GaAs PIN diode SPST switch

$$\text{Isolation(SPST}-2\text{diode)} = 40\lg\left(\frac{Z_0}{2R_{\text{on}}}\right) + 6\text{(dB)} \quad (1)$$

$$\text{Insertion(SPST}-2\text{diode)} = 20\lg[1+(\pi f C_{\text{off}} Z_0)^2]\text{(dB)} \quad (2)$$

The SPST switches are designed using high-impedance quarter-wavelength transmission line sections in order to obtain higher isolation according to Eq. (1): when the characteristic impedance of transmission line Z_0 is increased, the isolation of the SPST switch becomes higher. The isolation improvement results in increased insertion loss, calculated using Eq. (2), which makes the diode off-state capacitance C_{off} become more noticeable as the characteristic impedance of transmission line increases. Therefore, the value of Z_0 should be a tradeoff between low insertion loss and high isolation. Once the value of Z_0 is determined, it is crucial to minimize R_{on} and C_{off} at the same time. Transmission line $L1$ with high impedance in the bias network minimizes the signal leakage from the bias network. The width and length of $L4$ and $L5$ also need to be optimized to match the input and output impedance.

4　Small signal performance

The SPST switch circuit dimensions are 1890μm $\times$690μm. The layout of the SPST switch is shown in Fig. 5. The performance with an on-chip bias network SPST switch is measured under +1.6, 0, −0.5, −1, and −1.5V. For different reverse bias voltages, the comparison in terms of insertion loss and return loss is summarized in Table 2. The insertion losses increase as the bias voltage increases from zero to −1.5V and the return losses also increase as the reverse bias voltage increases, as shown in Fig. 6. This phenomenon results from PIN diode off-state capacitance, which increases when reverse bias voltage increases, causing more signal leakage from diodes to ground. Figures 7 and 8 show the insertion loss of an SPST

Table 2　Insertion loss and return loss under different reverse bias voltage

Reverse bias voltage /V	Insertion loss /dB	Return loss /dB
0	1.6	12.4
−0.2	1.9	13.1
−0.5	2.0	14.0
−0.8	2.2	14.6
−1.0	2.2	15.2
−1.2	2.6	15.9
−1.5	2.9	16.5

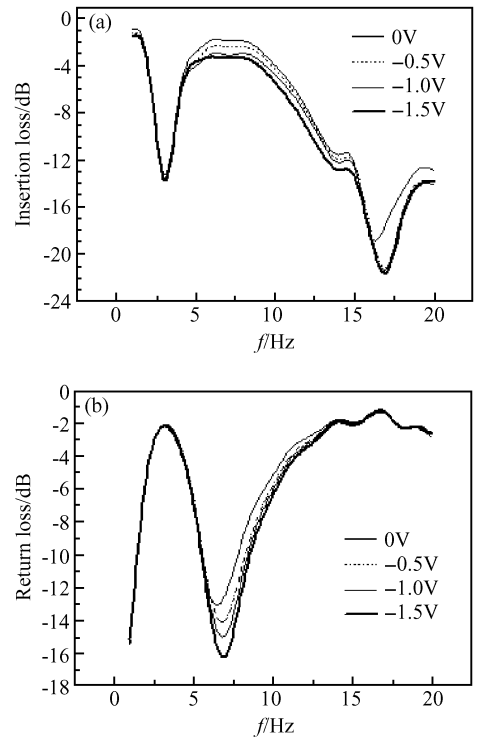

Fig. 6　Insertion loss (a) and return loss (b) under different bias voltages

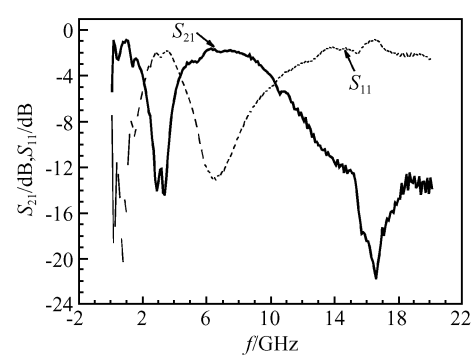

Fig. 7　Insertion loss of SPST switch under 0V

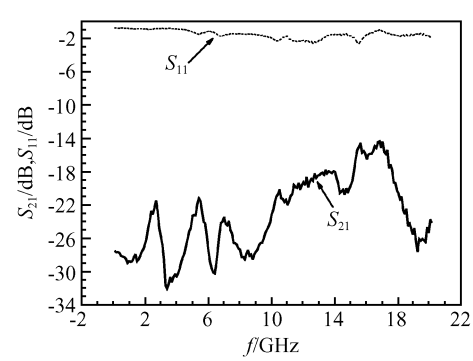

Fig. 8　Isolation of SPST switch under +1.6V

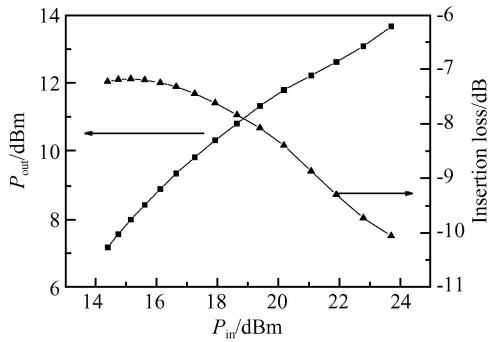

Fig. 9 Output power and insertion loss of SPST switch at 8GHz

switch under 0V and its isolation under +1.6V. In the range from 5.5 to 7.5GHz, the insertion loss is less than 1.6dB, while the return loss is larger than 10dB. The isolation is larger than 23dB from 5.5 to 7.5GHz. Moreover, the insertion loss of the switch will be further decreased by minimizing the off-state capacitance of GaAs PIN diodes.

The power-handling capability of GaAs PIN switches is evaluated on an automated on-wafer load-pull measurement system. Measurements are performed at 8GHz, at which large power signal sources are available. The P_{1dB} is about 20dBm, as shown in Fig. 9.

5 Conclusion

This paper reports a monolithic SPST switch based on the fabrication technology of GaAs PIN diodes from IMECAS. To simulate the SPST switch, a small signal model of GaAs PIN diodes is developed. The insertion loss of the SPST switch is less than 1.6dB under zero bias voltage and the isolation is larger than 23dB under a forward bias voltage of 1.6V. The performances of SPST switches under different reverse bias voltages are compared.

References

[1] Coats R, Klein J, Pritchett S, et al. A low-loss monolithic five-bit PIN diode phase shifter. IEEE MTT-S Digest, 1990: 915

[2] Seymour D, Heston D, Lehmann R, et al. X-band monolithic GaAs PIN diode variable attenuation limiter. IEEE MTT-S Digest, 1990: 841

[3] Nesbit G H, Chen J C, Wen C P, et al. Monolithic transmit/receive switch for millimeter-wave application. IEEE GaAs IC Symp Tech Digest, 1987: 147

[4] Lan G L, Dunn D L, Chen J C, et al. A high performance V-band monolithic FET transmit-receive switch. IEEE Microwave and Millimeter-Wave Monolithic Circuits Symp Digest, 1988: 99

[5] Tayrani R, Glew R W. Ultrafast GaAs microwave PIN diodes. Electron Lett, 1983, 19(13): 479

[6] Tayrani R, Bartle D C, Barrett N J. GaAs surface oriented microwave PIN diodes. IEEE GaAs Integrated Circuit Symp, 1984: 85

[7] Wu Rufei, Zhang Haiying, Yin Junjian, et al. A novel equivalent circuit model of GaAs PIN diodes. The 15th National Proceeding of Semiconductor Integrated Circuit and Silicon Material, 2007

[8] Chorney P. Multi-octave and multi-throw, PIN diode switches. Microwave Journal, 1974, 17(9): 39

C 波段 GaAs PIN 二极管单片单刀单掷开关*

吴茹菲† 张 健 尹军舰 张海英

(中国科学院微电子研究所，北京 100029)

摘要：基于中国科学院微电子研究所的 GaAs PIN 二极管工艺，研究了一种单片单刀单掷开关. 为了仿真该单片单刀单掷开关，研制开发了 GaAs PIN 二极管的小信号模型. 在 5.5～7.5GHz 的频段内，开关正向导通时的插入损耗低于 1.6dB，回波损耗大于 10dB，开关关断状态的隔离度大于 23dB.

关键词：C 波段；单刀单掷；开关；GaAs；PIN 二极管

PACC：3220D；7280E EEACC：1350H；2520D；2570A

中图分类号：TN454 **文献标识码**：A **文章编号**：0253-4177(2008)05-0879-04

* 国家自然科学基金资助项目(批准号：10002909)

† 通信作者. Email: rfwu04@mails.gucas.ac.cn

2007-10-29 收到，2007-12-16 定稿