A Total Dose Radiation Hardened PDSOI CMOS 3-Line to 8-Line Decoder

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Abstract: The first domestic total dose hardened 2μm partially depleted silicon-on-insulator (PDSOI) CMOS 3-line to 8-line decoder fabricated in SIMOX is demonstrated. The radiation performance is characterized by transistor threshold voltage shifts, circuit static leakage currents, and *I-V* curves as a function of total dose up to 3×10^5 rad(Si). The worst case threshold voltage shifts of the front channels are less than 20mV for nMOS transistors at 3×10^5 rad(Si) and follow-up irradiation and less than 70mV for the pMOS transistors. Furthermore, no significant radiation induced leakage currents and functional degeneration are observed.

Key words: PDSOI; decoder; total dose; radiation
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1 Introduction

Silicon-on-insulator (SOI) CMOS circuits have been widely used in the field of low-power and high performance ICs owing to their advantages in low junction-capacitance, reduced second order effects, and latch-up immunity[1]. Furthermore, the small volume of active silicon reduces their sensitivity to transient radiation, SEU, or dose rate, encountered in these environments[2~5]. Therefore, SOI technologies are of great interest for the purpose of radiation hardened space applications. Nevertheless, the thick buried oxide layer introduces an extra contribution to the total dose response unless radiation hardened.

Previous investigations have reported on radiation hardened PDSOI CMOS inverters[6], 1.2μm PDSOI 4kb[7] and 64kb SRAM[8], 0.8μm PDSOI 128kb SRAM[9,10], and 0.35μm PDSOI 256kb SRAM[11] fabricated in SIMOX material. This is the first domestic work on a radiation hardened 2μm PDSOI CMOS 3-line to 8-line decoder. The SOI radiation hardening process was developed using a front and back gate hardened, body-tie, lightly doped drain (LDD), and a hardened field oxide region. In this work, the radiation induced transistor front gate threshold voltage shifts, circuit static leakage currents, and *I-V* curves of 2μm PDSOI CMOS decoder as a function of total dose from 1×10^5 to 3×10^5 rad(Si) are reported.

2 Experiment

The decoder was fabricated in standard O^+ implanted SIMOX wafers acquired from SIMGUI. A high energy implantation of oxygen and a high temperature anneal resulted in approximately 375nm of buried oxide and approximately 390nm of top silicon. The HF decorated defect density was less than 0.5cm^{-2}[12]. The process steps for the 2μm PDSOI CMOS 3-line to 8-line decoder essentially included field implant, LOCOS isolation, n well and p well formation, V_{th} adjust and back gate implant, gate oxidation, poly Si gate process, LDD, side wall, nMOS and pMOS source/drain region formation, titanium silicide, contact, metal and final passivation. The high level doping concentrations of LOCOS field region and back gate channel region were proposed to mitigate the effects of radiation-induced charge trapping in the LOCOS and buried oxide on transistor performance. Furthermore, both body tied to source (BTS) and external body contacts were adopted to limit the kink effect and the action of the parasitic bipolar transistor inherent in PDSOI MOSFETs. The corresponding layout of the 2μm PDSOI CMOS decoder is shown in Fig. 1. The decoder chips were packaged in 16 lead ceramic dual-in-line metal seal packages.

The Co-60 irradiation facility at the Xinjiang Technical Institute of Physics and Chemistry of the Chinese Academy of Sciences was used for total dose radiation testing, providing a dose rate of 5.94×10^3 rad(Si)/min as measured from the Unidos dose tester. The ambient temperature of the testing environment was 25℃. The circuits were irradiated at the worst case radiation bias condition, which was stipulated by MIL-M-38510. Our decoders worst case was

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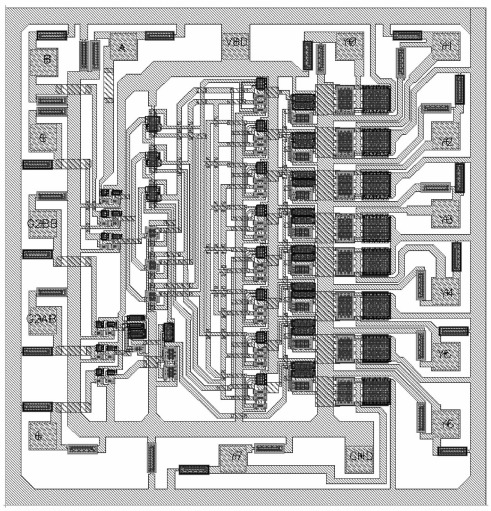

Fig.1　Layout of 2μm PDSOI CMOS decoder

that the 1,2,3,6,16 pins were connected to the supply voltage (V_{DD} = 5V), the 4,5,8 pins to ground, and all other terminals were floated. Moreover, the circuit radiation effect testing system was developed by the Xinjiang Technical Institute of Physics and Chemistry of Chinese Academy of Sciences, which provided the threshold voltage, static power current, and *I-V* curve measurements.

In order to investigate the response of the PDSOI CMOS decoders, which were irradiated and annealed after irradiation, two different test procedures were adopted. First, two sets of decoders were irradiated until the total dose achieved 1×10^5 rad(Si), then annealed at 25℃ for 24h. Fifty percent of the forenamed dose was added to the two sets of postirradiation decoders afterwards. Finally, these decoders were annealed at 80℃ for 168h. The second test procedure was similar to the first except the total dose of irradiation was 3×10^5 rad(Si) when the initial irradiation ended.

3　Results and discussion

Total dose degradation is caused by radiation-induced charge buildup in oxides. The total dose response of SOI circuits is more complex than for bulk-silicon circuits due to the buried oxide. Radiation-induced trapped charge in the gate oxide layer can degenerate the threshold voltage of the PDSOI MOSFETs. Moreover, radiation-induced trapped charge in the buried oxide can increase the leakage currents. So, we assessed the total dose hardness of the circuit by measuring the threshold voltage shifts and the leakage currents in packaged decoders. Figure 2 shows the *I-V* curves of 2μm PDSOI CMOS decoders as a function of total dose from 1×10^5 to 3×10^5 rad(Si).

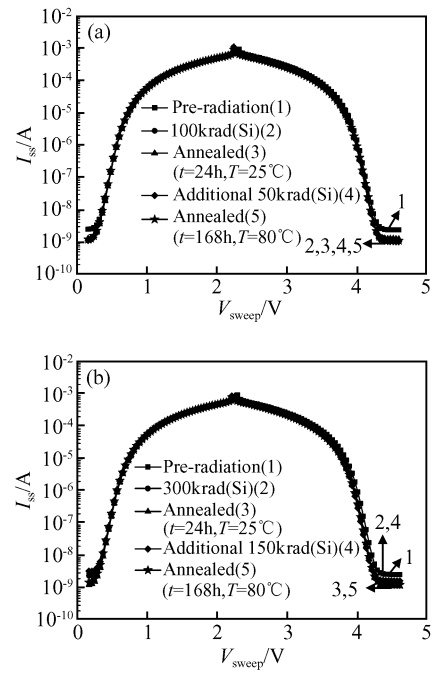

Fig.2　*I-V* characteristic curves as a function of total dose and annealing process　(a) Total dose = 1×10^5 rad(Si); (b) Total dose = 3×10^5 rad(Si)

The opposite sides of the curves were bilaterally symmetric and in an identical manner. With the additional radiation and annealing added on the decoders, the characteristics of the circuit changed little. This indicated that the radiation hardened nMOS and pMOS were matched well, the decoders were functioning normally, and the circuits were thus hardened to 3×10^5 rad(Si).

As shown in Fig. 2, the leakage currents of both 'off' and 'on' states dropped when the decoders were irradiated and annealed. This can be seen more clearly in Fig. 3, where the static leakage currents are shown as a function of total dose and annealing process. The leakage current dropped nearly 2nA at 1×10^5 rad(Si) and 3nA at 3×10^5 rad(Si) mainly because of 'pre-irradiation hardened' effects. The appropriate dose pre-irradiation could raise the threshold voltage which made the transistor more difficult to turn on. Thus, this effect compensated the influence of the positive radiation-induced trapped charge in the buried oxide. As a result, the radiation induced leakage currents were lowered. Nevertheless, when the cumulative total dose achieved a high level, the radiation-induced charge in the buried oxide and field oxide became large enough to cause an increase in the leakage currents. This prevents the top gate of the MOSFETs from turning off completely and even cased parametric and potentially functional failures. In general, little radiation induced leakage currents of our decoders at both 1×10^5 and 3×10^5 rad(Si) were

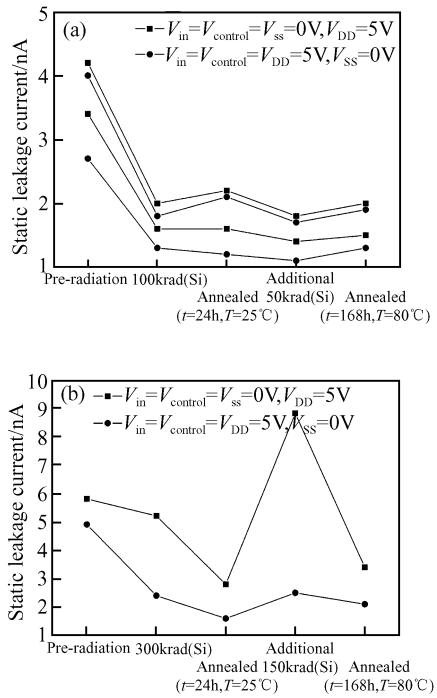

Fig. 3 Static leakage currents as a function of total dose and annealing process (a) Total dose = 1×10^5 rad(Si); (b) Total dose = 3×10^5 rad(Si)

observed.

In addition, the top gate threshold voltage shifts for the MOSFETs of the decoder in this study are shown in Figs. 4 and 5. Very small radiation induce threshold voltage shifts after irradiation and anneal were observed for both 1×10^5 and 3×10^5 rad(Si).

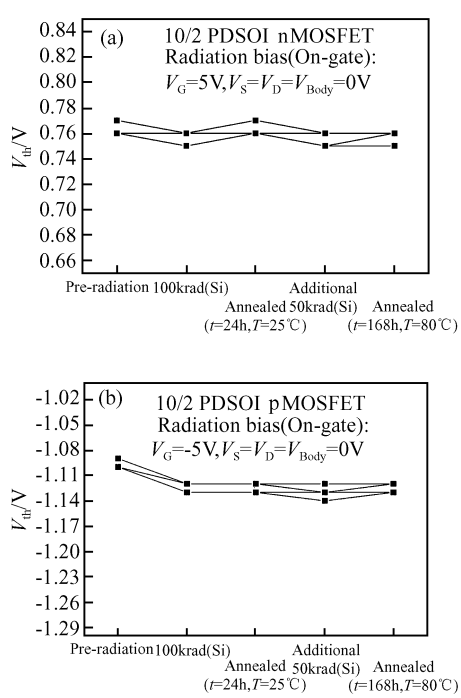

Fig. 4 Front channel threshold voltages of 10/2 nMOSFET and pMOSFET as a function of total dose and annealing process (Total dose = 1×10^5 rad(Si))

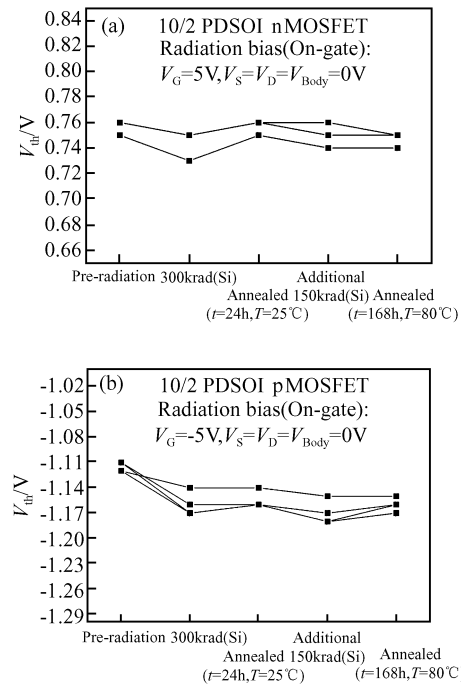

Fig. 5 Front channel threshold voltages of 10/2 nMOSFET and pMOSFET as a function of total dose and annealing process (Total dose = 3×10^5 rad(Si))

The worst case threshold voltage shifts of the front channels were less than 20mV for nMOS transistors and less than 70mV for pMOS transistors. Therefore, the gate oxide was hardened to 3×10^5 rad (Si).

4 Conclusion

In conclusion, 3×10^5 rad(Si) total dose hardened 2μm PDSOI CMOS 3-line to 8-line decoders have been fabricated in SIMOX. The worst case total dose radiation data, anneal, and additional irradiation performance have been demonstrated. The results suggest that the maximum front channel threshold voltage shifts were less than 20mV for nMOS transistors at 3×10^5 rad(Si) and follow-up irradiation and less than 70mV for pMOS transistors. In addition, no significant radiation induced leakage currents and functional degeneration were observed. Moreover, all electrical performance characteristics fell well with in the normal range. Therefore, this decoder will perform well in harsh radiation environments.

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总剂量辐照加固的 PDSOI CMOS 3 线－8 线译码器

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摘要：报道了一种制作在 SIMOX 晶圆之上的总计量加固的 2μm 部分耗尽 SOI CMOS 3 线—8 线译码器电路，其辐照特性由晶体管的阈值电压、电路的静态泄漏电流以及电流电压特性曲线表征. 实验表明，该译码器的抗总剂量能力达 3×10^5 rad(Si)，nMOS 管和 pMOS 管在最坏情况下前栅沟道阈值漂移分别小于 20 和 70mV，并且在辐照、退火以及后续追加辐照过程中无明显的泄漏电流增加，电路的功能并未退化.

关键词：部分耗尽 SOI；译码器；总剂量；辐照
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