A High-Performance Sample-and-Hold Circuit with Sampling Bandwidth Compensation

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Abstract: A novel charge exchanging compensation (CEC) technique is proposed for a wideband sample-and-hold (S/H) circuit applied in an IF sampling ADC. The CEC technique compensates the sampling bandwidth by eliminating the impact from finite on-resistance of the sampling switch, and avoids increasing clock feedthrough and charge injection. Meanwhile, a low power two stage OTA with a class AB output stage is designed to provide the S/H a 3Vp-p input range under 1.8V power. The S/H achieves a 94dB spurious-free dynamic range for a 200MHz input signal at a 100Ms/s sample rate and consumes only 26mW with a 5.5pF load.

Key words: bandwidth; sampling switch; spurious-free dynamic range; two-stage OTA; class AB output stage
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1 Introduction

Direct IF sampling for wireless communication places stringent requirements on the resolution, speed, and spurious-free dynamic range (SFDR) of ADCs[1]. To achieve and preserve the high performance for high input frequency, a wideband sample-and-hold (S/H) front end is necessary, which eliminates the aperture error and eases the sampling of the following stages.

Early works on wideband sampling concentrated mainly on improving the input switch. Techniques including bootstrapping[2,3], bulk effect compensation, bottom plate sampling, and feedthrough cancelation[4] have lowered the switch on-resistance and reduced the effect of switch non-idealities. Consequently, the bottleneck has shifted to the sampling switch. For high-accuracy wide-band sampling, simple CMOS sampling switches[3,5,6] can hardly meet the low on-resistance requirement. Clock-boosting[1,2,4] and capacitance coupling[6] are used to reduce the on-resistance. However, the increased gate voltage and size of the sampling switch introduce great clock feedthrough and charge injection, which limits the SFDR of the S/H.

In this paper, the limitation from the sampling switch is eliminated by adopting a novel charge exchanging compensation (CEC) that cancels the effect from the finite on-resistance of the sampling switch and suppresses the switch non-idealities. On the other hand, we design a high-swing power-efficient two stage OTA to guarantee the holding accuracy. At a 100Ms/s sample rate, the S/H achieves over 94dB SFDR with the input frequency up to 200MHz. Driving a 5.5pF load, the whole circuit consumes only 26mW under 1.8V power.

2 Circuit architecture

A flip-around S/H structure, shown in Fig. 1, was adopted for its advantages in power, capacitor area, and noise[2]. Non-overlapped clocks CK1D and CK2D control the sampling phase and holding phase, respectively. CK1 drops in advance of CK1D for bottom plate sampling.

The gain of the S/H is provided by a two stage OTA. With a class AB output stage, the OTA provides a large output swing to achieve a 3Vp-p differential input range under a 1.8V supply.

A bootstrapped nMOS switch similar to the structure in Ref. [3] is used as the input switch Si. It provides a very low and almost constant on-resistance for wideband sampling. The output switch Sl was also

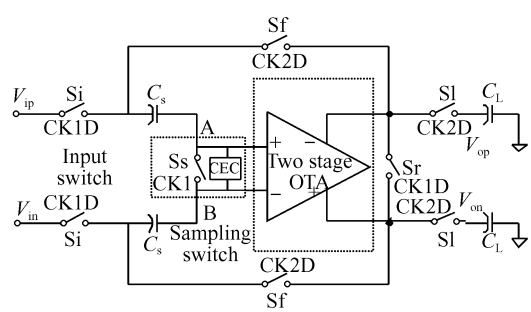

Fig. 1 Flip-around S/H architecture

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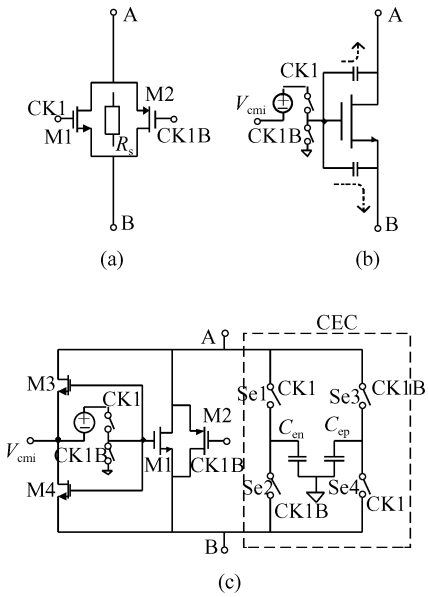

Fig. 2　Sampling switch schemes　(a) CMOS switch; (b) Large nMOS switch with boosted clock; (c) Proposed sampling switch

bootstrapped to keep the charging path to the load C_L expedient despite the large output swing. A small bootstrapped switch with fast turn on/off speed was used as the feedback switch Sf. The sampling switch Ss is designed with boosted clock and a CEC network, which will be introduced below.

3　Sampling switch with CEC

For high input frequency, the sampling linearity of the S/H circuit is dependent mainly on the bandwidth of the sampling network consisting of Si, C_s, and Ss[7]. With bootstrapped gate voltage and large size, Si normally has very low on-resistance, which shifts the bottleneck of the bandwidth to the sampling switch Ss.

Conventionally, a CMOS switch, as shown in Fig. 2 (a), is used for Ss. Since A and B (input nodes of the amplifier) are usually floating nodes around half of VDD, the limited gate-source voltage of the CMOS switch can hardly provide a very low on-resistance to maintain high SFDR under high input frequency[3,5]. Even worse, the floating CMOS switch may be unworkable under low supply voltage[6]. A nMOS switch with a boosted clock and a large size, as shown in Fig. 2 (b), can reduce the on-resistance. But great clock feedthrough is introduced, which will cause differential error to nodes A and B due to the mismatch between the paths. In this work, as shown in Fig. 2 (c), the size of the nMOS switch M1 is limited for a minimal feedthrough, and the resulting bandwidth reduction is compensated by the CEC network.

The CEC network consists of two error sampling

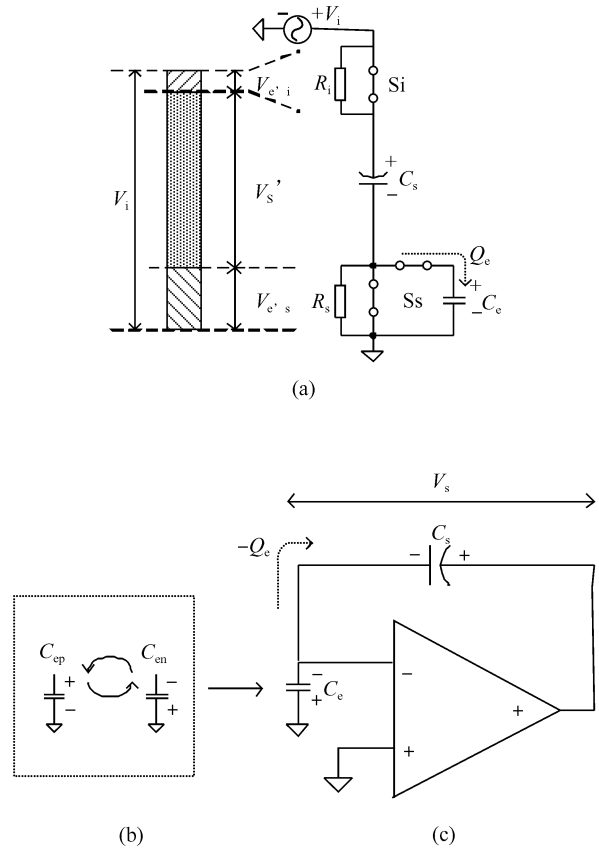

Fig. 3　CEC compensation　(a) Sampling phase; (b) Charge exchanging; (c) Holding phase

capacitors C_{ep}, C_{en} and their respective exchanging switches Se1～Se4. The compensation is accomplished by exchanging the charge sampled by C_{ep} and C_{en}, which is explained below.

Single side circuits of the sampling and holding phase are shown in Fig. 3 (a)～(c), where C_e represents either C_{ep} or C_{en} in one side. When high frequency input signal V_i is sampled by the low pass sampling network, it will attenuate to V_s' across C_s. The error voltage will be distributed on Si and Ss (with on-resistance of R_i and R_s) as $V_{e,i}$ and $V_{e,s}$. C_e is used to sample the error voltage $V_{e,s}$. The charge sampled by C_s and C_e is given below:

$$\begin{cases} Q_s(s) = \dfrac{1}{1 + s\left(R_i + R_s \dfrac{1}{1 + sR_sC_e}\right)C_s} C_s \\ Q_e(s) = \dfrac{\dfrac{sR_sC_s}{1 + sR_sC_e}}{1 + s\left(R_i + R_s \dfrac{1}{1 + sR_sC_e}\right)C_s} C_e \end{cases} \tag{1}$$

By returning Q_e to C_s, the error from the sampling switch will be compensated, which is done during the holding phase. Before this step, the polarity of Q_e should be reversed, since the top plate of C_s stores negative charge against Q_e. This reversal is achieved by exchanging the connection of C_{ep} and C_{en} with Se1～Se4, as shown in Fig. 3 (b).

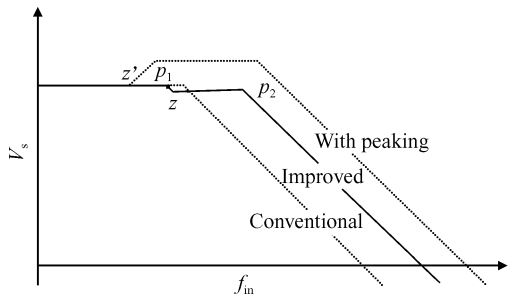

Fig. 4 Improved equivalent sampling bandwidth

Once the holding phase starts, C_s and C_e form the charge redistribution structure shown in Fig. 3. The error charge Q_e is squeezed from C_e and transferred to C_s. The final compensated sampled voltage is:

$$V_s(s)=\frac{1+s\times 2R_sC_e}{s^2R_iR_sC_sC_e+s(R_sC_s+R_sC_e+R_iC_s)+1}V_i(s) \quad (2)$$

With the assumption $R_s \gg R_i$, the poles and zero of the transfer function of V_s can be concluded as follows and the transfer curve is drawn in Fig. 4.

$$p_1=\frac{1}{R_s(C_s+C_e)},\ p_2=\frac{C_s+C_e}{R_iC_sC_e},\ z=\frac{1}{2R_sC_e} \quad (3)$$

The compensation result depends on the ratio $k=C_e/C_s$. When $k<1$, increasing k will move z towards p_1, which will flatten the band. When $k=1$, p_1 can be completely canceled by z, and a perfect compensation is achieved. The bandwidth will thus be increased by $2(R_i+R_s)/R_i$. However, if $k>1$, peaking will occur due to the advancement of z, which will increase distortion again. The transfer curves with different values of k are simulated in MATLAB as shown in Fig. 5. The greatest bandwidth improvement is achieved when k is around 1. However, it is also economical to shift k towards 0.5, which will save area and power at the cost of a small bandwidth lost.

The above analysis neglects the effect of the on-resistance of Se1～Se4, which may cause attenuation in error sampling. However, since the amplitude of $V_{e,s}$ is much smaller than V_i, the on-resistance requirement for Se1～Se4 is relaxed. With small sizes, the charge injection and clock feedthrough introduced by Se1～Se4 are not obvious. Moreover, the injection/feedthrough will be cancelled by their complementary switching sequence.

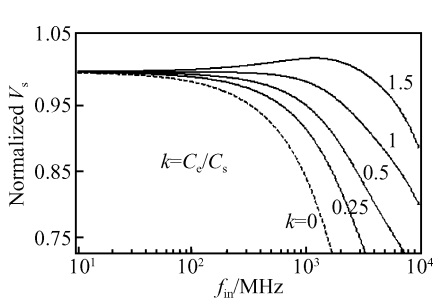

Fig. 5 Input bandwidth versus C_e

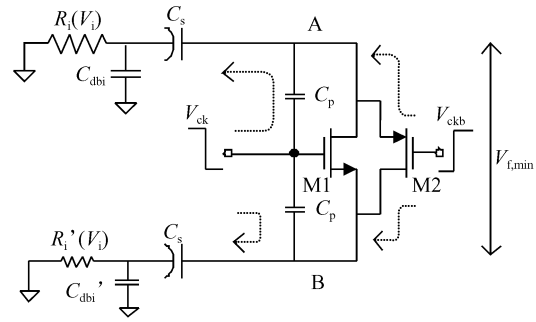

Fig. 6 Mismatch of clock feedthrough to A and B

Besides the finite R_s, the clock feedthrough of Ss is also a major error source. As depicted in Fig. 6, the clock drop is coupled to A and B through the parasitic capacitor C_p. Since on-resistance (R_i, R_i') and the junction capacitors (C_{dbi}, C_{dbi}') of the input switch depend on the input voltage V_{in} due to the bulk effect, there is an impedance mismatch between the two feedthrough paths. This will cause a feedthrough mismatch $V_{f,mis}$ between A and B.

$$V_{f,mis}(s)\doteq-\frac{(s^2R_i^2C_s\Delta_{Cdbi}+s\Delta_{Ri}C_s)}{(sR_i(C_{dbi}+C_p)+1)^2}\times\frac{C_p^2}{C_s^2}V_{ck}(s) \quad (4)$$

where $\Delta_{Ri}=R_i'-R_i$, $\Delta_{Cdbi}=C_{dbi}'-C_{dbi}$. The equation shows that the effect from C_p is greater than that from V_{ck}, since $V_{f,mis}$ is proportional to C_p^2. Thus, to lower the on-resistance, it is preferable to increase the clock voltage V_{ck} rather than to enlarge the switch size. Consequently, in this work, Ss has a boosted clock and reduced size. In addition, as in Fig. 2(c), a pMOS switch M2 is adopted to introduce a negative clock edge to compensate partially the clock feedthrough mismatch. Two small nMOS switches M3 and M4 help A and B recover to the desired common mode voltage V_{cmi}.

4 OTA design

The structure of the adopted two-stage OTA is shown in Fig. 7. The first stage of the OTA is based on a gain-boosted telescopic structure, which provides about 90dB voltage gain for the OTA. The output stage is based on a Class AB structure. With the transistors biased near the weak inversion region, the output stage can achieve 1.5V swing under a 1.8V supply, which guarantees a 3Vp-p input range for the S/H. For KT/C noise consideration, having a large input range allows the use of smaller capacitors in the whole ADC (50% smaller compared with 2Vp-p), which in turn reduce the power. On the other hand,

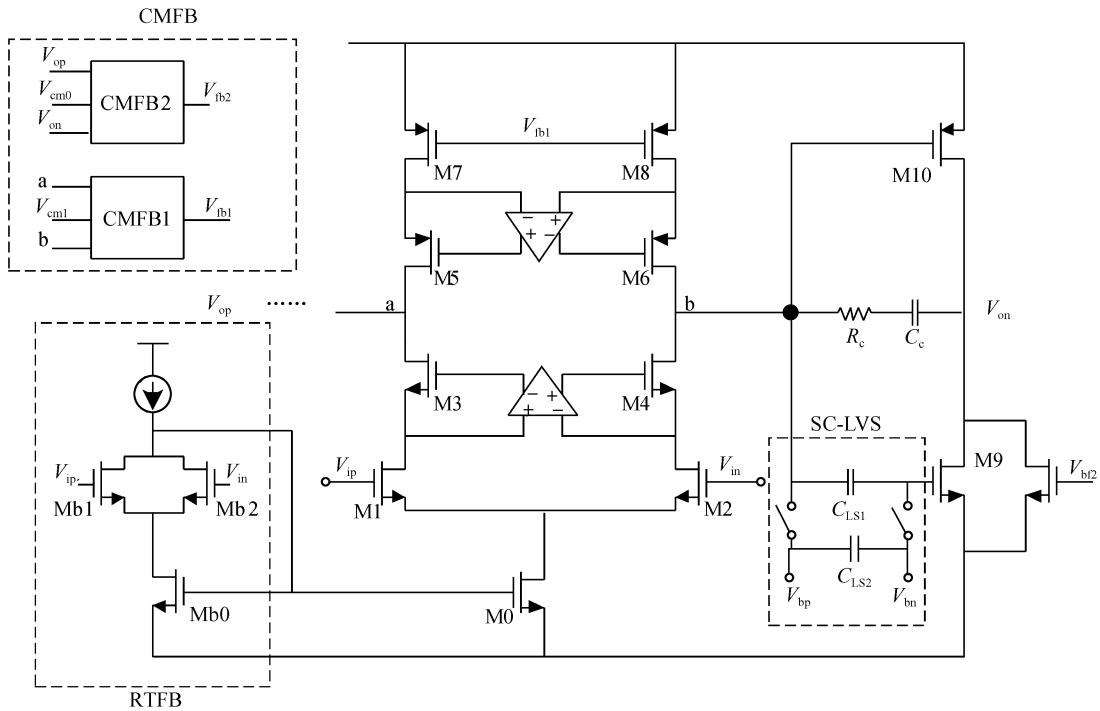

Fig. 7　Two stage OTA with class AB output stage

two transistors contribute to the g_M of the output stage rather than the one in Class A mode, which leads to a current reduction about 40%.

A switched-capacitor level shifter (SC-LVS) is adopted to connect the output of the first stage and the nMOS input of the second stage[8]. Two switched capacitor common mode feed back (SC-CMFB) circuits are used to stabilize the output common mode voltage of stage1 and stage2.

A simplified replica-tail feedback bias (RTFB)[9] is adopted to keep the tail current immune to the input common mode voltage variation. Otherwise, the gain of the OTA will change with the tail current, causing nonlinearity to the differential output.

Since the adoption of CEC lowers the feedback factor, the g_M of the first stage needs to be increased to maintain a closed loop bandwidth equal to the case without CEC. However, the g_M of the second stage needs no increment, since the position of non-dominant pole in the second stage is required by the closed loop bandwidth and phase margin, which is unchanged. Thus, the power used for the CEC is not obvious. The simulated performance of the OTA is summarized in Table 1.

Table 1　OTA performance

Load capacitor	5.5pF
Output swing	1.5Vp-p
DC gain	115dB
Close loop BW	830MHz
Close loop PM	74°
Settling time	3.3ns (0.1‰ accuracy)

5　Simulation results

The S/H circuit (Fig. 1) is designed in an SMIC 0.18μm process and simulated with HSPICE. The results given below are for the slowest cases. In Fig. 8, the simulated CEC course with full compensation

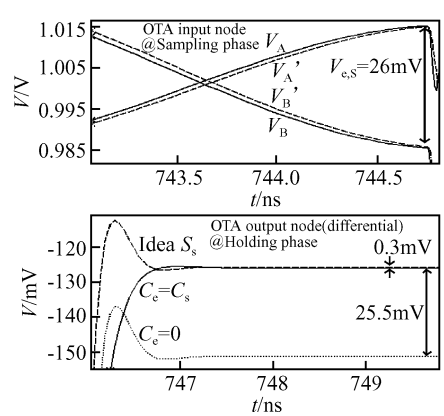

Fig. 8　Simulated CEC course under a 198MHz 3Vp-p input

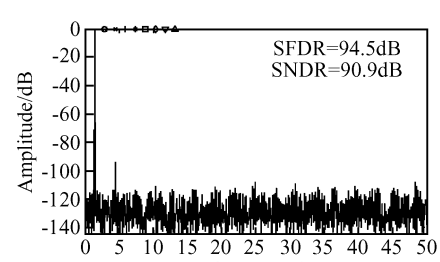

Fig. 9　Spectrum of a 198MHz 3Vp-p input at 100Ms/s

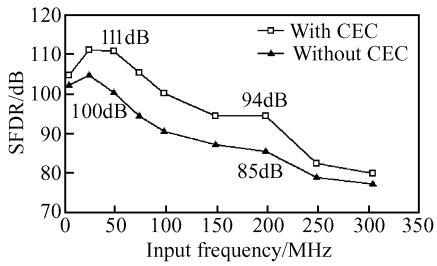

Fig. 10 SFDR performance of the proposed S/H

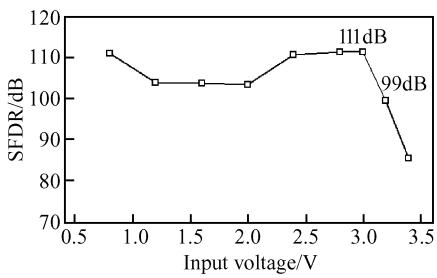

Fig. 11 SFDR versus input amplitude f_{in} = 48MHz@100Ms/s

(taking $C_e/C_s = 1$) is shown. During the sampling phase, a 198MHz 3Vp-p input causes a voltage error $V_{e,s}$ across the OTA input node (V_A, V_B) with a maximum amplitude of 26mV, which is sampled by the CEC capacitor as V_A', V_B'. During the holding phase, the error is returned to the differential output. The compensated result is compared with the case with an ideal sampling switch ($R_{on} = 0.5\Omega$) and the case without CEC ($C_e = 0$). The sampling error is reduced from 25.5mV to only 0.3mV with the aid of CEC.

Figure 9 shows the output spectrum for a 198MHz input signal under a 100Ms/s sampling rate, with the SFDR of 94dB. Figure 10 shows a performance comparison between the cases with the CEC added or removed. The SFDR is improved by about 10dB by the CEC in the zone from 50 to 200MHz. For the 90dB SFDR level, the CEC extends the sampling bandwidth from 100 to over 200MHz. For even higher frequency, the S/H achieves 80dB for a 300MHz input.

Figure 11 shows the SFDR performance versus input amplitude with 48MHz input and a 100Ms/s sampling rate. The circuit can achieve 99dB SFDR even when the input range reaches 3.2Vp-p. The whole circuit consumes 26mW under a 1.8V power supply. A performance summary of the S/H circuit is shown in Table 2

Table 2 Performance summary

	CEC	No CEC
Process	0.18μm	
Supply voltage	1.8V	
Sample rate	100Ms/s	
Input range	3Vp-p	
Power	26mW	24mW
SFDR @ 48MHz	111dB	100dB
SFDR @ 198MHz	94dB	85dB

6 Conclusion

In this paper, a novel CEC technique that extends the sampling bandwidth by compensating the finite on-resistance of the sampling switch is presented and analyzed. Meanwhile, a two stage OTA with class AB output is designed to provide the S/H a wide input range. Working at a 100Ms/s sampling rate, the S/H achieves very good linearity within a 200MHz input bandwidth and consumes only 26mW power.

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一种具有采样带宽补偿的高性能采样/保持电路

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摘要：针对中频采样模数装换器中的宽带采样/保持电路，提出了一种新颖的电荷交换补偿（CEC）技术.该技术通过消除采样开关有限导通电阻的影响，补偿了采样带宽，并避免了时钟馈通和电荷注入的加剧.同时设计了具有 AB 类输出的低功耗两级运放，在 1.8V 电源下为该采样/保持提供了 3V 峰-峰值的输入范围.该采样/保持电路在 100Ms/s 的采样率下，对于 200MHz 输入信号达到了 94dB 的无杂散动态范围.在 5.5pF 的负载下，功耗仅为 26mW.

关键词：带宽；采样开关；无杂散动态范围；两级运放；AB 类输出级

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