Concept and Design of a Novel High-Bandwidth, High-Sensitivity Differential Receiver for Optical Interconnections*

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Abstract: A novel high-bandwidth, high-sensitivity differential optical receiver without any additional cost compared to general optical receivers, is proposed for high-speed optical communications and interconnections. High bandwidth and high sensitivity are achieved through a fully differential transimpedance amplifier with balanced input loads and two photodetectors to convert the incident light into a pair of differential photogenerated currents, respectively. In addition, a corresponding 0.35μm standard CMOS optoelectronic integrated receiver with two 60μm × 30μm, 1.483pF fingered p^+/n-well/p-substrate photodiodes is also presented. The simulation results demonstrate that it achieves a 1.37GHz bandwidth and a 81.9dBΩ transimpedance gain, supporting data rates up to at least 2Gbit/s. The device consumes a core area of 0.198mm^2 and the optical sensitivity is at least −13dBm for a 10^{-12} bit error rate under a $2^{15}-1$ PRBS input signal.

Key words: high-bandwidth; high-sensitivity; CMOS; optical receiver
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1 Introduction

Differential optical receivers are commonly applied in high-speed fiber communications because of their high immunity to common-node noises and their high stability. Progress has also been made recently based on CMOS processes. References[1~3] have reported several high-speed CMOS differential optical receivers, some of which achieve a 3.125Gb/s data rate. However, all of these receivers are either hybrid-integrated[1,2] or inapplicable[3] because of the poor responsivity of standard CMOS photodetectors and the tradeoff limitation between the sensitivity and the bandwidth.

To solve these issues, the concept of a novel high-bandwidth, high-sensitivity differential optical receiver is proposed based on general differential optical receivers. A corresponding differential optoelectronic integrated receiver is also presented in an unmodified Chartered 0.35μm standard analog CMOS 2P4M, 3.3V process.

2 Concept of a novel differential optical receiver

In this section, a method for improving the bandwidth of a single-beam differential transimpedance amplifier (TIA) is introduced. Then, a novel method of doubling a single-beam differential optical receiver's sensitivity is proposed. Combining these two methods, a high-bandwidth, high-sensitivity differential optical receiver is acquired.

2.1 High bandwidth design of differential TIAs

In the high-frequency domain, differential amplifiers are commonly used for overcoming instability caused by supply variations and parasitic inductors' effect of bonding wires[4]. In addition, a differential amplifier can also achieve a cut-off frequency twice as high as a single-input, single-ended amplifier[5]. A doubling of bandwidth could be achieved if the two input loads of a conventional single-beam differential TIA are balanced, which could be implemented by adding a dummy capacitor[2] or a shaded detector[3], or by applying a spatially modulated photo-detector[1,6].

Figure 1(a) is a differential TIA with balanced input loads proposed to acquire high bandwidth, where C_{d1} is a dummy capacitor added for input load balancing. The capacitance of C_{d1} is equal to the pn-junction capacitance of the 40μm × 40μm, 1.313pF p^+/n-well photodiode D1, supplied in a Chartered 0.35μm standard analog CMOS 2P4M, 3.3V process. In the circuit design, nMOS transistors are applied here to replace load resistors for stable performance

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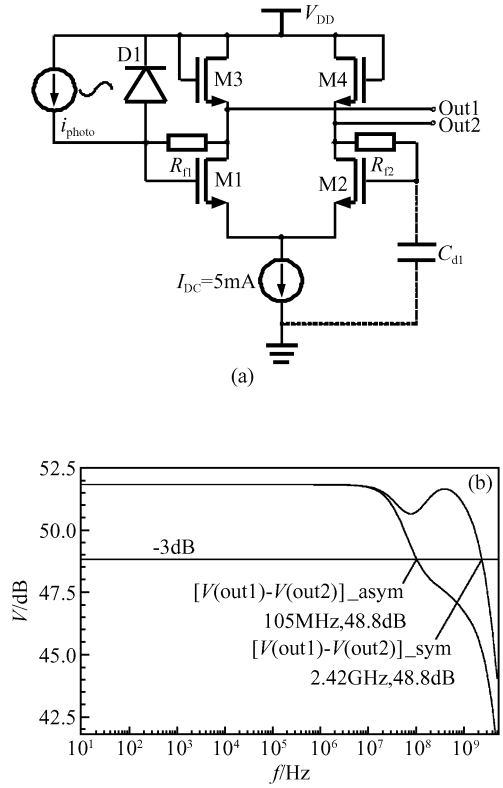

Fig. 1 A differential TIA with balanced input loads (a) Schematic; (b) Frequency response

because of the resistors' poor precision. Figure 1(b) is the simulated frequency response characteristic acquired by a Cadence Spectre Simulator with the Chartered 0.35μm standard analog CMOS 2P4M, 3.3V process model library, where [V(out1)-V(out2)]_asym and [V(out1)-V(out2)]_sym are the results without and with the dummy capacitor C_{d1}, respectively. The differential TIA has a great improvement in bandwidth, from 105MHz to 2.42GHz.

2.2 Circuit architecture of a novel differential optical receiver

Though differential TIAs with balanced input loads could double the bandwidth, the branches for input loads balancing do not contribute to incident light sensing[1,3,6]. To improve optical sensitivity, a novel fully differential TIA is proposed in Fig. 2(a). The biggest distinction of this TIA is that a dummy capacitor or a shaded photodiode for input loads balancing in a conventional differential TIA is replaced with an illuminated photodiode, that is, two completely identical illuminated photodiodes are applied here to convert the incident light into a pair of differential photogenerated currents.

To maintain balanced input loads, D1 and D2 should be designed with the same size and work at the same reverse bias. Thus, DC operating voltages at the differential TIA's two input nodes should both be $V_{DD}/2$. When the receiver works, the photo-currents generated by D1 and D2 will be approximately equal to i_{photo}, but with opposite current directions. It acts like there is a current source i_{photo} between the two input ports of the differential TIA. Consequently, the total input photo-current is $2i_{photo}$, twice that of a conventional differential TIA, and the doubling of sensitivity is achieved.

Figure 2(a) is the circuit architecture of the novel high-bandwidth, high-sensitivity differential optical receiver proposed in this paper. The TIA is the aforementioned fully differential transimpedance amplifier, the LMA is comprised of several stages of a fully differential amplifier, and the DFSO is a differential to single-ended output buffer.

Another prominent advantage of the differential optical receiver is that no additional fiber is needed and no extra cost is produced compared to conventional single-beam differential receivers. Taking the example of fingered p^+/n-well/p-substrate photodiodes[7], the two photodiodes could be placed side by side as in Fig. 2(b). Therefore, they can acquire incident lights from only one fiber simultaneously.

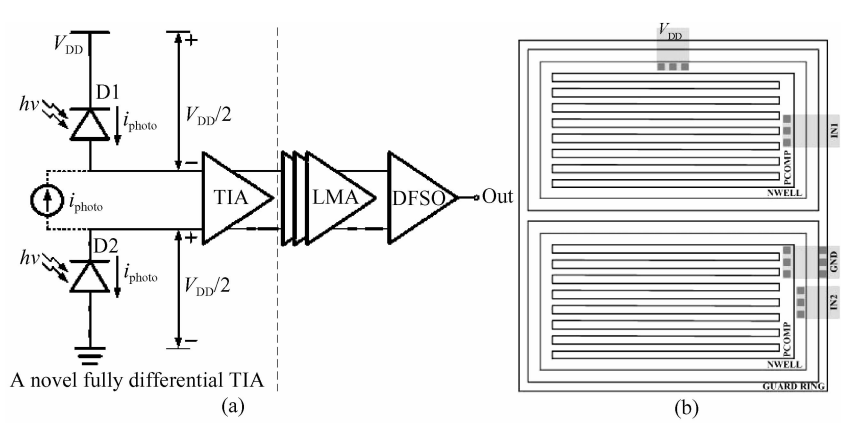

Fig. 2 A novel high-bandwidth, high-sensitivity differential optical receiver (a) Circuit diagram; (b) Layout of the two illuminated photo-detectors

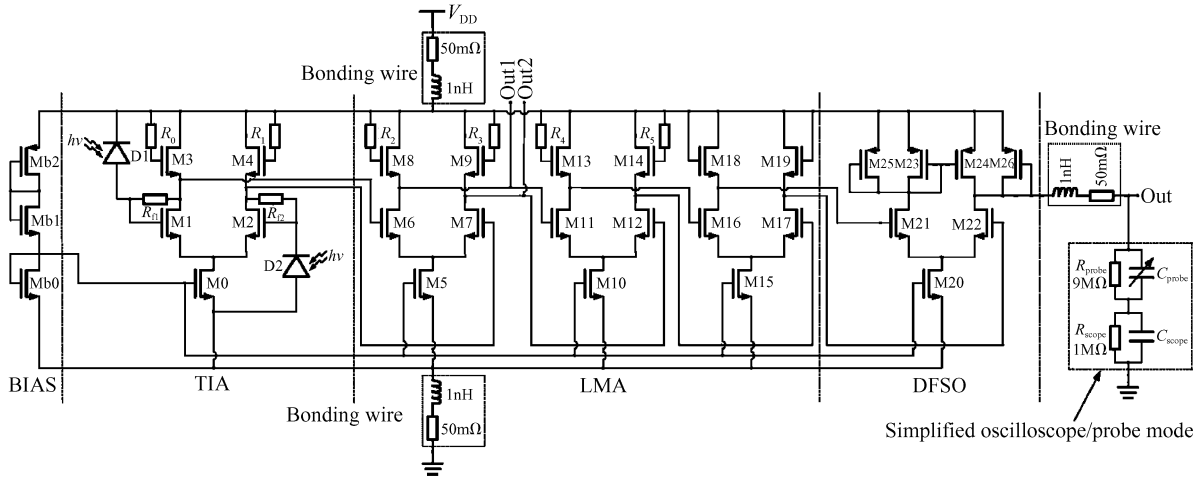

Fig. 3　A standard CMOS implementation of the novel differential optical receiver

3　Design of a standard CMOS optoelectronic integrated receiver

Most back-end digital processing cells in fiber communication systems have been implemented in standard CMOS processes. However, no applicable standard CMOS optical receivers have been reported yet. In this section, a high-bandwidth, high-sensitivity CMOS differential optoelectronic integrated receiver is presented, which shows a great potential for commercial applications.

3.1　Circuit design

Figure 3 is a standard CMOS integration example of the receiver shown in Fig. 2(a) in a Chartered 0.35μm standard analog CMOS 2P4M, 3.3V process on p-type substrate. In the design, two 60μm×30μm, 1.483pF fingered p^+/n-well/p-substrate photodiodes[7], D1 and D2, sense 850nm incident light signals. The photodiode is fully compatible with standard CMOS processes, where the n-well region of the photodiode and the n-well (substrate) regions of pMOS transistors are fabricated simultaneously. The fingered p^+ region and the p^+ guard ring of the photodiode and the p^+ (source and drain) regions of pMOS transistors are fabricated simultaneously. The pn-junction capacitance of the photodiode is acquired by layout extraction. The LMA is composed of three low-gain, high-bandwidth fully differential amplifiers. Except the TIA, LMA, and DFSO, an additional BIAS stage is also needed to supply a bias current for the whole chip. For bandwidth enhancement, folded active inductors[7] are also used, such as R_0 and M3, R_1 and M4, R_2 and M8, R_3 and M9, R_4 and M13, and R_5 and M14.

In the high-frequency domain above gigahertz, it is significant to take parasitic inductors of bonding wires into consideration. Usually, a 1mm bonding wire will produce about a 1nH parasitic inductor[8]. Therefore, the circuit model of a bonding wire can be equivalent to the series of a 1nH inductor and a 50mΩ resistor (large enough for a bonding wire's resistance), shown in Fig. 3. Excluding the parasitic inductors, the circuit model of the oscilloscope / probe system[5] is also considered in the design.

3.2　Simulated performance

Figures 4 and 5 are the simulated results acquired by a cadence spectre simulator with the Chartered 0.35μm standard analog CMOS 2P4M, 3.3V process

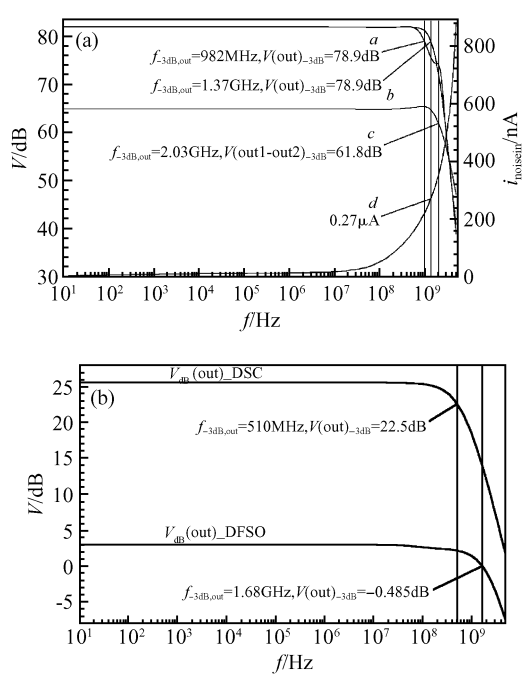

Fig. 4　Simulated characteristics　(a) Frequency response and noise characteristics of the optical receiver; (b) Frequency response of the DFSO

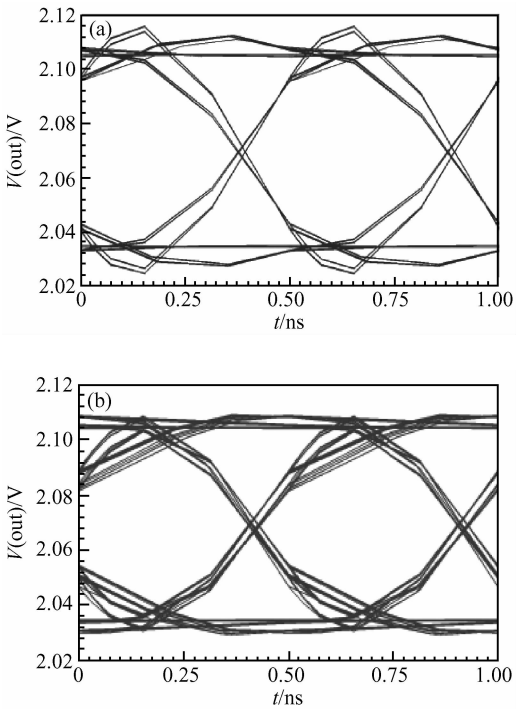

Fig. 5 Simulated eye diagrams under a $2^{15}-1$ PRBS input signal (a) 2Gb/s without parasitic inductors; (b) 2Gb/s with parasitic inductors

model library. Figure 4(a) is the corresponding frequency response and noise characteristic of the receiver shown in Fig. 3. Curves *a* and *b* are the characteristics of the output voltage V(out) versus frequency with bonding wires and without bonding wires, respectively. Curves *c* and *d* are the characteristics of the differential voltage V(out1)-V(out2) versus frequency with bonding wires and the total equivalent input integral noise current, respectively. A 1.37GHz −3dB frequency and a 81.9dBΩ transimpedance gain are achieved. Comparing curve *a* with *b*, the parasitic inductors of bonding wires contribute to a several hundred megahertz reduction in the −3dB frequency. Curve *c* indicates that a 2GHz bandwidth could be obtained if the −3dB frequencies of the LMA and the DFSO are enhanced to about 10GHz, meaning that smaller gate length processes should be applied. In addition, curve *d* demonstrates that the total equivalent input integral noise current of the chip is about 0.27μA from zero to −3dB frequency, and a −13dBm sensitivity can be achieved under the limitation of a 10^{-12} bit error rate for 60μm × 30μm fingered p^+/n-well/p-substrate photodiodes, the responsivity of which is about 0.0378A/W[7] (the calculation of optical sensitivity is described in Ref. [9]).

Generally, the bandwidth of a typical DSC (differential to single-ended conversion) is only several hundred megahertz because of its high output resistance. To extend the bandwidth, a new DFSO is designed, shown in Fig. 3, where two pMOS diodes are added in parallel with the two pMOS loads to reduce the output resistance greatly. Figure 4(b) is the simulated frequency response of the DFSO and the corresponding conventional DSC without pMOS diodes. The bandwidth has been greatly improved, from 510MHz to 1.68GHz.

Figures 5(a) and 5(b) are simulated output eye diagrams under a $2^{15}-1$ PRBS input signal, where the intensity of the photodiode's photogenerated current is assumed to be 3μA (the experiment photogenerated current of a 40μm × 40μm fingered p^+/n-well/p-substrate photodiode under a −11dBm or 79.4μW incident optic power is 3μA[7]). The figures show that the output voltage signal amplitude is about 90mV, and the receiver can achieve at least a 2Gb/s data rate.

3.3 Chip layout

Figure 6 is the entire chip layout of the receiver, shown in Fig. 3, in the Chartered 0.35μm standard analog CMOS 2P4M, 3.3V process. The core area is about 0.198mm^2 and the total chip size with pads is about 1285μm × 303μm.

4 Conclusion

A novel high-bandwidth, high-sensitivity differential optical receiver is proposed, and a corresponding optoelectronic integrated receiver is also presented in a Chartered 0.35μm standard analog CMOS 2P4M, 3.3V process. In the receiver, two completely identical photodetectors are used to double the bandwidth and the sensitivity simultaneously. They are also integrated into a single layout cell to acquire incident light from the same fiber for cost reduction. In addition, a high-bandwidth differential to single-ended output buffer is also designed.

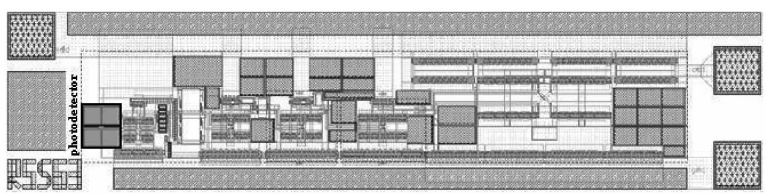

Fig. 6 Chip layout

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可应用于光互连的新型高带宽、高灵敏度差分光接收机的概念提出与设计*

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摘要： 提出了一种可应用于高速光通信和光互连的新型高带宽、高灵敏度差分光接收机. 其中，高带宽和高灵敏度分别通过输入负载平衡的全差分跨阻前置放大器和将入射光信号转换成一对差分光生电流信号的两个光电探测器来实现. 与常用光接收机相比，这种新型光接收机无任何附加成本. 设计了一种相应的、与 0.35μm 标准 CMOS 工艺完全兼容的光电集成接收机. 其中，光电探测器采用面积为 60μm×30μm、结电容为 1.483pF 的插指型 p^+/n-well/p-substrate 光电二极管. 仿真结果表明：该光电集成接收机的带宽为 1.37GHz；跨阻增益为 81.9dBΩ；面积为 0.198mm^2；数据传输率至少可达 2Gb/s；对于 $2^{15}-1$ 位的输入伪随机码序列(PRBS)，在误码率为 10^{-12} 条件下，灵敏度至少可达 −13dBm.

关键词： 高带宽；高灵敏度；CMOS；光接收机

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