Emerging Challenges in ESD Protection for RF ICs in CMOS*

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Abstract: On-chip electrostatic discharge (ESD) protection design has become an emerging challenge for radio-frequency (RF) integrated circuits (IC) design as IC technologies migrate into the very-deep-sub-micron (VDSM) regime and RF ICs move into multi-GHz operations. The key problem originates from the complex interaction between the ESD protection circuitry and the core RF IC circuit under protection. This paper discusses the recent development in RF ESD protection research and design, outlining emerging challenges, new design methods, and novel RF ESD protection solutions.

Key words: electrostatic discharge; ESD protection; RF ESD; parasitic
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1 Introduction

As IC technologies continuously migrate into the VDSM regime, RF IC design benefits significantly from the advance in IC technologies and circuit design techniques, reflected by improvement in key RF circuit parameters, such as cut-off frequency, maximum oscillation frequency, minimum noise figure, and linearity, etc. Unfortunately, ESD protection design does not benefit from the advance in CMOS IC technologies accordingly and ESD protection design emerges as a grand new challenge to mixed-signal and RF IC designs, particularly as RF IC operation quickly moves into the multi-GHz domain. It hence draws significant attention and research and development effort for advanced RF ESD protection solutions[1~12]. The key problems in RF ESD protection circuit design include properly defining the uniqueness of the RF ESD protection and accurately understanding the complex interactions between the ESD protection circuitry and the core RF IC circuit being protected[4]. In principle, RF ICs, typically used in wireless handheld devices, demand robust ESD protection because such devices are more prone to ESD-induced damages. The general principle for RF ESD protection remains the same, which is to provide a low-impedance current shunting path to discharge ESD transients without generating too much heat and to clamp the pad voltage to a sufficiently low level to avoid any dielectric rupture to CMOS[3]. Figure 1 illustrates typical snapback *I-V* characteristic for an ESD protection structure where critical parameters are given for triggering, holding, discharging, and thermal breakdown. However, it is important to realize that the RF ESD protection design has its unique features that are different from traditional IC ESD protection circuit design, where one of the key issues is associated with the complex interactions between the ESD protection circuitry and the core RF IC circuit, which is defined as the ESD-Circuit Interactions[4]. On one hand, any ESD protection structure, being an extra device to the IC core, will inevitably introduce parasitic effects to the core circuit that negatively affect the chip performance, a phenomenon defined as the ESD-to-Circuit Influence[4]. While digital ICs are typically insensitive to the ESD-induced parasitic effects, which are often ignored by IC designers in practice. However, such ESD-induced parasitics, including parasitic capacitance (C_{ESD}), resistance (R_{ESD}), noise coupling, and self-generated noises, etc, must be considered in

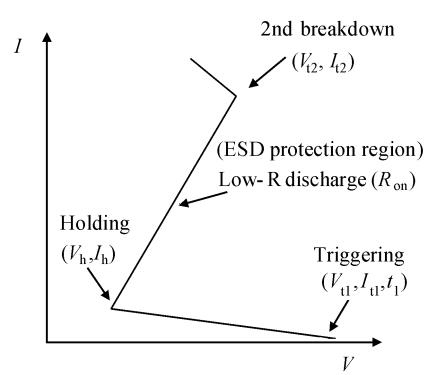

Fig. 1 Typical *I-V* curve for ESD protection

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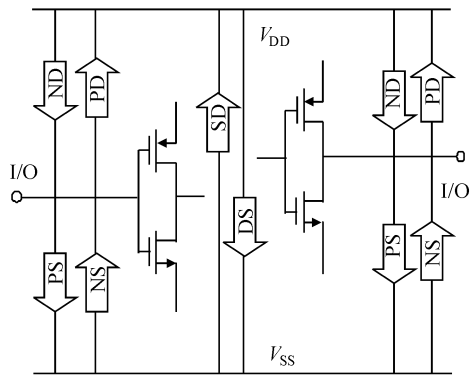

Fig. 2　Example full-chip ESD protection scheme using traditional one-direction ESD protection structures

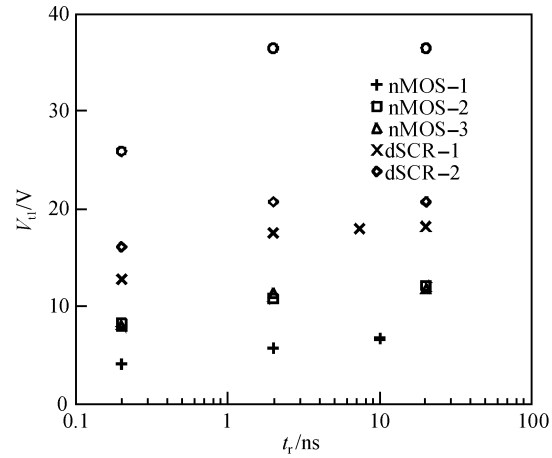

Fig. 3　V_{t1}-t_r curves for various ESD protection structures measured by TLP

RF IC design in order to avoid RF IC performance degradation due to ESD parasitic effects because RF ICs are extremely sensitive to any parasitic effect. The phenomena can be understood graphically by using Fig. 2, which illustrates a typical full-chip complete ESD protection scheme for a mixed-signal chip. Such a protection scheme uses a group of ESD protection structures at all I/O pads to protect against all ESD pulse modes, i. e., positive (PD) and negative (ND) to V_{DD}, and positive (PS) and negative (NS) to V_{SS}, as well as a number of power clamping devices for all supply lines to defend against possible ESD surges from V_{DD} to V_{SS} (DS) or vise verse (SD)[4]. While the total number of ESD structures on a chip varies for different ESD protection requirements and types of ESD structures used, the total count of ESD protection units needed for full-chip complete ESD protection can be very large, resulting in substantial overall ESD-induced parasitic effects. On the other hand, the IC circuits may adversely affect the ESD protection circuit, a phenomenon defined as the Circuit-to-ESD Influence[4]. For example, the normal RF signals are fast and strong, which may cause mis-triggering of an ESD protection structure, resulting in IC malfunction. Hence, RF ESD protection design must be considered at full chip level in order to ensure design success. This paper outlines various key aspects of RF ESD protection design.

2　ESD degradation

The Circuit-to-ESD Influence describes the phenomena that the protected IC circuit core may adversely affect the ESD protection structure, resulting in ESD protection performance degradation. In principle, an ESD protection device is a switch that remains OFF during normal circuit operation, but can be turned ON by an ESD surge and forms a low-impedance conducting path to discharge the large ESD transients[3]. Critically, an ESD protection structure must be insensitive to any desired signals and their reasonable fluctuation, while responding to any undesired ESD pulses efficiently and swiftly in order to provide ESD protection. However, the displacement currents originate with any significant variation in input voltage signal, dV/dt, and/or that in incoming current signal, dI/dt, may be coupled into the ESD devices through the parasitic capacitor and inductor, resulting in unwanted early turn-on of the ESD protection structures, which is defined as the mis-triggering of RF ESD protection structures[4]. The problem with the early triggering effect is that the ESD protection structure will be turned on by regular circuit signals, resulting in short-circuit and malfunction of the IC chip protected. This negative phenomenon can be understood from the following analysis. It was recently observed in TLP (transmission line pulsing) measurements of ESD protection structures that the triggering voltage, V_{t1}, of an ESD protection structure may be altered by the rise time, t_r, of a TLP pulse used in TLP tests. TLP test data show that triggering voltage decreases as the TLP pulse rise time decreases[4,13]. The triggering reduction effect is clearly shown in Fig. 3 for a group of different ESD protection structures, including grounded-gate nMOS (ggnMOS, labeled nMOS1-3) and dual-direction silicon-controlled rectifier (SCR, labeled dSCR1-3), that were tested by a TLP tester with varying pulse rise time from 200ps to 20ns, where a strong relation of V_{t1} on t_r is readily observed. The relationship of V_{t1} and t_r is attributed to the displacement current associated with the substantial dV/dt of the incoming waveform. Taking the ggnMOS ESD protection structure shown in Fig. 4 as an example, ESD protection works when an ESD pulse appears at the drain and causes the drain junction breakdown. The avalanche

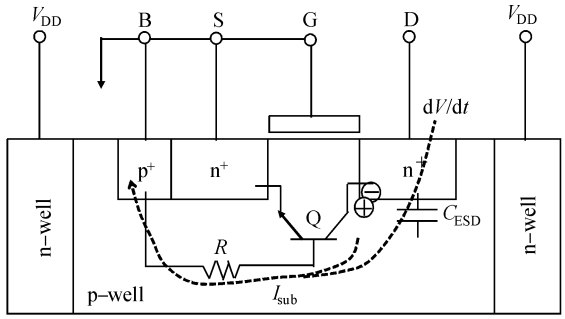

Fig. 4 ggnMOS ESD protection structure mechanism

current running through the p-well resistor will trigger the parasitic lateral pnp transistor, form a low-resistance conducting path, and then discharge. Apparently, the V_{t1} is directly controlled by the substrate current, I_{sub}. Hence, when unwanted dV/dt current across the drain junction capacitance (C_{ESD}) becomes significant, the displacement current, $i = C \times \frac{dV}{dt}$, will increase the I_{sub}, therefore accelerating the triggering process and reducing the V_{t1}. It is estimated that the required dV/dt threshold to turn-on the ggnMOS and SCR ESD protection structures ranges from 3×10^{10} to 1×10^{11} V/s[4], shown as solid markers in Fig. 5. Meanwhile, typical dV/dt values for a set of human body model (HBM) ESD zapping testers, real HBM ESD waveforms, and TLP testers are from 7×10^8 to 1×10^{11} V/s, shown in Fig. 5 as hollow markers[14]. These two groups of data are apparently at the same level, indicating that the dV/dt displacement does play a role in the V_{t1}-t_r relationship. We then consider some reported RF IC circuit examples, for which the dV/dt data are extracted as $\sim 2.5 \times 10^8$ V/s for a 2.5GHz CMOS clock recovery circuit[15], $\sim 4.3 \times 10^7$ V/s for a 1GHz CMOS clock synthesizer chip,[16] and $\sim 1.23 \times 10^7$ V/s caused by 7.1MHz digital clock noise coupling in a mixed-signal CMOS receiver chip[17]. Figure 5 shows that these dV/dt data for the practical RF ICs are still somewhat lower than the threshold dV/dt data needed to trigger an ESD protection structure for these examples. However, as the RF IC operation frequency becomes higher and their signal becomes stronger, as evident in the recent technology trends, it is inevitable that such a mis-triggering effect will become a big issue in multi-GHz RF IC design where the ESD protection structures can cause chip malfunction by regular RF or mixed signals. It is hence imperative to explore novel ESD protection triggering mechanisms that are insensitive to the dV/dt effect.

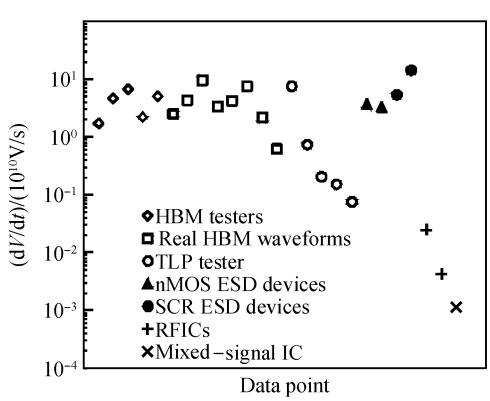

Fig. 5 dV/dt data comparison

3 RF circuit degradation

Since any ESD protection structure produces parasitics, it will inevitably affect circuit performance of the chip it protects. Such ESD-to-Circuit Influence effects include RC delay associated with the parasitic C_{ESD} and R_{ESD}, noise coupling between I/O and substrate due to C_{ESD}, ESD self-generated noises, and I/O impedance matching for RF ICs. All these ESD effects may substantially affect RF IC circuit performance, such as clock, signal integrity, RF impedance matching, power transfer efficiency, bandwidth, and noise figure, etc[4]. This section presents RF IC design examples to demonstrate the ESD-to-Circuit Influences. In this study, two RF building circuits were designed to include a 5GHz low noise amplifier (LNA) and a 5GHz mixer. The ESD protection used is an optimized ggnMOS structure with a width of 110μm targeting for a 2kV HBM ESD protection level. The ggnMOS ESD structure is minimized using a mixed-mode ESD simulation-design methodology so that the measured parasitic C_{ESD} is only 0.41pF. The designs were implemented in a commercial 0.35μm SiGe BiCMOS technology[1,18].

Figure 6 shows the schematic for the LNA circuit, a two-stage high-gain LNA featuring on-chip impedance matching, a power-down function, and a high/low gain control. Its design specifications are: power supply voltage V_{CC} = 3V, power consumption P_{supply} = 19.8mW, center frequency = 5GHz, Gain = 24dB, noise figure NF = 2.88dB, and 3rd-order input intercept point IIP_3 = −10.6dBm. The ggnMOS ESD protection structure is connected at the input pad. The same LNA circuits without and with ESD protection were characterized with the critical circuit parameters listed in Table 1. All key LNA circuit specifications, e.g., gain (S_{21}), NF, reflection ratio (S_{11}), and bandwidth (BW_{-3dB}), are affected by the ggnMOS ESD protection structure substantially even though the ESD protection structure was optimized for minimum parasitic effect by mixed-mode simulation in design.

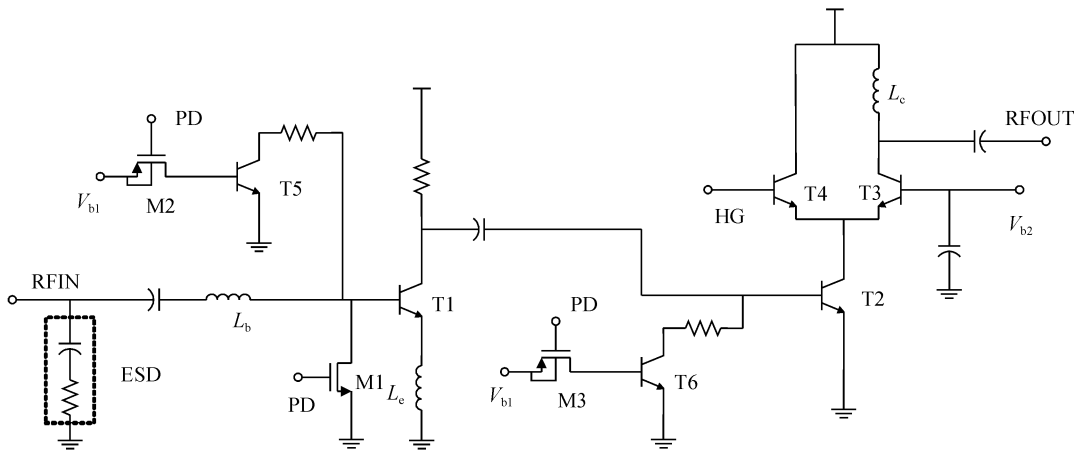

Fig. 6　A 5GHz LNA circuit with ggNMOS ESD protection studied

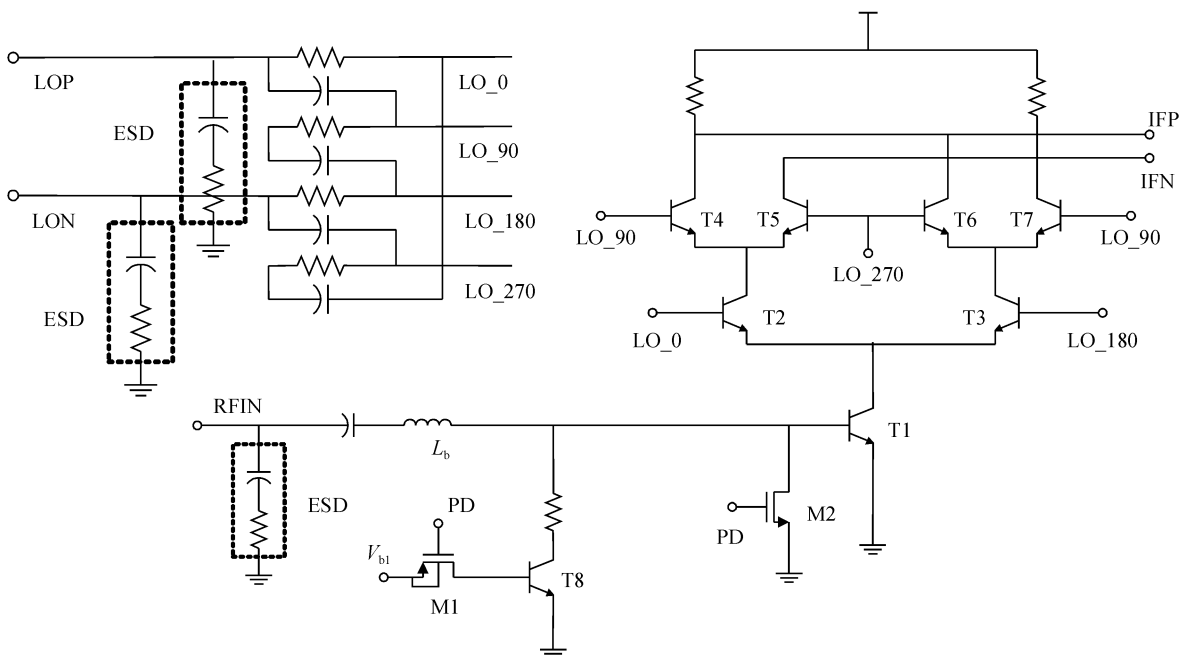

Fig. 7　A 5GHz mixer circuit with ggNMOS ESD protection studied

Table 1　LNA circuit comparison

Specs	S_{21}/dB	S_{11}/dB	NF/dB	BW_{-3dB}/GHz
No ESD	24.25	−12	2.88	4.18～6.38
ggnMOS ESD	22.4	−7.5	4.28	4～6

Table 2　Mixer circuit comparison

Specs	Conversion gain /dB	S_{11}/dB	NF/dB
No ESD	2.16	−3.7	11
ggnMOS ESD	1.76	−3	12.35

Figure 7 shows the 5GHz sub-harmonic direct down-conversion mixer with on-chip matching, featuring RF = 5.25GHz, local oscillation frequency LO = 2.6GHz, intermediate frequency IF = 50MHz, V_{cc} = 3V, P_{supply} = 10.8mW, gain = 2.16dB, and NF = 11dB. The ggnMOS ESD protection structures are connected to both RF and LO ports. The mixer circuits without and with the ESD protection structures were characterized with typical specifications listed in Table 2, which clearly shows that all the key circuit parameters, including gain, noise figure, and S_{11}, are significantly affected by the ESD protection structures as expected.

The above examples demonstrate that even using an optimized RF ESD protection structure with minimum parasitic parameters, RF circuits may be substantially affected by the ESD-induced parasitic effects in practical designs. Therefore, such ESD-to-Circuit Influence must be carefully considered in practical RF IC design.

Table 3 RF ESD protection guidelines

Key factors	Comment
Triggering	Immune to normal RF signals
Low parasitics	Reduce ESD-to-circuit influences
Compact	Reduce parasitic; Be layout friendly
Robustness	Higher RF ESD protection level
Constant C_{ESD}	Stable performance across bandwidth
Flexible V_{t1}	Meet specifications at different pads
Multiple-mode	Reduce count of ESD protection devices

4 RF ESD protection

RF ESD protection is a very challenging design problem. It is impractical to look for any all-fit RF ESD protection solution because RF ESD protection design is application-specific and strongly depends upon the RF IC circuits to be protected. In principle, any conventional ESD protection structure may be used for RF ESD protection as well, given that the ESD-circuit interactions are fully considered and minimized. Research on RF ESD protection is receiving more attention in the IC design field. Table 3 gives a list of key guidelines that should be considered in practical RF ESD protection circuit design.

This section presents some promising RF ESD protection solutions. In general, novel, low-parasitic, compact, and multiple-mode ESD protection structures are preferred for RF ESD protection. As an example, Figure 8 shows the cross-section of a novel three-terminal all-mode ESD protection structure that delivers a high ESD protection to area ratio of 80V/mm-width[19]. The main advantage of this structure is that it guarantees an active low-impedance discharging path formed by an SCR-type device between any two terminals in both directions. As a result, only one such all-mode ESD protection device is needed at each I/O pad to provide complete ESD protection, as shown in Fig. 9, compared to using up to four traditional uni-direction ESD protection devices, as illustrated in Fig. 2[20]. This protection scheme requires fewer and smaller ESD protection devices per chip, hence minimizing total ESD-induced parasitic on a chip. It is generally believed that the popular MOSFET type ESD protection structure is not a suitable RF ESD protection solution due to its large size and strong parasitic effect. Recently, a diode string has been considered as an attractive RF ESD protection solution due to its low total parasitic C_{ESD} in its series connection[7]. Certainly, one has to minimize diode dynamic resistance by designing proper sizes in order to ensure that the increase in voltage drop over the diode string does not cause the voltage clamping problem under large ESD currents. Meanwhile, the Darlington application may increase the leakage in such diode-string ESD protection solutions, which must be considered in designs[3]. Stacked diodes in polysilicon were reported to reduce the C_{ESD} and to suppress the Darlington effect; however, its poor heat dissipation may be a practical problem[6]. Furthermore, in using

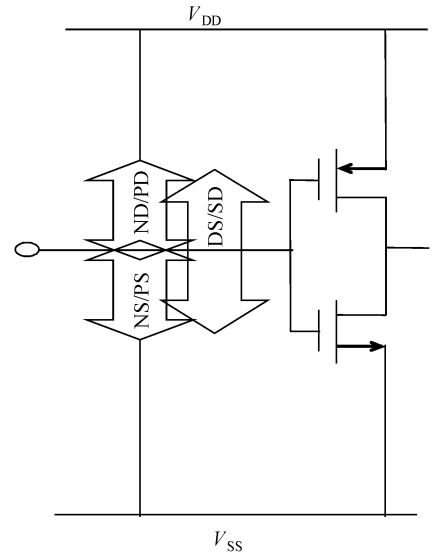

Fig. 9 ESD protection scheme using all-mode ESD protection structure

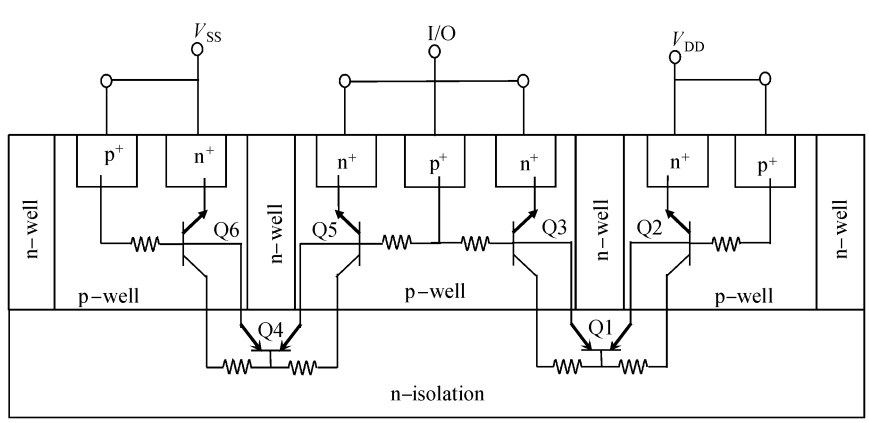

Fig. 8 Cross-section for a three-terminal all-mode SCR-type ESD protection structure

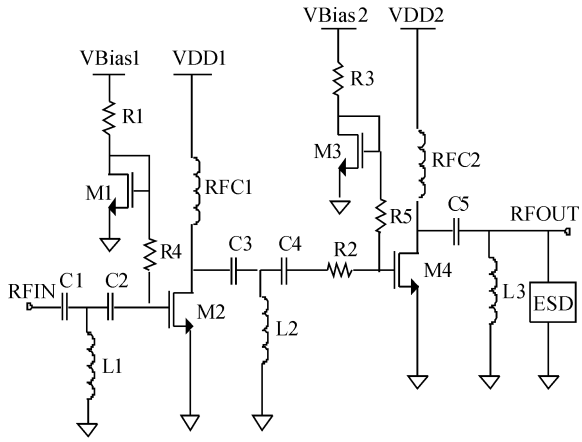

Fig. 10　2.4GHz PA with output matching of C5 & L3, inter-stage matching of C3, C4 & L2, and ESD protection at output

diode strings, other types of parasitic C_{ESD}, e.g., metal interconnects, might increase as more diodes are stacked up. Considering the conflicts in designing diode strings, one has to consider the overall ESD protection performance in practical design[4]. Recently, there have been several designs reported to address the RF impedance mis-matching problem, including using a bonding wire inductor or an LC tank to ensure impedance matching and using transmission line coil networks to realize broadband ESD protection[10~12]. In fact, a new design method is desirable that can integrate RF IC design and ESD protection design in the same phase in order to optimize the ESD-protected RF IC chip design. Such a new ESD-RF co-design method was recently reported, which achieves excellent whole-chip design optimization for an RF power amplifier (PA) circuit[21]. Figure 10 shows the reported 2.4GHz ESD-protected PA circuit featuring 5kV ESD protection using a diode structure designed in a commercial 0.18μm CMOS technology with its die photo shown in Fig. 11. In this study, the 5kV ESD diode was optimized for minimum parasitic C_{ESD}.

However, the optimized ESD protection structure still affects the PA circuit performance due to the I/O impedance mis-matching. The new ESD-RF co-design method allows the inclusion of the parasitic effects into the PA circuit simulation by using a direct s-parameter insertion technique. Thus, the I/O impedance corruption can be eliminated by re-matching design. Table 4 shows the PA gain comparison for the CMOS PA circuit under different conditions. The ESD parasitic effect degrades PA gain performance substantially due to ESD-induced I/O mis-matching, while such performance degradation can be almost recovered by using the new ESD-RF co-design method.

Table 4　S_{21} of 2.4GHz PA

	No ESD	5kV ESD	5kV ESD REM
Gain	26.9	26.7	26.9

Layout is very critical to ESD protection design because ESD protection structures are usually large and make full chip layout difficult. Hence, novel ESD protection layout designs can be very beneficial for full chip design. Figure 12 shows one novel pad-oriented all-mode ESD protection design that is layout-friendly[22]. In addition, a well-thought-out full chip RF ESD protection scheme is highly preferred in RF ESD protection design. Figure 13 illustrates a whole-chip RF ESD protection solution using dual-direction ESD protection structures[23], where a low-R, active SCR-type ESD discharging path is created between any two pads. Compared with an ESD protection scheme using traditional uni-direction ESD devices, as shown in Fig. 2, the total number of ESD protection devices per chip is greatly reduced using this scheme, resulting in much lower overall ESD-induced parasitic on chips. Use of a common ESD discharging bus can also help to reduce the number of ESD devices needed on a chip[3]. Recently, Xie *et al*.[24] reported a new low-parasitic polysilicon SCR ESD protection structure that achieved a very low reported parasitic C_{ESD}

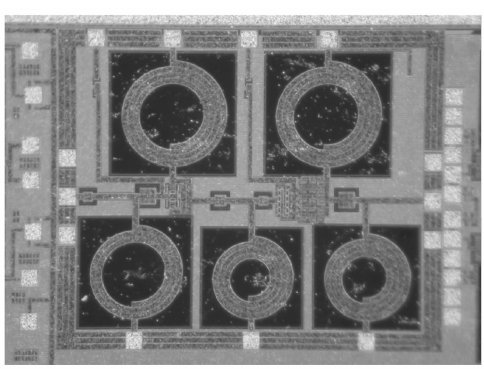

Fig. 11　Die photo of the PA in CMOS

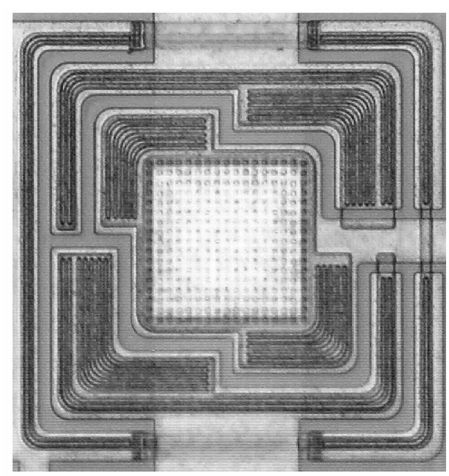

Fig. 12　Die photo of a pad-oriented all-mode ESD protection structure

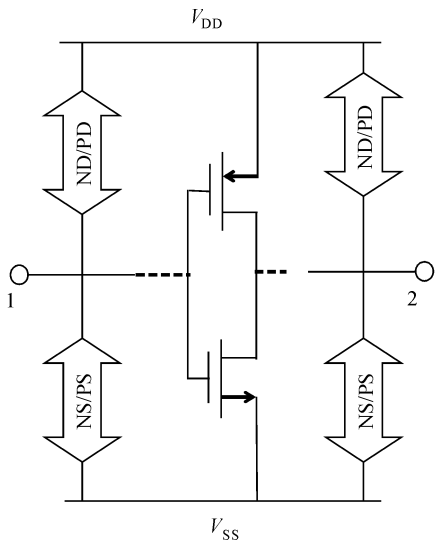

Fig. 13 Full-chip ESD protection scheme using dual-direction ESD protection

of ~92.3fF for a 3.2kV ESD protection level, as shown in Fig. 14. In brief, while there are many good RF ESD protection designs reported, more research and development efforts are expected to explore novel RF ESD protection solutions that address the unique RF ESD protection problem.

5 RF ESD protection evaluation

Due to the significant ESD-to-Circuit influences, thoroughly characterizing any RF ESD protection design is imperative to ensure design success. One new RF ESD evaluation method is to characterize its *S*-parameters, using a series or parallel C_{ESD}-R_{ESD} network[4], from which the parasitic C_{ESD} and R_{ESD} can be extracted and used for ESD-RF co-design[21]. In *S*-parameter measurement, a co-planar GSG (ground-source-ground) RF test pattern is required and a de-embedding dummy test pattern is also needed to ensure measurement accuracy. The following example depicts the *S*-parameter characterization procedure where a group of commonly used ESD protection structures were investigated, including ggnMOS, diode

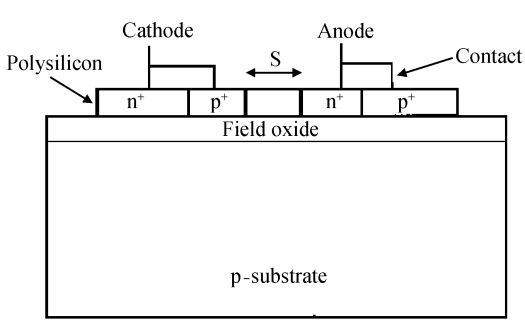

Fig. 14 Cross-section for an SCR ESD protection structure in polysilicon in CMOS

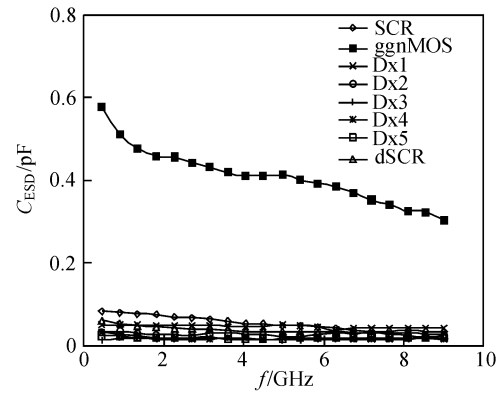

Fig. 15 Measured C_{ESD} for 2kV ESD protection structures including ggnMOS

strings using n^+/pwell diodes, SCR, and a dual-direction SCR structure (dSCR)[4]. The diode strings consist of 1, 2, 3, 4, and 5 diodes (i.e., Dx1, Dx2, Dx3, Dx4, & Dx5). All ESD protection structures were designed and fabricated in commercial 0.35μm BiCMOS technology. For comparison, all ESD protection structures were designed for a 2kV HBM[25] ESD protection level. Figures 15 and 16 show the measured total parasitic ESD capacitances, C_{ESD}, in a 10GHz spectrum for all the ESD protection structures studied. The ggnMOS has the highest C_{ESD} due to its large size. For the diode strings, the total C_{ESD} of diode strings decreases in general as the number of diodes in the diode strings increases; however, it does not follow the trend of $C_{ESDtotal} = C_{junction}/n$. The reason is that the total measured C_{ESD} includes extra parasitic capacitances in addition to its junction capacitance. Hence, the reduction in total C_{ESD} is not governed by the above formula. Furthermore, the measured data show that the C_{ESD} reduction trend saturates as the number of diodes increases to more than three in a diode string. Considering that increasing the number of diodes in a diode string will result in a linear increase in the total Si area consumed, a two or three-diode string seems to be an optimal RF ESD protection solution

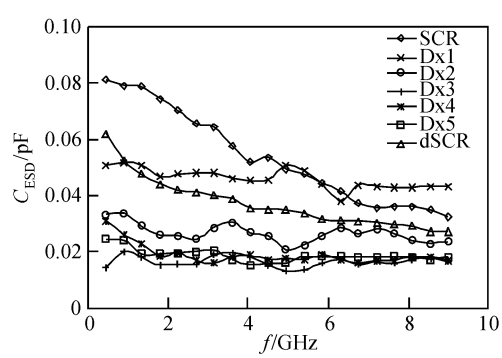

Fig. 16 Measured C_{ESD} for 2kV ESD protection structures without ggnMOS

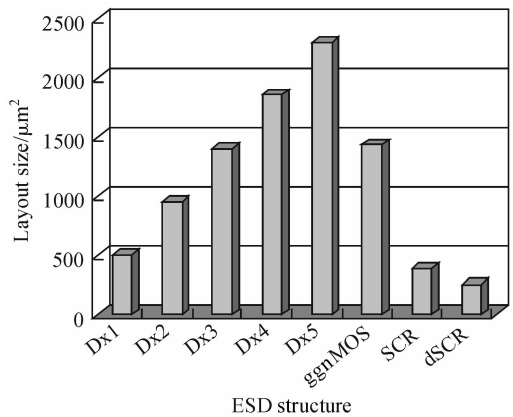

Fig. 17　Layout size comparison for various 2kV ESD protection structures

for an RF ESD protection design with optimized overall specifications, including parasitic C_{ESD} and total size. In addition, the dSCR is a favorable RF ESD protection structure because of its low C_{ESD}. For overall performance of the RF ESD protection structures, it is important to consider other factors, such as the layout sizes, in addition to the C_{ESD}. Figure 17 shows the sizes of different ESD protection structures, which indicates that neither ggnMOS nor very large diode strings are good candidates for RF ESD protection structures. SCR ESD protection structures typically enjoy a small size. To better characterize the overall ESD performance of various RF ESD protection structures, a new figure-of-merit parameter, called the F-factor, defined as $F = \dfrac{V}{\text{Size} \times C_{ESD} \times \text{NF}}$, was proposed in Ref. [4], where V is the ESD protection voltage level in volts and NF is the noise figure. Clearly, a large F value is preferred for a better RF ESD protection structure. Figure 18 shows the measured F-factor data, which indicates that the dSCR is the best RF ESD protection design and a 2/3-diode string can also be an attractive solution. In addition to

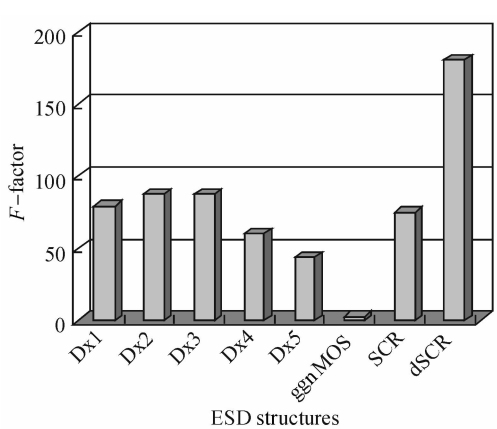

Fig. 18　F-factor comparison for various 2kV ESD protection structures

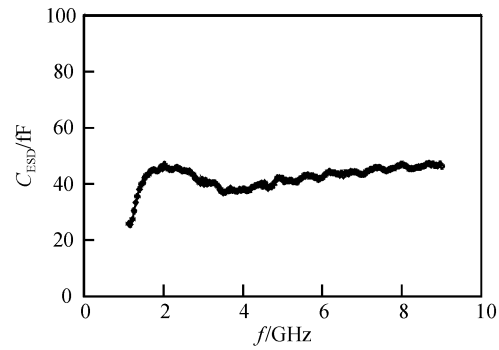

Fig. 19　Measured parasitic C_{ESD} for a 5kV n-well diode ESD protection in 0.13μm CMOS

S-parameter characterization, noise behavior should be evaluated as well by characterizing the noise figure of an RF ESD protection structure. This new RF ESD characterization method was further confirmed recently by a series of ESD protection designs implemented in commercial 0.13μm RF CMOS technology. Figure 19 shows the measured parasitic C_{ESD}-f curve across a 10GHz spectrum for a 5kV+ diode ESD protection structure that is optimized for a very low C_{ESD} of less than 50fF. From these observations, a new RF-ESD co-design method that integrates measured ESD-parasitics into RF IC circuit simulation was developed recently, which makes it possible to realize full chip RF IC design optimization, including ESD protection[21].

6　Summary

This paper reviews various key aspects in RF ESD protection circuit design, including unique challenges, ESD-circuit interactions, possible RF ESD solutions, and RF ESD characterization. It discusses the importance of integrating ESD protection parameters into RF IC chip design to achieve whole-chip RF IC optimization. Practical design examples are presented to argue the new RF ESD protection design techniques.

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CMOS 射频集成电路 ESD 保护的挑战*

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摘要: 随着集成电路(IC)工艺进入深亚微米水平,以及射频(Radio-Frequency, RF)IC 工作频率向数千兆赫兹频段迈进,片上防静电泄放(ESD)保护设计越来越成为 RF IC 设计的挑战.产生这一挑战的关键原因在于 ESD 保护电路和被保护的 RF IC 核电路之间存在着不可避免的复杂交互影响效应.本文讨论了 RF ESD 保护的研究和设计领域的最新动态,总结了所出现的新挑战、新的设计方法和最新的 RF ESD 保护解决方案.

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