GaAs PIN Diodes for X-Band Low Loss and High Isolation Switches*

Wu Rufei†, Zhang Haiying, Yin Junjian, Zhang Jian, Liu Huidong, and Liu Xunchun

(*Institute of Microelectronics, Chinese Academy of Sciences, Beijing* 100029, *China*)

Abstract: GaAs PIN diodes optimized for X-band low loss and high isolation switch application are presented. The impact of diode physical characteristics and electrical parameters on switch performance is discussed. A new structure for GaAs PIN diodes is proposed and the fabrication process is described. GaAs PIN diodes with an on-state resistance of $<2.2\Omega$ and off-state capacitance <20fF in the range of 100MHz to 12.1GHz are obtained.

Key words: GaAs PIN diodes; low-loss; high-isolation; switch
PACC: 3220D; 7280E **EEACC**: 1350H; 2520D; 2570
CLC number: TN315$^+$.3 **Document code**: A **Article ID**: 0253-4177(2008)05-0832-04

1 Introduction

Monolithic microwave integrated circuit (MMIC) switches are widely used in millimeter-wave communication systems as a result of recent progress in MMIC technology[1,2]. For such applications, switches need low insertion loss and high isolation. GaAs PIN diodes are generally considered as candidates for such MMIC switches because of their high power-handling capability, low on-state resistance, and high switching cutoff frequencies. A vertical epitaxial structure is commonly used in GaAs PIN diodes[3] since they can provide lower RF impedance under forward bias than planar ion-implanted PIN structures[4]. The disadvantage is the generation of parasitic MIM capacitors.

In this paper, the characteristics of the GaAs PIN diodes are analyzed and the impact of diode parameters on switch performance is discussed. Based on physical analysis, a new GaAs PIN diode structure is proposed and the fabrication process is presented. The measurement showed $C_{\rm off}<20$fF at -10V reverse bias and $R_{\rm on}<2.2\Omega$ at $+10$mA forward bias.

2 Design of GaAs PIN diodes

To obtain insight into the influence of the PIN diode parameters on the switch performance, a SPST switch with a single GaAs PIN diode in a shunt configuration is investigated. The shunt configuration minimizes the through insertion loss and maximizes the isolation. Figure 1 shows the schematic of SPST switches with a bias network.

The maximum-achievable isolation and the minimum-achievable insertion loss of the investigated switch are given in Eqs. (2) and (3)[5]:

$$\text{Isolation(SPST}-\text{1diode)} = 20\lg\left[1+\frac{Z_0}{2R_{\rm on}}\right] \quad (2)$$

$$\text{Insertion(SPST}-\text{1diode)} = 10\lg[1+(\pi f C_{\rm off} Z_0)^2] \quad (3)$$

where Z_0 is the characteristic impedance of the transmission line, $R_{\rm on}$ is the diode on-state resistance, and $C_{\rm off}$ is the diode off-state capacitance. Equation (2) indicates the isolation of the SPST switch will improve by reducing the diode on-state resistance. A small $R_{\rm on}$ is crucial for minimizing the voltage drop across the PIN diode, thus improving the signal isolation of the switch. Equation (3) shows that the insertion loss depends primarily on the off-state capacitance. A small $C_{\rm off}$ can effectively reduce the signal leakage through the reversely biased diode.

A commonly used device structure, proposed by Takasu[3], is shown in Fig. 2. When the diode is forward biased, the diode impedance is small because the

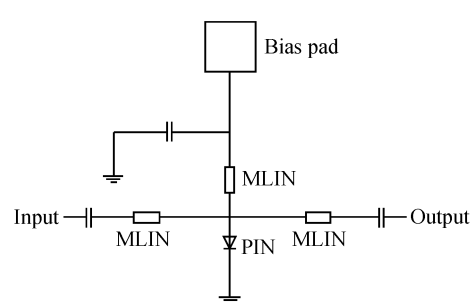

Fig. 1 Topology of single pole single throw switch

* Project supposed by the National Natural Science Foundation of China (No. 10002909) and the State Key Development Program for Basic Research of China (No. G2002CB311901)
† Corresponding author. Email: rfwu04@mails.gucas.ac.cn
Received 21 November 2007, revised manuscript received 19 December 2007

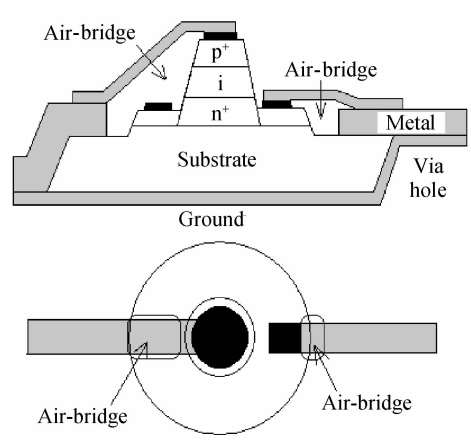

Fig. 2　GaAs PIN diode structure proposed by Takasu

i-layer is filled with carriers and the depletion capacitance is very large. When reversely biased, the i-layer is depleted of carriers and the impedance is very high. The depletion capacitance becomes smaller as the depletion width increases. Differences in high-frequency impedance of the diode between the on- and off-states lead to its application in MMIC switches.

To maximize switch isolation, a small R_{on} is preferred. The total small-signal on-state resistance R_{on} of the diode is composed of the resistance of the i-layer, resistance of the n^+- and p^+- layers, and parasitic contact resistance. The resistance of the i-layer is negligible due to conductivity modulation effect[6]. R_{on} is dominated by the resistance of the n^+- and p^+-layers. To minimize the value of R_{on}, p^+- and n^+-layer should be highly doped. Meanwhile, proper contact metal should be chosen to minimize contact resistance.

To minimize switch insertion loss, diodes with small C_{off} are necessary to prevent signal leakage through the off-state diode. The total small-signal off-state capacitance C_{off} is composed of the depletion capacitance and parasitic capacitance. When i-layer thickness increases, the depletion width increases and off-state capacitance decreases, which results in significant improvement in insertion loss. However, unintentional doping of the i-layer limits the maximum depletion width to about 1μm for given off-state bias and prevents further improvement of the insertion loss for thicker i-layers.

Therefore, in order to obtain a low-loss and high-isolation switch, GaAs PIN diodes should be designed with small size, a thick i-layer, and highly doped n^+- and p^+-layers.

The diode structure is another important design consideration. In the structure proposed by Takasu, the n^+-layer is circular. An air-bridge is important to eliminate the parasitic MIM capacitor. Since the p^+- and i-layer step can be as high as 10μm (for high power-handling capability applications), it is difficult to fabricate an air-bridge to cover the step. To overcome this issue, a new structure for GaAs PIN diodes is proposed, as shown in Fig. 3. Here, the n^+-layer is designed to be semicircular instead of circular. Thus, no parasitic MIM capacitor will be generated.

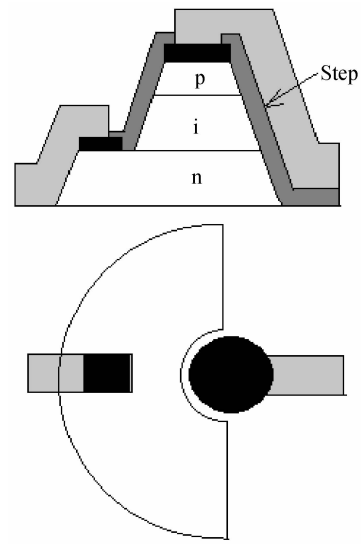

Fig. 3　Cross-section and platform of new structure of GaAs PIN diodes

3　Fabrication of GaAs PIN diodes

The cross section and platform of the GaAs PIN diode are shown in Fig. 3. The diodes were manufactured on a molecular beam epitaxy (MBE) grown material. The p^+- and n^+-layer were highly doped with a concentration of $1\times10^{18}\sim5\times10^{19}\,cm^{-3}$ (gradually increasing) and $3\times10^{18}\,cm^{-3}$ to minimize the on-state resistance. To maximize the off-state capacitance, diodes with different n+-layer radii and i-layer widths were implemented and the optimum values were found to be 12μm and 3μm, respectively. The diodes were fabricated on circular mesas using wet etching with $H_3PO_4:H_2O_2:H_2O=2:3:30$ solution. P-type metal contacts made of Pt/Ti/Au were deposited on the p^+-layer. Ni/Ge/Au/Ge/Ni/Au contacts were then deposited on the n^+-layer. Both contacts were annealed at 375℃ for 1min. Diodes were passivated with 0.5μm Si_3N_4. Electroplating was used to implement the electrode down-leads instead of evaporation since the evaporation is anisotropic and cannot cover p^+- and i-layer steps tightly, whereas the electroplating is isotropic.

4　Results

The de-embedded *ABCD*-parameter of the on-

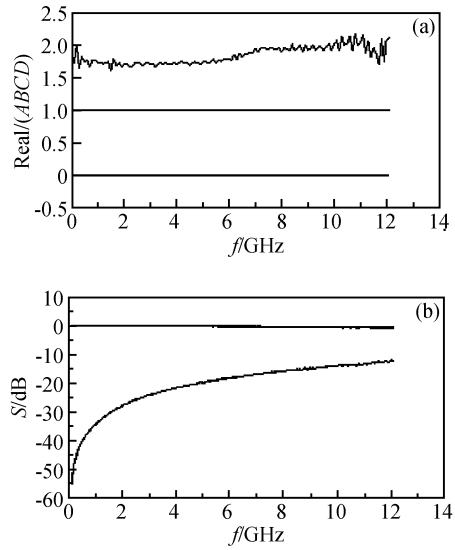

Fig. 4 Small signal parameter of GaAs PIN diodes (a) On-state *ABCD*-parameter; (b) Off-state *S*-parameter

state and the *S*-parameter of the off-state are shown in Fig. 4. From the on-state *ABCD*-parameter, the on-state resistance R_{on}, which is frequency dependent, has a maximum value of 2.2Ω at +10mA forward bias from 0.1 to 12.1GHz. R_{on} could be further reduced by improving the p^+- and n^+-layer doping concentration. To calculate the off-state capacitance, the *S*-parameter is transformed to an *ABCD*-parameter and Eq. (3) is then applied. C_{off} is found to be less than 20fF at −10V reverse bias from 100MHz to 12.1GHz, as shown in Fig. 5. DC characterization of the diodes demonstrated turn-on voltage V_{on} = 1.1V and reverse breakdown voltage V_b = −78V, respectively. The diode cut-off frequency, which is a commonly used figure of merit, is about 3.6THz by Eq. (4). The low on-state resistance and low off-state capacitance together with the high cut-off frequency of the GaAs PIN diode validates its feasibility on high frequency high performance MMIC switch applications. The comparison between this work and previous research in terms of on-state resistance, off-state capacitance, bias condition, p^+-layer area, and i-layer width is summarized in Table 1.

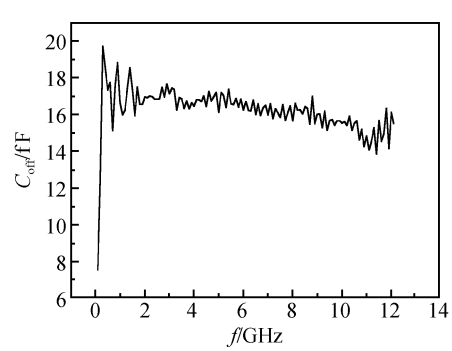

Fig. 5 Off-state capacitance versus frequency

Table 1 Comparison of the diode performance between this work and previous research

	R_{on} /Ω	C_{off} /fF	I_{on} /mA	V_{off} /V	Area /μm²	i-layer width/μm
This work	2.2	20	10	−10	452	3
Ref.[7]	1.5	65	30	−5	1962	3
Ref.[8]	1.6	32	10	0	615	NA
Ref.[9]	2.2	30	10	0	2122	2
Ref.[10]	3.7	27	5	−10	113	2
Ref.[11]	5	35	30	0	NA	1.2
Ref.[12]	5	20	NA	NA	36	1

$$C_{off} = \frac{1}{\omega \times \mathrm{imag}(ABCD(1,2))} \tag{3}$$

$$f_c = \frac{1}{2\pi R_{on} C_{off}} \tag{4}$$

5 Conclusion

A new structure for GaAs PIN diodes was proposed for X-band low-loss and high-isolation MMIC switches. The fabrication process was then described. The low on-state resistance, low off-state capacitance, and high cut-off frequency of the GaAs PIN diode validates its feasibility on high frequency high performance MMIC switch applications.

Acknowledgements GaAs PIN diode material was offered by the Institute of Physics, Chinese Academy of Sciences. Device measurement was supported by Ouyang Sihua and Li Yankui.

References

[1] Colquhoum A, Schmidt L P. MMICs for automotive and traffic applications. GaAs IC Symposium, 1992: 3

[2] Takagi T, Yamauchi K, Itoh Y, et al. MMIC development for millimeter-wave space application. IEEE Trans Microw Theory Tech, 2001, 49(11): 2073

[3] Takasu H. Estimation of equivalent circuit parameters for a millimeter-wave GaAs PIN diode switch. IEEE Proc Circuits Devices Syst, 2003, 150(2): 92

[4] Tayrani R, Bartle D C, Barrett N J. GaAs surface oriented microwave PIN diodes. Proc IEEE GaAs Integrated Circuit Symp, 1974: 85

[5] Chorney P. Multi-octave and multi-throw, PIN diode switches. Microwave Journal, 1974, 17(9): 39

[6] Baliga B J. Tower semiconductor devices. PWS Publishing Company, 1996: 155

[7] Bellantoni J V, Bartle D C, Payne D, et al. Monolithic GaAs p-i-n diode switch circuits for high-power millimeter-wave applications. IEEE Trans Microw Theory Tech, 1989, 37(12): 2162

[8] Putanam J, Barter M, Wood K, et al. A Monolithic GaAs PIN switch network for a 77 GHz automotive collision warning radar. IEEE Radio Frequency Integrated Circuits Symposium, 1997: 225

[9] Buber T, Kinayman N, Yun Y H, et al. Low-loss high-isolation 60−80GHz GaAs SPST PIN switch. IEEE MTT-S Digest, 2003: 1307

[10] Kobayashi K W, Tran L, Oki A K, et al. A 50MHz-30GHz broad-

band co-planar waveguide SPDT PIN diode switch with 45-dB Isolation. IEEE Microw Guided Wave Lett, 1995, 5(2): 56

[11] Pritchett S D, Seymour D. A monolithic 2－20GHz GaAs PIN diode SP16T switch. IEEE MTT-S Digest, 1989: 1109

[12] Case M, Matloubian M, Sun H C, et al. High-performance W-band GaAs PIN diode single-pole triple-throw switch CPW MMIC. IEEE MTT-S Digest, 1997: 1047

X 波段低损耗高隔离开关应用的 GaAs PIN 二极管*

吴茹菲†　张海英　尹军舰　张　健　刘会东　刘训春

（中国科学院微电子研究所，北京　100029）

摘要：报道了一种适用于 X 波段的低损耗高隔离度开关的 GaAs PIN 二极管. 讨论了 GaAs PIN 二极管的物理特性和主要电学参数对开关性能的影响，并且介绍了工艺制备过程. 测试结果表明在 100MHz～12.1GHz 范围内，正向电流为 10mA 时的开关电阻小于 2.2Ω，而反向电压为－10V 时开关电容小于 20fF.

关键词：GaAs PIN 二极管；低损耗；高隔离；开关

PACC：3220D；7280E　　**EEACC**：1350H；2520D；2570a

中图分类号：TN315+.3　　**文献标识码**：A　　**文章编号**：0253-4177(2008)05-0832-04

* 国家自然科学基金（批准号：10002909）和国家重点基础研究发展规划（批准号：G2002CB311901）资助项目

† 通信作者. Email：rfwu04@mails.gucas.ac.cn

2007-11-21 收到，2007-12-19 定稿