Missing Via Mechanism and Solutions

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Abstract: Missing via has been a defect in semiconductor manufacturing, especially of foundries. Its solution can be rather attractive in yield improvement for relatively mature technology since each percentage point improvement will mean significant profit margin enhancement. However, the root cause for the missing via defect is not easy to determine since many factors, such as, defocus, material re-deposition, and inadequate development, can lead to missing via defects. Therefore, knowing the exact cause for each defect type is the key. In this paper, we will present the analysis methodology used in our company. In the experiments, we have observed three types of missing vias. The first type consists of large areas, usually circular, of missing patterns, which are primarily located near the wafer edge. The second type consists of isolated sites with single partially opened vias or completely unopened vias. The third type consists of relatively small circular areas, within which the entire via pattern is missing. We have first tried the optimization of the developing recipe and found that the first type of missing via can be largely removed through the tuning of the rinse process, which improves the cleaning efficiency of the developing residue. However, this method does not remove missing via of the second and third type. We found that the second type of missing via is related to local defocus caused by topographical distribution. To resolve the third type of missing via defects, we have performed extensive experiments with different types of developer nozzles and different types of photomasks, and the result is that we have not found any distinct dependence of the defect density on either the nozzle or the mask types. Moreover, we have also studied the defect density from three resists with different resolution capability and found a correlation between the defect density and the resist resolution. It seems that, in general, lower resolution resists also have lower defect density. The results will be presented in the paper.

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1 Introduction

Via defects are an annoying issue in semiconductor manufacturing. They affect device performance and chip yield, causing profit loss. In the foundry business, since the size of the customer's order may be very small, the defect reduction is especially important to maintain sizable income. Missing via is a serious defect in BEOL layers. It exhibits itself as missing holes during optical inspection, the normal method[1~3]. To improve optical contrast, such defect detection is usually done after etch and barrier metal deposition. Therefore, any missing via defect found during the defect scan may be potentially caused by both photo, dry etch, chemical mechanical polishing (CMP), and thin film processes. As a result, finding the root cause for missing via may be quite difficult. In this paper, we will present our work on the classification of the missing via defect found in our photo processes and our methodology in the solution of it. First, we will classify the defects according to their appearances. Second, we will describe the experiments we designed for finding the root causes for various different missing via defects. Finally, we will present our study of the three common types of defects in lithography.

2 Classification of missing via defects

Although the optical detection method is widely used for the characterization of defects, an expectation of complete detection is not practical because not all defects have strong optical signatures. Another method is electronic testing (ET) with special test structures, such as via chains. Although this method can give a good estimate as to the density of the defects, its capability is still limited because the test is either carried out at a couple of layers behind or it needs test masks and short loop wafers. Therefore, a good strategy is to use the optical method to help find the root causes of the defects and re-optimize the process recipe to remove them. As the related process modules in via process are thin film, lithography, etch and CMP, we have done cross checking experiments with the help from other process modules to identify the origin of defects. These experiments indicate that most defects can be put into the following categories: chamber particles, small unknown circular defects in

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film deposition, big circular defects at the wafer's edge, single missing via in dense via area, and small circular defects in lithography. There are also chamber particles from the etch process. The images of typical defects are displayed in Figs. 1～3.

2.1　Thin film process induced missing via defects (scanned after film deposition)

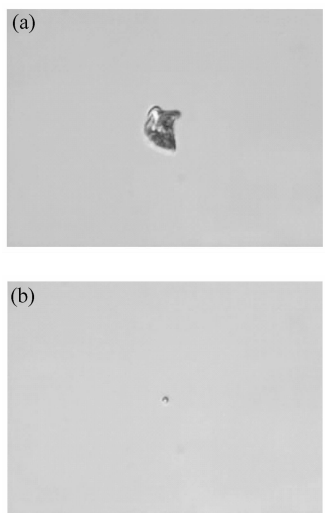

Fig. 1　Classical defects in thin film process　(a) Big particle in film deposition chamber; (b) Small unknown circular defects

2.2　Lithographic process induced missing via defects (scanned after develop)

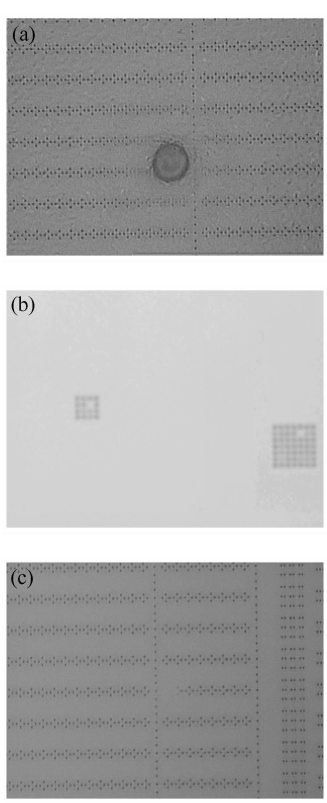

Fig. 2　Classical missing via defects found in lithographic process　(a) Big circular defect at the wafer's edge; (b) Single via missing in dense via area; (c) Small circular defect

2.3　Dry etch process induced missing via defects (scanned after resist strip and wet cleaning)

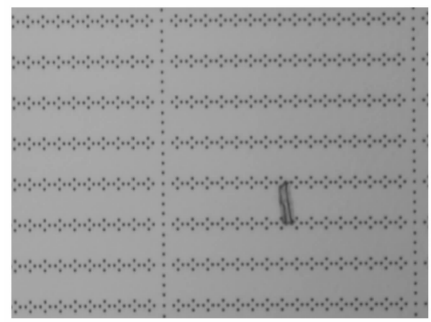

Fig. 3　Classical etch process induced missing via defects; chamber particle in etch

The chamber particle defects in thin film and etch processes described in the figures above can be mostly removed by chamber cleaning during the periodical maintenance in daily operation. The small, relatively unknown, circular defect in film deposition usually is not a threat to yield and electronic performance. Therefore, we conclude that the efforts need to be focused on the analysis and solution of the missing via defects found in the photolithography process.

3　Root cause and solutions for defects in photolithography

In this section, we will demonstrate the root cause and the solutions for defects in the lithographic module, i. e., missing vias. We will also show that these defects are related to process recipe and resist characteristics.

We begin with the first type of missing via defect: the big circular defect found at the wafer's edge. During the optical inspection, as shown in Fig. 2, within the center of the circular defect, there is a core-like region with obvious color variation. Color variation within a thin film, such as inter-metal dielectric (IMD) or the photoresist or BARC, means thickness variation of the thin films and produces interference patterns. Such a "core" can possibly be related to the particles in the developer cup or particles generated by an inadequate development process[4,5]. But the fact that the particles in a developer cup are usually found randomly throughout the wafer indicates that the particle, which is detected at the edge of the wafer, is related to the development process. Inadequate development may be caused by an un-optimized development process, or by an inefficient removal process for the material produced by the development process. We therefore refined the development process, including the optimization of the prew-

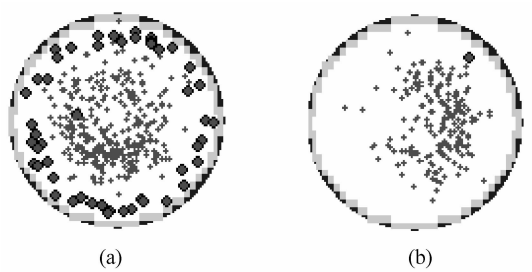

Fig. 4 Defect map with original development recipe and refined development recipe (Big circular defects located at wafer edge is removed by refined develop recipe) (a) Original recipe; (b) Newly refined recipe

et, the spin acceleration/speed, the puddle method, and the optimization of the rinse time. The before and after scans are displayed in contrast in Fig. 4, which shows that most of the edge located defects are removed.

Compared to the first type of missing via defect, instead of being found at the wafer's edge and with a rather large optical signature, the second type of missing via defects are found in a limited area, or a "point-like" area, shown in Fig. 2(b). The image of contacts or vias in photolithography usually has a relatively small depth of focus, around 300nm. At back-end-of-the-line (BEOL) of the process, due to the presence of wafer topography variation, this effect can be rather obvious. One topography variation is contributed by the CMP process, which can produce up to 100nm in film thickness variation for each IMD layer. After several layers, such topographic variation can be comparable to the total depth of focus for the via photo process. To confirm whether this type defect is caused by de-focus due to wafer topography, we experimented on bare wafer with different focus conditions. We found that the defect count grows very quickly when the wafer moves away from focus. Described in Fig. 5 are three defect scans with each wafer at the best focus, best focus $+0.1\mu$m, and best focus $+0.2\mu$m positions, respectively. The defect count grows quickly from 0 and 1 for the first two focus settings (up to 0.1μm away from the best focus) to 14 just 0.2μm away from best focus condition (Table 1).

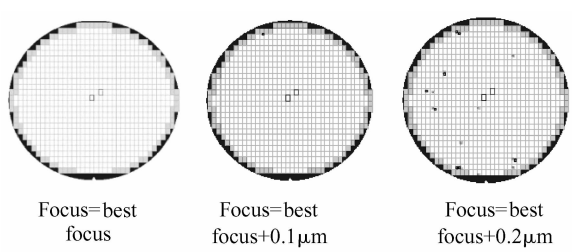

Fig. 5 Defect account growth with serious de-focus Big circular defects located at wafer edge are removed by refined development recipe.

Table 1 Defect account growth as a function of de-focus

Focus/μm	Best focus	Best focus + 0.1	Best focus + 0.2
Defect account	0	1	14

Since the field curvature for typical exposure tools can be as much as 200 to 300nm over the entire exposure field, these type of missing via defects can be quite common.

The third type of small circular defect, shown in Fig. 2(c), is more difficult to remove. Its distribution on the wafer is usually random and its appearance is always related to certain types of photoresists. We have performed experiments by changing the illumination conditions, mask types (binary and attenuated phase shifting), and the development condition (nozzle types and developing recipes). However, we found that its density is not sensitive to the imaging or development condition. Its insensitivity to the exposure resolution, shot size and shot distribution, and pattern density indicates that it is not related to the imaging process. The fact that it does not depend on mask types[6] further indicates that it is not related to the optical imaging quality. Although it appears to be related to the development process, its insensitivity to the various developing recipes, as we have described in the previous section, suggests that it may be related to the resist material design. Therefore, either the designed dissolution reaction may be inadequate for the material removal, or the chemical species produced during the developing process may be hard to remove.

We have tried several other resists with different resolution and we noticed these resists usually have a relatively high resolution. The resists (resist 1, 2, and 3) we have experimented with have different lithography performances and defect performances. The relative defect performances of these resists are demonstrated in Fig. 6. A more detailed process performance is shown in Table 2. We found that resist 3, which has relatively lower resolution, has the lowest defect count among the three. Therefore, to completely solve missing via defects, we will need to work with the resist makers.

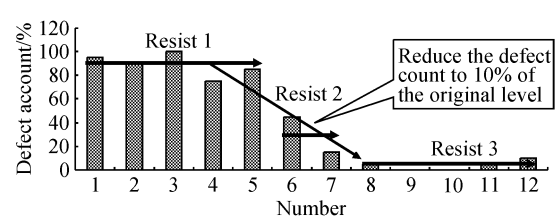

Fig. 6 Defect count of the third type missing via defect for three photoresists The defect count with resist 3 has been reduced to 10% of the original level with resist 1.

Table 2　Process window performance of three kinds of photo resists

	Resist 1	Resist 2	Resist 3
DoF (CD @ 0.18μm)/μm	0.6	0.5	0.45
EL/%	35.40	30.00	27.50
MEEF	2.6	2.8	3.2

4 Conclusion

We analyzed and categorized three types of missing via defects found in our process. Among these defects, we demonstrated three types of missing via defects in the photolithographic process. The first type, big circular defects around the wafer's edge, is caused by an un-optimized development process. The second type, single via missing in dense via areas, is caused by local de-focus due to wafer topography introduced by other processes, such as CMP in BEOL layers. The third type, small circular defects, is caused by some photoresists. Through the use of an optimized development recipe and good resists, we have demonstrated that we can reduce all types of missing via defects significantly. To solve the missing via issue completely, we will need to work with resist makers for the optimization of resist chemistry.

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对通孔消失机理的研究以及相应的解决方案

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摘要： 通孔消失是困扰半导体生产的难点之一.它与产品的生产合格率息息相关,正因为如此这一问题一直摆在业界工程师面前.由于这一问题的成因较多,故在分析和解决问题上存在诸多困扰.本文实验并分析了多种通孔消失的实效模型,结合先进的缺陷测试手段对其给出了不同的解决方案.此外,对相应的光刻胶也进行了研究并将缺陷密度与光刻胶的分辨率相联系,通过研究发现较低的分辨率的光刻胶的缺陷密度也相应较低.

关键词： 通孔消失；缺陷；良率提升；光刻胶；光刻技术

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