# An Adaptive-Bandwidth CMOS PLL with Low Jitter and a Wide Tuning Range

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**Abstract**: This paper presents a novel adaptive-bandwidth charge pump PLL with low jitter and a wide tuning range. With an adaptive bandwidth, the proposed PLL can scale its loop dynamics proportional to the output frequency and maintain optimal performance over its entire output range. In order to improve the jitter performance of the PLL, a matching technique is employed in the charge pump, and a voltage-to-voltage converter is used to achieve a low gain VCO. The experimental chip was fabricated in a 0.35$\mu$m CMOS process. The measured results show that the PLL has perfect jitter performance within its operating range from 200MHz to 1.1GHz.

**Key words**: PLL; adaptive bandwidth; low jitter; wide tuning range
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## 1 Introduction

A challenge in designing phase locked loops (PLLs) is providing ample flexibility for a variety of applications in ASICs. The diversity of ASIC applications has led to various requirements for PLLs' operating frequencies. Due to their fixed bandwidth, conventional PLLs can not provide diversiform operating frequencies with high quality[1]. However, adaptive-bandwidth PLLs can solve this problem by adjusting for different output frequencies. They achieve an adaptive bandwidth proportional to the reference frequency and a constant damping factor independent of the process, voltage, and temperature variation. Thus, adaptive-bandwidth PLLs can sustain optimal jitter performance over the entire operating range.

Several techniques for adaptive-bandwidth PLLs have been developed[2~4]. However, complicated filter structures, such as active filters and current model filters, were used in those designs. In this paper, a novel adaptive-bandwidth charge pump PLL (CPPLL) is presented. This proposed PLL achieves an adaptive bandwidth and a constant damping factor with a simple passive filter structure and a smaller chip area. Jitter is another critical performance that must be considered in the design of PLLs. In this proposed circuit, a matching technique and a voltage-to-voltage converter are applied to the charge pump and VCO circuit, respectively, to improve the jitter performance.

## 2 Structure and operation principles

A structural overview of the proposed adaptive-bandwidth CPPLL is shown in Fig. 1. The CPPLL consists of a phase frequency detector (PFD), two charge pumps (CP1 and CP2), a passive filter, a gain compensation VCO, and a feedback divider. The passive filter includes a diode-connected nMOS MR, which is used as a resistor. The gain compensation VCO is composed of a voltage-to-voltage converter and a conventional VCO.

The charge/discharge current of charge pump CP1 and CP2 are $I_{CP1} = I_{CP}$ and $I_{CP2} = GI_{CP}$ ($G$ is a constant). Assuming that the resistance of the diode-connected nMOS is $R$, as shown in Fig. 1, the relationship between $V_C$ and $I_{CP}$ is

$$F(s) = \frac{V_C}{I_{CP}} = \frac{1 + sRC'_1}{sC_1(1 + sRC_2)} \tag{1}$$

In this circuit, $C'_1 = (1 + G)C_1 + C_2$ and $C_2$ is much smaller than $(1 + G)C_1$, so $C'_1 \approx (1 + G)C_1$.

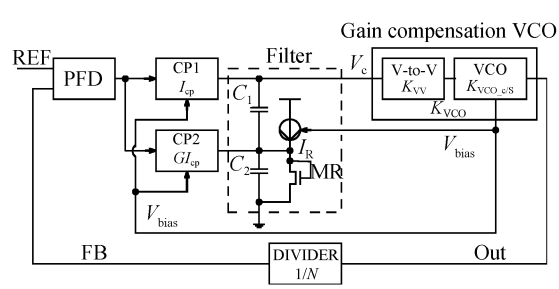


Fig. 1 Structure of the proposed CPPLL

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The gain of the PFD and CP ($K_{PFD}$) is proportional to the charge/discharge current of the charge pump. The gain compensation VCO has a gain of $K_{VCO}$. $1/N$ is the gain of the frequency divider. Consequently, the open loop transfer function of the proposed PLL is

$$H_o(s) = \frac{I_{CP}K_{VCO}(1 + sRC'_1)}{2\pi NC_1 s^2(1 + sRC_2)} \quad (2)$$

This expression is similar to the open loop gain of a conventional 3rd CPPLL with a classic 2nd passive filter[5]. $\omega_n$ and the damping factor $\zeta$ of this CPPLL can be approximately calculated by following equations.

$$\omega_n = \sqrt{\frac{I_{CP}K_{VCO}}{2\pi NC_1}} \quad (3)$$

$$\zeta = \frac{1}{2}RC'_1\omega_n \approx \frac{1}{2}R(1 + G)C_1\omega_n \quad (4)$$

$\zeta$ is equal to $\frac{1}{2}RC\omega_n$ in a conventional 3rd CPPLL. Thus, with the same $R$ and $\omega_n$, the filter capacitance in the proposed circuit is $1/(1 + G)$ of that in the conventional CPPLL. The filter capacitance can be reduced further by increasing the value of $G$.

As shown in Fig. 1, the MOS diode, charge pumps, and VCO use the same biasing voltage $V_{bias}$. Thus, the biasing current of the MOS diode ($I_R$) and charge pumps ($I_{CP}$) are both proportional to the biasing current of VCO ($I_{VCO}$), that is, $I_R \propto I_{CP} \propto I_{VCO}$. The resistance of the diode-connected nMOS $M_R$ is

$$R = \frac{1}{G_m} \propto \frac{1}{\sqrt{I_R}} \propto \frac{1}{\sqrt{I_{VCO}}} \quad (5)$$

In the proposed circuit, the biasing current $I_{VCO}$ and the operating frequency $\omega_{VCO}$ have the relationship[6]

$$\omega_{VCO} \propto \sqrt{I_{VCO}} \quad (6)$$

Therefore, we have the following relationship in this PLL.

$$\frac{\omega_n}{\omega_{VCO}} \propto \frac{\sqrt{I_{CP}}}{\sqrt{I_{VCO}}} \propto \frac{\sqrt{I_{VCO}}}{\sqrt{I_{VCO}}} = \text{constant} \quad (7)$$

$$\zeta \propto \frac{1}{\sqrt{I_R}} \times \sqrt{I_{CP}} \propto \frac{1}{\sqrt{I_{VCO}}} \times \sqrt{I_{VCO}} = \text{constant} \quad (8)$$

Figure 2 shows the simulation results of the relationship between the voltage $V_c$ and the response of

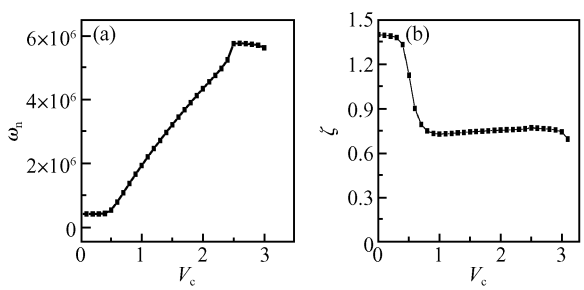



Fig. 2　Dynamic response of the proposed PLL　(a) $\omega_n$ versus $V_c$; (b) $\zeta$ versus $V_c$

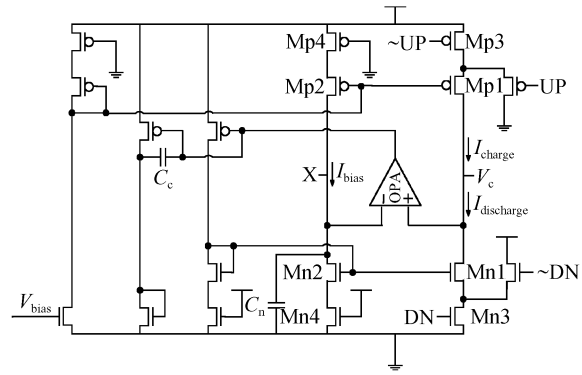



Fig. 3　Schematic of charge pump

the PLL. Since the operating frequency is proportional to $V_c$, the simulation results demonstrate that the proposed PLL has a loop bandwidth proportional to the operating frequency and a constant damping factor over its operating range, as described in Eqs. (7) and (8).

## 3　Circuit design

### 3.1　Charge pump

The charge pump circuit is shown in Fig. 3. $C_n$ and compensation capacitor $C_c$ stabilize the feedback loop. With an error amplifier and the negative feedback loop, the voltage at node X follows the voltage $V_c$ as long as the gain of the amplifier is high enough. Therefore, the voltage $V_c$ is equal to the voltage at node X. In this charge pump, Mp1 = Mp2, Mp3 = Mp4, Mn1 = Mn2, and Mn3 = Mn4. So, $I_{charge} = I_{bias}$ when the UP signal is high and $I_{discharge} = I_{bias}$ when the DN signal is high, making $I_{charge} = I_{diacharge}$ regardless of the voltage $V_c$. Hence, the charge and discharge current match well and the performance of the PLL is improved. Figure 4 is the simulation result of charge and discharge current of the charge pump when the voltage $V_c$ sweeps from 0 to 3.3V. As the simulation result shows, the mismatch of the charge pump is less than 1‰ within the valid operating range.

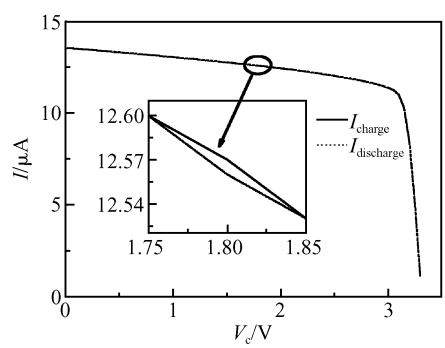



Fig. 4　Charge pump current matching characteristic

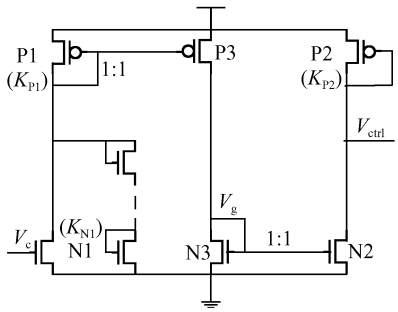



Fig. 5 Voltage-to-voltage converter

### 3.2 Voltage-to-voltage converter

Figure 5 is the circuit of the voltage-to-voltage converter. The nMOSs in series produce a biasing current when the input voltage $V_c$ is lower than $V_{THn}$. When all transistors work in saturation, $I_{P2} = I_{N1}$ and the output voltage $V_{ctrl}$ is

$$V_{ctrl} = -\sqrt{\frac{K_{N1}}{K_{P2}}} \times V_c + V_{DD} - |V_{THp}| + \sqrt{\frac{K_{N1}}{K_{P2}}} \times V_{THn} \tag{9}$$

So, the output voltage has linear characteristic against the input. The gain can be changed by adjusting the value of $K_{N1}/K_{P2}$, which is determined by $(W/L)_{N1}/(W/L)_{P2}$. To make sure N1 and N2 are in saturation, the input voltage $V_c$ has a maximum $V_{INMAX}$ of

$$V_{INMAX} = \frac{V_{DD} - |V_{THp}|}{1 + \sqrt{K_{N1}/K_{P1}}} + V_{THn} \tag{10}$$

The output voltage has a minimum $V_{OUTMIN} = V_g - V_{THn}$.

### 3.3 Gain compensation VCO

As shown in Fig. 1, we use a voltage-to-voltage converter and a VCO to compose the gain compensation VCO. In order to improve the jitter performance, it is important to achieve a low gain VCO[7]. In the same output frequency range, enlarging the valid input range helps reduce the VCO gain. In this proposed CPPLL, the input range of the conventional VCO is much smaller than the output range of the charge pump. From Eq. (9), a large input range can be linearly scaled down to a smaller output range by a voltage-to-voltage converter. Therefore, we add a voltage-to-voltage converter in front of the conventional VCO to enlarge the valid input range.

With the help of the voltage-to-voltage converter, the gain compensation VCO has the same output range as the conventional VCO but a larger input range. The gain of the gain compensation VCO is

$$K_{VCO} = K_{VV} K_{VCO\_C} \tag{11}$$

where $K_{VCO\_C}$ is the gain of the conventional VCO and $K_{VV}$ is the gain of the voltage-to-voltage converter. Since $K_{VV}$ is less than 1, the gain compensation VCO has a lower gain than the conventional VCO

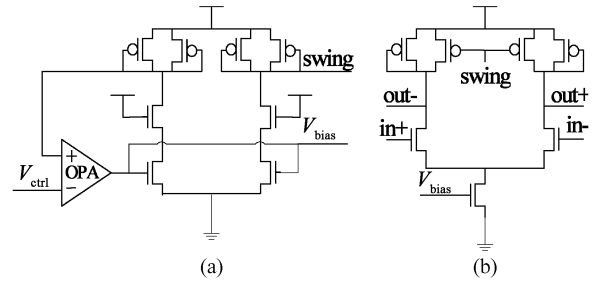



Fig. 6 (a) VCO bias circuit; (b) VCO delay cell

The conventional VCO delay cell with symmetric loads[6] is shown in Fig. 6(b). The biasing voltages of the VCO are generated by the circuit in Fig. 6(a).

## 4 Measured results

The described PLL circuit was fabricated with an SMIC 0.35$\mu$m CMOS process. Figure 7 shows the layout of the PLL circuit, including pads.

The chip was measured by the Agilent 93k SOC test system. Because of the bandwidth limitation of the measurement instruments, we did not measure the output signal directly. We denote the output signal of divided by $N$ ($N = 32$) as FB, which is shown in Fig. 1. To achieve measurement accuracy, we measured the FB signal instead.

The measured results show that the PLL works well from 200MHz to 1.1GHz. Figure 8(a) is the output waveform of FB at 31.25MHz, corresponding to the output signal at 1GHz. As illustrated in Fig. 8(b), the measured lock time of the proposed PLL is about 2$\mu$s when the input frequency changes from 10 to 20MHz. This corresponds to the output signal from 320 to 640MHz, which is about 36% of the tuning range.

A performance summary of this work is listed in Table 1. The jitter was measured by TIA (DTS1000) embedded in the 93k test system. These jitter measurements are not de-embedded and the cascaded dividers are adopted in the design, so the measured jitter

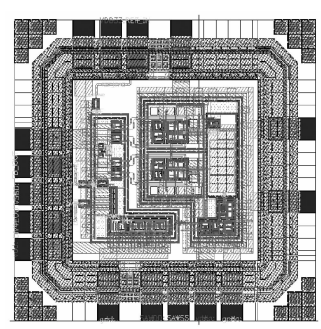
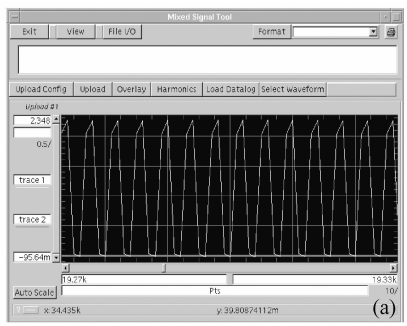


Fig. 7 Layout of the proposed PLL



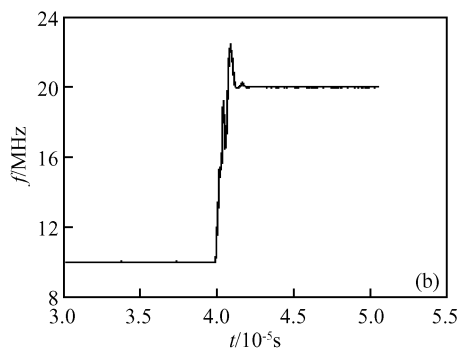




Fig. 8　(a) Output waveform of FB at 31.25MHz; (b) Acquisition process as input frequency changes from 10 to 20MHz

of the FB signal contains the jitter contribution from the Agilent 93k oscilloscope and the frequency dividers. In fact, the jitter of the output signal is less than the measured jitter of the FB signal. The performance comparison is shown in Table 2, and the performance of the proposed PLL can be further improved with advanced processes.

Table 1　Performance summary

| | | |
|---|---|---|
| Process | 0.35$\mu$m CMOS | |
| Chip area | 580$\mu$m× 620$\mu$m | |
| Supply voltage | 3.0～3.6V | |
| Power consumption | 22mW@ $f_{OUT}$ = 1GHz | |
| Operating range($f_{VCO}$) | 200M～1.1GHz | |
| Jitter performance (FB signal) | Frequency/MHz | RMS jitter/mean period |
| | 10 | ＜0.08% |
| | 15 | ＜0.05% |
| | 20 | ＜0.04% |
| | 25 | ＜0.03% |
| | 30 | ＜0.04% |

Table 2　Performance comparison

| | This work | Reference [3] |
|---|---|---|
| Process | 0.35$\mu$m CMOS | 0.15$\mu$m CMOS |
| Operating range | 200M～1.1GHz | 250M～2GHz |
| Output RMS jitter / mean period | ＜1.28% @ 1.1GHz* | 1.54% @ 1.2GHz |

* Calculated from the measured results

## 5　Summary

An adaptive-bandwidth PLL with a simple passive filter is described and analyzed in this paper. The jitter performance of the proposed PLL is improved by applying a matching technique and a voltage-to-voltage converter to the charge pump and VCO circuit, respectively. The measured results demonstrate that the adaptive-bandwidth CPPLL maintains optimal dynamic response and jitter performance in its wide operating range. Moreover, compared with the conventional CPPLL, the chip area of the filter capacitance can be scaled down in the proposed PLL.

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# 一种低抖动、宽调节范围的带宽自适应 CMOS 锁相环

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**摘要**：提出了一种低抖动、宽调节范围的带宽自适应 CMOS 锁相环.由于环路带宽可根据输入频率进行自动调节，电路性能可在整个工作频率范围内得到优化.为了进一步提高电路的抖动特性，在电荷泵电路中采用匹配技术，并在压控振荡器中应用电压-电压转换电路以减小压控振荡器的增益.芯片采用 SMIC 0.35$\mu$m CMOS 工艺加工.测试结果表明该锁相环电路可在 200MHz～1.1GHz 的输出频率范围内保持良好的抖动性能.

**关键词**：锁相环；自适应带宽；低抖动；宽调节范围

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