Multiplexer Design Applied to High-Speed Signal Transmission*

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Abstract: A multiplexer with a low-distortion high-bandwidth analog switch is presented. The gate-to-source voltage of the switch is set by the combined on-voltage of a pMOS and an nMOS, and the difference between its gate-source voltage and the threshold voltage (V_{GST}) is guaranteed to be constant with input variation. Thus, the body effect is nearly canceled. Implemented in a TSMC 0.18μm CMOS process, results from HSPICE simulation show that the V_{GST} is nearly constant with an input range from 0.3 to 1.7V, and the −3dB bandwidth is larger than 10GHz; the SFDR (spurious free dynamic range) of the output is 67.11dB with 1GHz input frequency; the turn-on time is 2.98ns, and the turn-off time is 1.35ns, which indicates a break-before-make action of the multiplexer. The proposed structure can be applied to high speed signal transmission.

Key words: low-distortion; high speed; multiplexer; analog switch
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1 Introduction

In high speed signal transmission and multi-channel analog-to-digital converter (ADC) systems, the design of high-linearity low-distortion input switches and multiplexers is critical because variation in the on-resistance (R_{on}) can introduce distortion. This variation can be easily demonstrated by the on-resistance of a simple MOS-only switch which can be written as:

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_G - V_{in} - V_{th})} \quad (1)$$

where V_G is the gate-voltage of the switch, V_{in} is the input voltage, and V_{th} is the threshold-voltage and is given as $V_{th} = V_{t0} + \gamma(\sqrt{2|\phi_F| + V_{SB}} - \sqrt{2|\phi_F|})$. Equation (1) shows that the on-resistance is dependent on the input. On the other hand, the −3dB bandwidth is also limited by R_{on} with load capacitance C_{hold} constant, and is:

$$f_{-3dB} = \frac{1}{2\pi R_{on} C_{hold}} \quad (2)$$

From the above analysis, the main limitation of the MOS-only switch is the non-linearity of R_{on} and its limitation on the input bandwidth. In order to solve these problems, a CMOS switch and a boostrap switch are used. However, despite improvements in the linearization of R_{on} in a CMOS switch, the corresponding nonlinearities in n- and p-transistors are not matched and substantial variation in R_{on} still occurs. Boostrap switches can make the gate-source voltage constant, but have body effects. References [1~3] presented some solutions. The main idea of Ref. [1] is to make the well connect to the source when the switch is on, but there is parasitic capacitance with the well. Other solutions may limit the input bandwidth or increase the complexity of the design.

In this paper, a low-distortion high-bandwidth analog switch is presented and is applied to a 2∶1 multiplexer, not only making the difference of gate-source voltage and the threshold voltage (V_{GST}) constant and achieving a significantly higher linearity, but also achieving feasibility for high-speed signal transmission and meeting the requirement of break-before-make action of the multiplexer.

2 Proposed constant V_{GST} switch

The proposed constant V_{GST} switch is shown in Fig. 1. The *I-V* relation of MOSFET operating in saturation is:

$$I = \frac{1}{2}\mu C_{ox} \frac{W}{L}(V_{gs} - V_{TH})^2 \quad (3)$$

Therefore,

$$V_{gs} = \sqrt{\frac{2I}{\mu C_{ox}(W/L)}} + V_{TH} \quad (4)$$

From Fig. 1, the following relation can be obtained:

$$V_{gs,N2} + V_{sg,P1} = V_{gs,N1} \quad (5)$$

Substituting Eq. (4) into Eq. (5), then:

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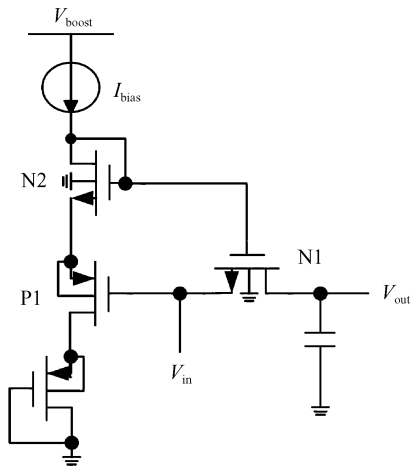

Fig. 1　Proposed constant V_{GST} switch

$$V_{gs,N1} = \sqrt{\frac{2I_{bias}}{\mu_n C_{ox}(W/L)_{N2}}} + V_{TH,N2} + \sqrt{\frac{2I_{bias}}{\mu_p C_{ox}(W/L)_{P1}}} + V_{TH,P1} \quad (6)$$

Therefore, the V_{GST} of switch N1 is:

$$V_{GST,N1} = \sqrt{\frac{2I_{bias}}{\mu_n C_{ox}(W/L)_{N2}}} + V_{TH,N2} - V_{TH,N1} + \sqrt{\frac{2I_{bias}}{\mu_p C_{ox}(W/L)_{P1}}} + V_{TH,P1} \quad (7)$$

The threshold voltage of N1 and N2 has the same variation with input, so the body effect of N1 and N2 can compensate each other, and P1 has no body effect because its well is tied to its source. Therefore, the proposed switch has a constant on-resistance and very low distortion.

3　Proposed multiplexer using proposed constant V_{GST} switch

Figure 2 is the proposed 2∶1 multiplexer. N1, N2, P1, P2, P6, P7, N9 and N20, N21, P19, P20, P16, P17, N19 form the circuit realization of a constant V_{GST} switch, respectively. The other part is used to determine which channel is selected; the Boost block is a boostrap circuit which makes the voltage of node ⑦ $2V_{dd}$, and has the same structure as Ref. [4]. The operation of the multiplexer is as follows: when clock CLK1 is low and CLK1N is high, the voltage of node ④ is boosted to be $2V_{dd}$ by MOS capacitor N10. Because the voltage of node ⑦ is also $2V_{dd}$, transistor P8 is off. At the same time, the voltage of node ② is low, and transistor N4 is on, making the voltage of node ⑥ low, the nMOS switch N2 off, and the input signal IN2 transmit to the output. On the contrary, when clock CLK1 is high and CLK1N is low, the voltage of node ④ is V_{dd} and transistor P8 is on, which makes the voltage of node ③ $2V_{dd}$. Then, P7 and N9 is on to provide bias current to transistor N1 and P1, turning switch N2 on and transmitting input signal IN1 to the output.

4　Simulation results

Based on a TSMC 0.18μm CMOS process, the circuit is simulated with HSPICE tools. Figure 3 shows the threshold voltage variation of transistor N1 and N2 with respect to the input signal level. The threshold voltage of transistor N1 changes in substantial unison with the threshold voltage of transistor N2, so the body effect of the two transistors remains the same to compensate each other. Figure 4 is the V_{GST} performance of the switch. With a 1.8V power supply, the V_{GST} changes from 0.83 to 0.64V with the input ranging between 0.3～1.7V, an improvement over Ref. [5] which has a V_{gs} variation of 200mV.

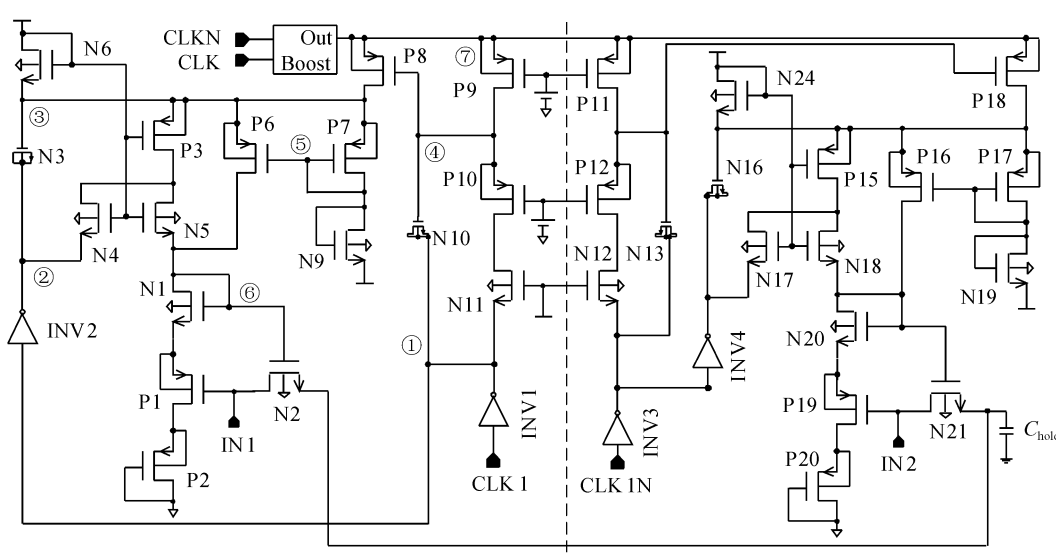

Fig. 2　Proposed multiplexer

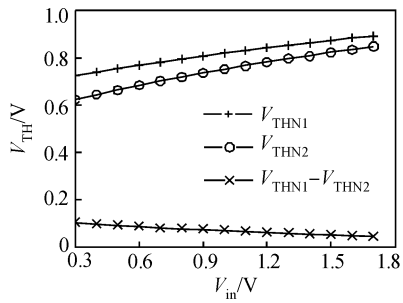

Fig. 3 Threshold voltage variation

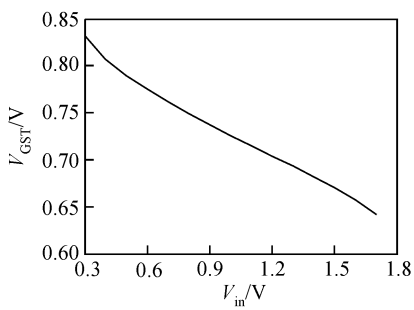

Fig. 4 V_{GST} variation with input signal

Figure 5 is R_{on} versus input for three switches (a regular CMOS, a boostrap switch from Ref. [6], and the proposed), and the proposed switch has the most flatness. A good multiplexer has a break-before-make switch action that guarantees only one channel is selected at a time. Using the test method given in Ref. [7], Figure 6 shows the turn-on and turn-off performance of the switch with input constant at 1.2V. The turn-on and turn-off time is 2.98 and 1.35ns, respectively, which indicates a break-before-make action.

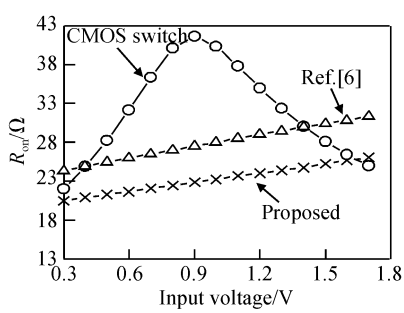

Fig. 5 On-resistance variation with input

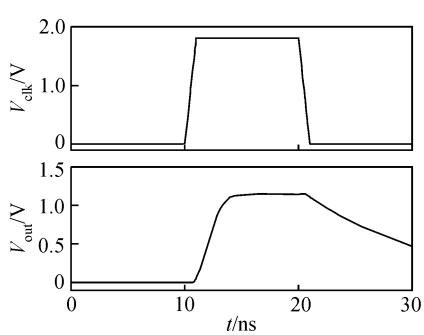

Fig. 6 Turn-on and turn-off performance

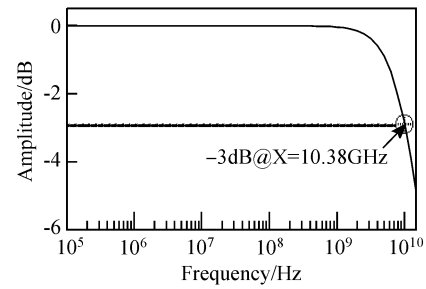

Fig. 7 −3dB bandwidth of the switch

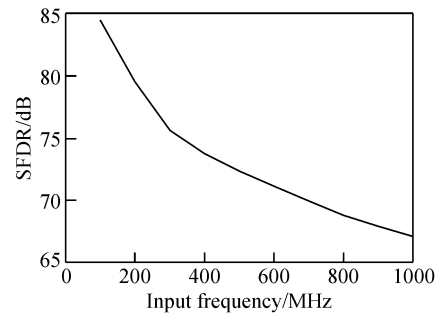

Fig. 8 SFDR versus input frequency

Figure 7 shows the frequency response of the switch. Its −3dB bandwidth can be larger than 10GHz, which allows the multiplexer to transmit signals with GHz frequency. Figure 8 is the SFDR of the output versus input frequency with a 0.8V peak-peak input. As input frequency increases, the SFDR decreases, and the SFDR is 67.11dB with 1GHz input frequency.

5 Conclusion

A multiplexer is proposed with a low-distortion high-bandwidth analog switch. The gate-source voltage of the switch is set by the on-voltage of an nMOS and a pMOS, not only making the difference of gate-source voltage and the threshold voltage constant, achieving a significantly higher linearity, but also making high-speed signal transmission feasible. The −3dB bandwidth of the switch is larger than 10GHz, and the turn-on and turn-off time is 2.98 and 1.35ns, respectively, which guarantees the break-before-make action of the multiplexer. Spectral analysis shows that the SFDR is 67.11dB with an input frequency of 1GHz. The proposed structure is suitable for high speed signal transmission.

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应用于高速信号传输系统的多路选择器*

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摘要：提出了一种能够传输高速信号的多路选择器，并为其设计了一种低失真、宽带模拟开关. 所提出开关的栅源过驱动电压由 nMOS 和 pMOS 的开启电压之和决定，并能够确保输入变化时，开关的栅源电压与阈值电压之差（V_{GST}）保持恒定，从而基本消除了体效应的影响. 采用 TSMC 0.18μm CMOS 工艺，HSPICE 仿真结果表明，输入信号在 0.3～1.7V 之间变化时，开关的 V_{GST} 基本保持恒定，其 -3dB 带宽大于 10GHz，当输入频率为 1GHz 时，其无杂散动态范围为 67.11dB；开关的开启时间为 2.98ns，关断时间为 1.35ns，确保了多路选择器的 break-before-make 特性. 该结构可应用于高速信号传输系统中.

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