A CMOS Power Amplifier with 100% and 18% Modulation Depth for Mobile RFID Readers

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Abstract: Aiming at the specific protocol of RFID technology, a 915MHz CMOS transmitter front-end for OOK modulation is implemented in a 0.18μm CMOS process. The transmitter incorporates a class-E power amplifier (PA), a modulator, and a control logic unit. The direct-conversion architecture minimizes the required on-and-off-chip components and provides a low-cost and efficient solution. A novel structure is proposed to provide the modulation depth of 100% and 18%, respectively. The PA presents an output 1dB power of 17.6dBm while maintaining a maximum PAE of 35.4%.

Key words: CMOS; power amplifier; RFID; transmitter; modulation depth
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1 Introduction

Radio frequency identification (RFID) is a wireless communication technology in which a reader captures data encoded in tags using radio waves[1,2]. Because the worldwide RFID market has been growing tremendously, RFID has become an essential field of research in modern industry. Potential applications of RFID are driving hardware developers to merge RFID readers into mobile devices such as PDAs and cell phones. In the integrated-circuit (IC) design field, great efforts are directed to develop low-cost, efficient solutions for RFID systems[3~6]. Meanwhile, the persistent scaling of CMOS technology has made CMOS-based single-chip solutions competitive for such short-range wireless standards. So, it is necessary to implement highly-integrated CMOS RFID products, such as reader and tags.

Of all the RF front-end components, the most difficult part to implement in a silicon process is the power amplifier (PA). Because of the low breakdown voltage, low transconductance capacity, and poor passive devices in the CMOS process, it is challenging to design a fully-integrated CMOS power amplifier with high output power, efficiency, and linearity. Linear PAs in CMOS can provide a linear output power, but with much lower efficiency. Considering the battery lifetime of mobile devices, efficient non-linear PAs can be a better choice in mobile RFID readers if the linearity demand is not so strict. Among non-linear power amplifiers, class-E PAs are frequent selections in the RF domain[7~9].

This paper aims at the ISO18000-6B protocol operating in the UHF 860~960MHz band[1]. After synthesizing the protocol, the transmitted signal mode between reader and tag is on-off keying (OOK) modulation as a Manchester encoding. The modulation depth of the forward signal is 100% (90%~100% flexible) and 18% (15%~20% flexible) selectively. The data rate is 10 or 40kbps according to local regulations.

This paper demonstrates a feasible 915MHz transmitter front-end for mobile RFID reader applications, which is comprised of a RF signal modulator, a two-stage class-E power amplifier, and a control logic unit. The chip is fabricated in a 0.18μm 1P6M CMOS process. The direct-conversion architecture minimizes the on-and-off-chip components required and provides a low-cost and efficient solution. A novel structure can provide the modulation depth of 100% and 18%, respectively. The PA presents an output 1dB compression of 17.6dBm while delivering a maximum power-added efficiency (PAE) of 35.4%.

2 Circuit implementation

Figure 1 shows the block diagram of the proposed transmitter front-end in a mobile RFID reader. The implemented functional modules include an RF signal modulator, a power amplifier, and a control logic unit. These are shown inside the dashed lines in Fig. 1.

The 915MHz RF carrier is generated by the PLL

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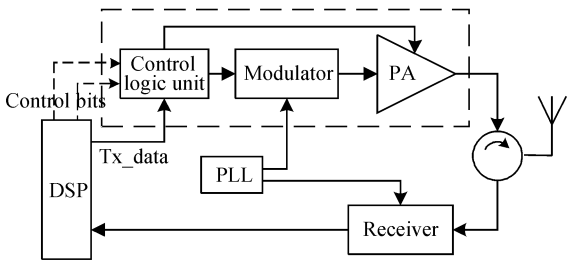

Fig. 1　Block diagram of the transmitter front-end in a mobile RFID reader

in the RFID reader. It passes through the modulator and then the PA. By the operation of the control logic unit, the transmitted OOK data lead to the RF signal modulator or PA separately. The 18% modulation depth is implemented by the operation of the RF signal modulator controlled by the control bits from the DSP module. The 100% modulation depth is fulfilled by an impedance-variable resistor connected to the gate of the output-stage transistor in the class-E PA.

Compared with other transmitter architectures, the proposed architecture has the potential advantages of less components and higher efficiency due to the usage of a class-E PA. The circuit implementation of the main blocks is explained below.

2.1　RF signal modulator

Figure 2 shows the schematic of the RF signal modulator, which serves two functions. One is the RF carrier path from PLL output to PA. The other is the generation of different RF output signals to the PA for the 18% modulation depth.

In order to obtain different RF output signals, two individual resistors are connected to the source node of M01, which functions as a voltage source follower. Meanwhile, in order to alleviate the

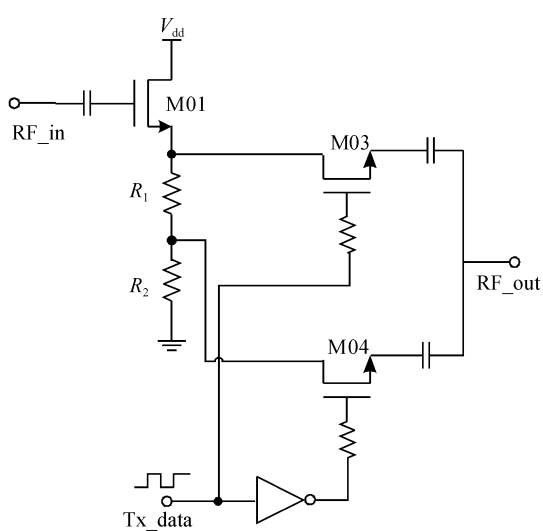

Fig. 2　Schematic of the RF signal modulator

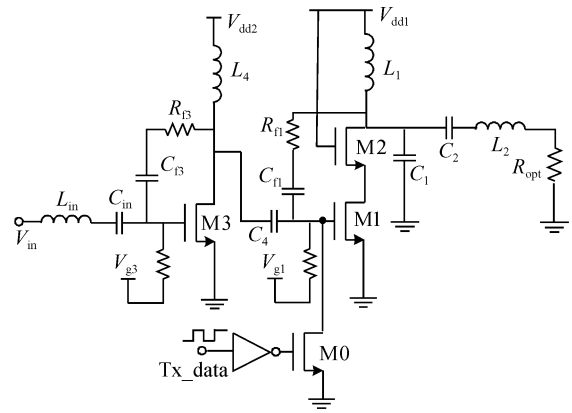

Fig. 3　Schematic of class-E PA

RF signal loss, two switch transistors are in the RF signal path respectively[10,11]. The gates of the switch transistors are controlled by the transmitted OOK data, fulfilling the 18% modulation of the RF signal.

2.2　CMOS class-E power amplifier

Among switched-mode power amplifiers, class-E is the most attractive candidate in terms of circuit simplicity and high frequency performance[9]. Figure 3 shows the implemented 2-stage class-E PA working at 915MHz. The two stages are class-AB and class-E, each with a power gain of about 11dB. Except for the drain inductor L_1, all the other components are implemented on-chip.

Because the maximum drain voltage of the class-E power stage can be over 3 times the supply voltage and the CMOS process sets the limit for the breakdown voltage of transistors[9], a cascode configuration and a thick gate-oxide transistor M2 have been adopted to alleviate the oxide breakdown problem and, accordingly, to employ a larger supply voltage. In the design, M1 is a 0.18μm transistor and M2 is a 0.34μm transistor. With the supply voltage V_{dd1} of 2.5V, the maximum gate-drain voltage does not exceed 2V even at an input signal power as high as 0dBm. On the other hand, if M2 is adopted to be a 0.18μm transistor, the value of V_{dd1} has to be 1.1V to avoid the breakdown of cascode transistor M2. Furthermore, a lower output power is achieved. Resistor R_{f1} and capacitor C_{f1} comprise series feedback to stabilize the output stage.

To the output matching network, the components are selected so that the conditions of soft switching for class-E operation are met: (1) the voltage across the switch transistor M1 is zero when the switch turns on; and (2) the first derivation of the voltage is zero when the switch transistor turns on. These conditions ensure no overlapping between the current and voltage waveform over the whole time period. So there is

no power dissipation to the switch transistor and a theoretical power efficiency of 100% can be achieved for the load. These components' values can be calculated using the following equations[9].

$$R_{\text{opt}} = \frac{8V_{\text{dd}}^2}{P_{\text{out}}(\pi^2+4)} \tag{1}$$

$$C_2 = \frac{P_{\text{out}}(\pi^2+4)}{\omega \times 8V_{\text{dd}}^2 Q_{\text{L}}} \tag{2}$$

$$L_2 = \frac{8V_{\text{dd}}^2 Q_{\text{L}}}{\omega P_{\text{out}}(\pi^2+4)} \tag{3}$$

Also in the design, an output matching network was added off-chip to transform the antenna resistance (50Ω) into a lower value .

In order to obtain the 100% modulation depth of the RF signal, a changeable impedance is connected to the gate of the output-stage transistor M1, which is comprised of a transistor M0 and an inverter. The on-off state of M0 is controlled by the transmitted data, leading to a variable impedance. When the transmitted data is "1", M0 is off and its equivalent effect is to add a small capacitance to the gate of M1. When the transmitted data is "0", the gate voltage of M0 is high. The transistor works in a deep triode region. The equivalent resistance of M0 is:

$$R_{\text{on}} = \frac{1}{\mu_{\text{n}} C_{\text{ox}}(W/L)(V_{\text{GS}} - V_{\text{TH}})} \tag{4}$$

From Eq. (4), a low value of R_{on} is obtained as long as the values of W/L and V_{gs}-V_{TH} are adequately large. Thus, the gate voltage of M1 is near zero and M1 is turned off, leading to a null output to load impedance.

In the driver stage of the PA, a 0.18μm transistor M3 is used. The supply voltage V_{dd2} is 1.8V. In order to obtain better linearity and higher efficiency, a class-AB amplifier is used. Meanwhile, R_{f3} and C_{f3} consist of a feedback network to increase the overall stability.

3 Experimental results

The proposed IC was fabricated in a 0.18μm 1P6M CMOS process. The die photograph is shown in Fig. 4. The majority of the layout is occupied by the class-E PA, which is illustrated in Fig. 3. The other portion is the RF signal modulator shown in Fig. 2. The chip takes 1.92mm × 1.16mm silicon area including pads. A printed circuit board (PCB) for testing the chip was also fabricated. The chip is directly glued to the PCB board using an electrically and thermally conductive adhesive. Ground pads of the chip and the signal pads were wire-bonded to the gold-plated metal lines on the PCB. Off-chip impedance matching components are also added in this design.

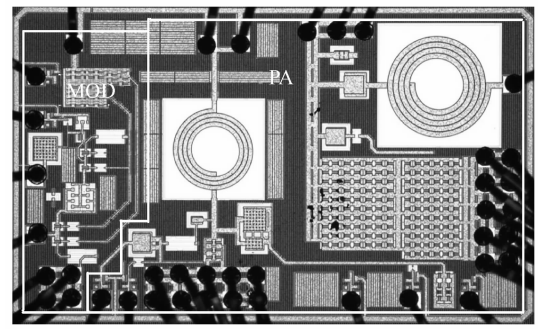

Fig. 4 Microphotograph of the chip

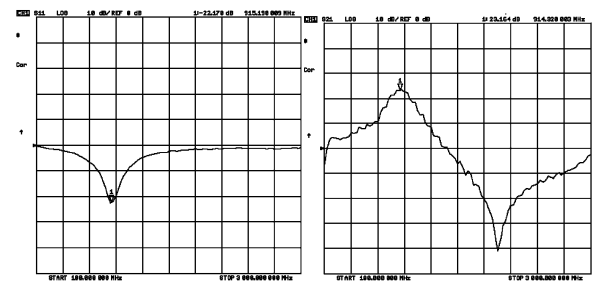

Fig. 5 Measured scattering parameters (S_{11}, S_{21}) of the PA

The measured scattering parameters (S_{11}, S_{21}) of the PA are shown in Fig. 5. It can provide a small-signal gain of 23.1dB at 915MHz.

With a supply voltage of 2.5V and a gate bias voltage of 0.51V in the output stage, and a supply voltage of 1.8V and a gate bias voltage of 0.85V in the driver stage, the power amplifier consumes 90.8mA of DC current overall. The output 1dB power is about 17.6dBm and the maximum PAE of 35.4% is achieved. The measured output power and PAE are shown in Fig. 6.

The transmitted data coding is Manchester coding and the bit rate is 40kbps. The transient waveform of the output signal is measured using an Agilent Infiniium 54845A Oscilloscope. The waveforms are shown in Fig. 7, which demonstrates that the 18% and 100% modulation depth is obtained.

Table 1 shows a summary of the measured results. All the design goals for the ISO18000-6B protocol are met.

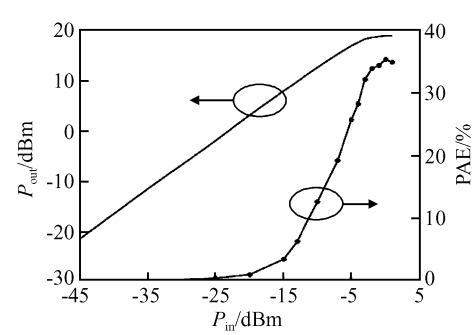

Fig. 6 Measured output power (P_{out}) and power-added efficiency (PAE) versus input power (P_{in}) of the PA

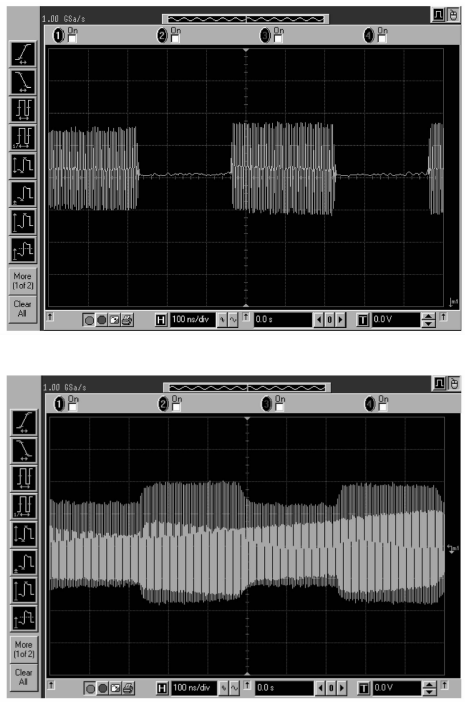

Fig. 7　Transient waveform for 100% and 18% modulation depth

Table 1　Performance summary of the transmitter

Parameter	Measured results
Operating voltage	1.8V + 2.5V
Frequency	915MHz
Small-signal gain	23.1dB
P_{1dB}	17.6dBm
PAE @ maximum	35.4%
DC power@P_{1dB}	199mW

4　Conclusion

In this paper, a 915MHz CMOS transmitter front-end for a mobile RFID reader is designed with a 0.18μm CMOS process. The transmitter provides the output signal with modulation depths of 100% and 18%. The small-signal gain is about 23dB. The fabricated PA delivers a 1dB output power of 17.6dBm with the maximum PAE of 35.4%. The implementation of the 100% modulation depth is the first reported in relevant papers.

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一种用于便携式射频识别阅读器的 CMOS 功率放大器

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摘要：针对一种特定的射频识别技术的通讯协议(ISO1800-6B)，提出了一种应用于射频识别读写器中的发射机前端结构，以实现发射信号的 OOK 调制. 采用 0.18μm CMOS 工艺实现的这种高效率、高度集成的无线发射机前端由射频信号调制器、E 类功率放大器以及相应的逻辑控制单元组成，其中的功率放大器的小信号增益约为 23dB，其 1dB 压缩点输出功率为 17.6dBm，最大输出功率为 19.0dBm，而最大功率增加效率为 35.4%. 整个发射机的输出信号满足相应协议的特定要求，可以实现不同调制深度(18%和 100%)的射频信号输出.

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