A High-PSRR CMOS Bandgap Reference Without Resistor

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Abstract: A CMOS bandgap reference (BGR) without a resistor, with a high power supply rejection ratio and output below 1V is proposed. The circuit is suited for on-chip voltage down converters. The BGR is designed and fabricated using an HJTC 0.18μm CMOS process. The silicon area is only 0.031mm^2 excluding pads and electrostatic-discharge (ESD) protection circuits. Experimental results show that the PSRR of the proposed BGR at 100Hz and 1kHz achieves, respectively, -70 and -62dB using the pre-regulator. The proposed BGR circuit generates an output voltage of 0.5582V with a variation of 1.5mV in a temperature range from 0 to 85℃. The deviation of the output voltage is within 2mV when the power supply voltage V_{DD} changes from 2.4 to 4V.

Key words: CMOS bandgap reference; current source circuit; PSRR; pre-regulator
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1 Introduction

With the rapid evolution of CMOS technology, on-chip CMOS voltage down converters are widely used for power management applications[1]. The voltage reference is an important component in the design of on-chip voltage down converters. It should be free from fluctuations of process, power supply voltage V_{DD}, and temperature, and should also be implemented in the standard CMOS fabrication process. The bandgap reference (BGR) is one of the most popular reference voltage generators, whose output is usually a weighted sum of the forward-bias emitter-base voltages across parasitic vertical pnp in any standard CMOS technology and the thermal voltage V_t[2~4]. The relative weighting is commonly adjusted by trimming the ratio of the resistors. The presence of resistors is a drawback for some applications. In CMOS technologies, resistors' models are not accurate and resistors consume more area than MOS transistors.

As an alternative, a CMOS BGR without resistors was presented by Buck *et al*.[5]. However, the output of the resistor-less BGR circuit is not accurate enough. Song *et al*. adopted an improved core circuit for the BGR and a current proportional to T^{α} (T is the absolute temperature and α is a constant) in order to compensate the higher order for the forward-bias voltages across p-n diodes in the resistor-less BGR[6]. A resistor-less CMOS BGR with less than 1V output has, respectively, been presented by Cheng *et al*.[7] and Weng *et al*.[8]. In general, these reported solutions cannot achieve high power supply rejection ratio (PSRR) over a broad frequency range. Moreover, the supply noise injected to the output of the BGR circuit is the most significant noise. On the other hand, a high PSRR BGR is desired to achieve a high performance VLSI system, particularly in wireless communications. Therefore, it is necessary to choose a BGR structure to achieve high PSRR over a broad frequency range to reject the supply noise coupled from the high-speed digital circuit on the chip.

In this paper, a resistor-less CMOS BGR with less than 1V output is proposed. Employing an improved core circuit for the BGR without a resistor and a pre-regulator, the circuit achieves a high PSRR over a wide frequency range and a good temperature characteristic over a wide temperature range. It is particularly useful as an alternative voltage reference for an on-chip voltage down converter.

2 Conventional bandgap reference

The conventional CMOS BGR without resistors[5] is shown in Fig. 1. For convenience, in this paper, it is assumed that the current through transistor Mi is I_i; W_i and L_i are, respectively, the channel width and length of transistor Mi. In Fig. 1, the proportional to absolute temperature (PTAT) voltage $\Delta V_D = V_{D4} - V_{D3}$ is applied across the differential pair M12, M13, and the resulting current is multiplied by G using current mirror M16, M17 and is delivered to the differential pair M14, M15. V_{D3} and V_{D4} are, respectively, the forward bias voltages across diode Q3 and diode Q4.

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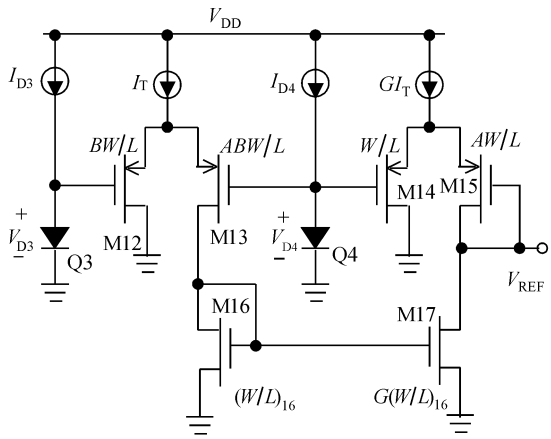

Fig. 1 Core schematic of the conventional BGR

Here, Q3 has an area that is N times that of Q4. All the MOS transistors work in strong inversion. So, the output voltage of the conventional BGR circuit, i.e., V_{REF}, can be written as

$$V_{REF} = V_{D4} + \sqrt{BG}(V_{D4} - V_{D3}) \quad (1)$$

V_{D4} has a negative temperature coefficient, and the second term in Eq. (1) is proportional to the absolute temperature T. So, by choosing the appropriate parameters for B and G, the temperature dependence of V_{REF} will become negligibly small.

3 Proposed bandgap reference

Figure 2 shows the complete schematic of the proposed BGR, and all MOS transistors adopt the long channel transistor so that the channel-length modulation effect is negligibly small. The proposed BGR consists of the core circuit of the BGR, the current source circuit, the pre-regulator, and a start-up circuit. The current source circuit, whose operating supply voltage is the internal regulated supply voltage V_{REG}, produces a current proportional to T^{α} (here, T is the absolute temperature and α is a constant), and will be discussed in Section 3.1. Because there are two possible equilibrium points on the current source circuit, a start-up circuit is necessary. MS1 ~ MS5 are the start-up circuits. The core circuit of BGR generates a bandgap voltage V_{REF} less than 1V and has a good temperature characteristic, and will be analyzed in Section 3.2. The function of the pre-regulator is to produce an internally regulated supply voltage V_{REG} that is the operating supply voltage of the core circuit of the BGR and the current source circuit instead of the power supply voltage V_{DD}. V_{REG} is adjusted by a negative feedback loop such that the condition of equality of the voltages at nodes 1 and 2 is achieved. So, the variation of V_{DD} can be rejected. Detailed analysis and design of the pre-regulator and PSRR will be presented in Section 3.3.

3.1 Current source circuit

As shown in Fig. 2 (b), the proposed current source circuit consists of M1 ~ M7, Q1, and Q2. It is similar to that reported in Ref. [6] but the operating supply voltage is replaced by V_{REG} and only nine transistors are adopted instead of eleven. Q1 and Q2 are the same. M2 ~ M7 form a cascode current mirror and $I_2 = NI_3$. Given a bias current I_C in the pnp transistor, it is concluded that the emitter-base voltage $V_{EB} = V_t \ln(I_C/I_S)$, where V_t is the thermal potential (kT/q). So, the drain-source voltage of M1, i.e., V_{DS1}, is equal to $V_t \ln N$. In fact, the temperature function of the mobility of an electron with a reference temperature T_r, i.e., μ_n, can be modeled as[9,10]

$$\mu_n(T) = \mu_n(T_r)(T/T_r)^{-\beta_{\mu n}} \quad (2)$$

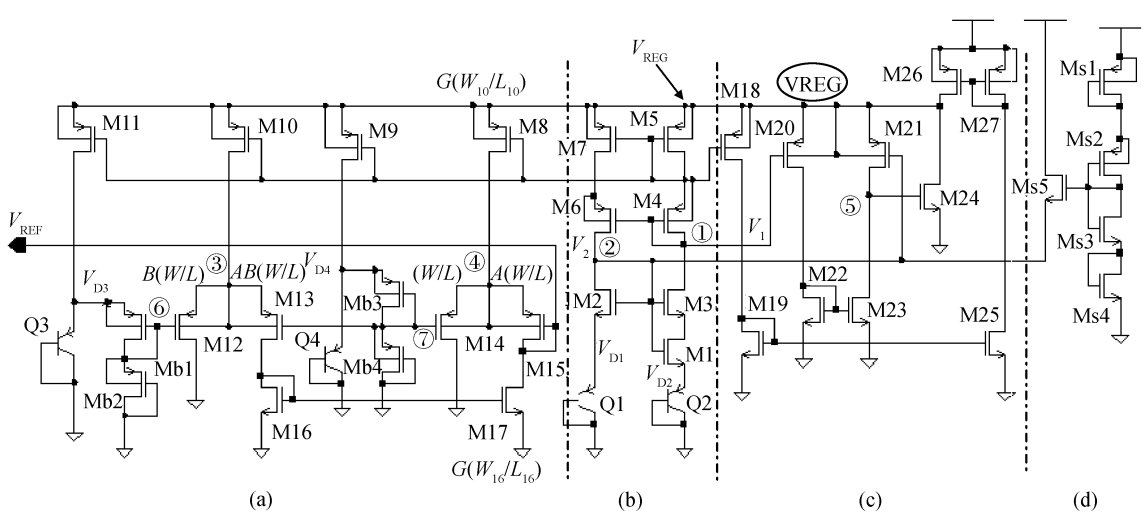

Fig. 2 Proposed BGR (a) Core circuit of BGR; (b) Circuit of current source; (c) Pre-regulator; (d) Start-up circuit

where $\mu_n(T_r)$ is the mobility of an electron at temperature T_r and $\beta_{\mu n}$ is the mobility exponent of an electron. In Fig. 2(b), M2～M7 operate in the saturation region and M1 is in the triode region. So, the drain current of M5 can be given as

$$I_5 = PT^{\alpha} \tag{3}$$

where

$$P = \frac{C_{OX}}{2}\left(\frac{W_1}{L_1}\right)^2\left(\sqrt{\frac{L_3}{W_3}}+\sqrt{\frac{L_3}{W_3}+\frac{L_1}{W_1}}\right)^2 \times \left(\frac{k}{q}\ln N\right)^2 \times \frac{\mu_n(T_r)}{T_r^{-\beta_{\mu n}}}$$

$$\alpha = 2 - \beta_{\mu n}$$

C_{OX} is the gate oxide capacitance per unit area. Equation (3) shows that the current I_5 is proportional to T^{α}.

3.2 Core circuit of bandgap reference

The core circuit of the proposed BGR is shown in Fig. 2(a) and consists of M8～M17, Q3～Q4, and Mb1～Mb4. The operating supply voltage of the proposed core circuit of BGR is V_{REG} instead of V_{DD}. Transistors M11-M5 and M9-M5 are, respectively, current-mirror pairs. $(W/L)_{11} = K_{11}(W/L)_5$ and $(W/L)_9 = K_9(W/L)_5$. So $I_{11} = K_{11}PT^{\alpha}$ and $I_9 = K_9PT^{\alpha}$. Transistor Q3 has an area that is N_1 times that of Q4. So the saturation current of Q3 and Q4 has $I_{S3} = N_1 I_{S4}$. The emitter-base voltage $V_{EB}(T)$ in the pnp transistor, with a bias current in the form of $I(T) = MT^{\beta}$ (here β and M are the constants), can be expressed as[9]

$$V_{EB}(T) = V_{G0} - V_t[(\gamma-\beta)\ln T - \ln(ME)] \tag{4}$$

where V_{G0} is the bandgap voltage of silicon at temperature 0K, E is a constant, and γ is a process dependent parameter equal to $4 - m$ (the constant m comes from the temperature exponent of the carrier mobility dependence on temperature). In Fig. 2(a), Mb1～Mb4 are all long-channel pMOS resistors (i.e. $L/W \geqslant 10$), and are the same. They have negligibly small drain current. The emitter currents of Q3 and Q4 are, respectively, $I_{Q3} = I_{11} = K_{11}PT^{\alpha}$ and $I_{Q4} = I_9 = K_9PT^{\alpha}$. So, the emitter-base voltages of Q3 and Q4 (i.e. V_{D3} and V_{D4}) are, respectively, written as

$$V_{D4}(T) = V_{G0} - V_t[(\gamma-\alpha)\ln T - \ln(EPK_9)] \tag{5}$$

$$V_{D3}(T) = V_{G0} - V_t[(\gamma-\alpha)\ln T - \ln(EPK_{11})] - V_t\ln N_1 \tag{6}$$

To analyze the voltages at node 6 and node 7, which are denoted as V_6 and V_7, respectively, a single-expression MOSFET model[11,12] useful in the weak, moderate, and strong inversion regions, will be employed. It is given by

$$I_d = 2\mu C_{OX}\frac{W}{L}nV_t^2\ln^2[1 + e^{(V_{GS}-V_{TH})/2nV_t}] \tag{7}$$

where n is defined in Ref. [12], and V_{TH} is the threshold voltage of the MOSFET. Transistors Mb1～Mb4 are the same and have negligibly small drain current, so the voltages V_6 and V_7 can, respectively, be expressed as

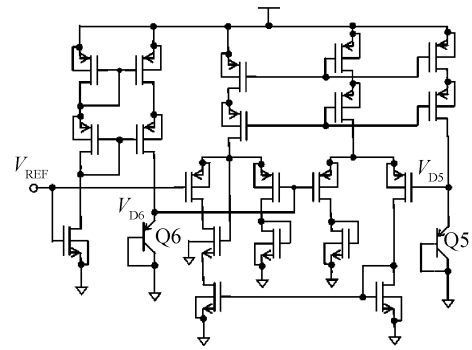

Fig. 3　Core circuit of BGR reported in Ref. [6]

$$V_6(T) = 0.5V_{D3}(T) \tag{8}$$

$$V_7(T) = 0.5V_{D4}(T) \tag{9}$$

Thus, the temperature characteristics of V_6 and V_7 are, respectively, the same as those of V_{D3} and V_{D4}. That is, the temperature characteristic of the BGR is not affected by the dividers Mb1～Mb4. M12～M17 operate in the saturation region, and $(W/L)_{14} = A^{-1}(W/L)_{15} = (W/L)_{12}B^{-1} = (W/L)_{13}A^{-1}B^{-1}$. M8-M5, M10-M5, and M16-M17 form, respectively, current-mirror pairs, and they have $(W/L)_8 = G(W/L)_{10}$ and $(W/L)_{17} = G(W/L)_{16}$. So, the output voltage of the proposed BGR, i.e., V_{REF}, is obtained as

$$V_{REF} = V_7 + \sqrt{BG}(V_7 - V_6) = 0.5V_{D4} + 0.5\sqrt{BG}(V_{D4} - V_{D3}) = \frac{1}{2}\left\{V_{G0} - V_t[(\gamma-\alpha)\ln T - \ln(EPK_9)] + V_t\sqrt{BG}\ln\frac{N_1K_9}{K_{11}}\right\} \tag{10}$$

Differentiating Eq. (10) with respect to temperature T, the temperature dependency of V_{REF} can be written as

$$\left.\frac{dV_{REF}}{dT}\right|_{T=T_0} = -\frac{1}{2}\times\frac{V_{t0}}{T_0}(\gamma-\alpha)(1+\ln T_0) + \frac{1}{2}\times\frac{V_{t0}}{T_0}\left(\ln(EPK_9) + \sqrt{BG}\ln\frac{N_1K_9}{K_{11}}\right) \tag{11}$$

As shown in Eq. (11), $(\partial V_{REF}/\partial T)|_{T=T_0} = 0$ (where T_0 is the room temperature) can be obtained by optimizing the circuit parameters. However, an absolutely temperature-independent V_{REF} is not possible over the whole temperature range, so a nonlinear temperature-dependent error voltage appears at V_{REF}. Compared with the temperature dependency of the BGRs, which have been reported in Refs. [5, 7, 8], they are on a commensurate level.

However, the BGR presented in this paper has a higher temperature coefficient than that reported in Ref. [6]. For convenience, the core circuit of the BGR, which is presented in Ref. [6], is shown in Fig. 3. The emitter current of Q5 is proportional to T^{α}

(i.e., $G_2 T^{\alpha}$, G_2 is a constant), which is similar to that of Q3 and Q4 in Fig. 2. Nonetheless, the emitter current of Q6 is independent of the temperature T and is a constant G_1. So, the emitter-base voltages of Q5 and Q6 (i.e., V_{D5} and V_{D6}) have $V_{D5} - V_{D6} = V_t \ln(G_2/G_1) + \alpha V_t \ln T$, which cancel the first order of the T term and the skewed-parabola shaped $T\ln T$ term in V_{D6}. Whereas, in this paper, $V_{D4} - V_{D3} = V_t \ln(N_1 K_9/K_{11})$, and only cancels the first order of the T term and not the $T\ln T$ term in V_{D4}. That is to say, the circuit reported in Ref. [6] is a higher order corrected BGR, but the proposed circuit in this paper is only a first order corrected BGR. Therefore, the output voltage of the BGR reported in Ref. [6] has a lower temperature dependency.

3.3 Pre-regulator and PSRR

To achieve a high power supply rejection ratio (PSRR) over a broad frequency range, a pre-regulator circuit configuration is introduced. A simple circuit is chosen in this paper, based on the consideration of stability and complexity of the circuit, as shown in Fig. 2(c). The operational transconductor amplifier (OTA) forms a negative feedback loop, and consists of M18 ~ M27. Therefore, the operating supply voltage of the proposed BGR core and current source circuit is the output of the OTA instead of V_{DD}. The output of the OTA should be set to ensure that transistor M26 is in the saturation region and the proposed BGR can work out its function. The voltage variations at node 1 and node 2 are, respectively, sensed by M20 and M21. The amplified voltage is sensed by M24, which feeds a current into the node VREG to force it to the correct voltage. The PSRR can be quantitatively analyzed as follows.

Let us assume an incremental variation v_{reg} at node VREG. For convenience, it is assumed that g_{mi} is the transconductance of Mi; and i_{mi} is the small-signal current of Mi. We can now write the following expressions for the incremental currents in the circuit.

$$i_{m5} = \frac{v_{reg}}{1/g_{m5} + 1/g_{m4} + g_{m3} R_{S1} r_{ds3}} \tag{12}$$

$$M_j : \begin{cases} i_{mj} = g_{mj} i_{m5}/g_{m5} \\ j = 7 \sim 11, \text{and } 18 \end{cases} \tag{13}$$

where R_{S1} is the equivalent resistance seen from the drain of M1 to ground and r_{ds3} is the source-drain resistance of M3. It is assumed that v_1 and v_2 are, respectively, the incremental voltage variation at node 1 and node 2. We have

$$v_1 = i_{m5} \times g_{m3} R_{S1} r_{ds3} \approx v_{reg} \tag{14}$$

$$v_2 = i_{m7} \times r_2 \approx 0 \tag{15}$$

$$i_{m20} = g_{m20}(v_{reg} - v_1) \approx 0 \tag{16}$$

$$i_{m21} = g_{m21}(v_{reg} - v_2) \approx g_{m21} v_{reg} \tag{17}$$

$$i_{m24} = g_{m24}(i_{21} - i_{m20} g_{m23}/g_{m22}) r_5 \approx g_{m24} g_{m21} v_{reg} r_5 \tag{18}$$

where r_2 denotes the output resistance seen from the drain of M2 to ground and r_5 is the output resistance seen at node 5. According to the Kirchhoff current law (KCL) at node VREG, the following equations can be obtained:

$$\frac{v_{dd} - v_{reg}}{r_{ds26}} + \frac{g_{m26}}{g_{m27}} \times \frac{g_{m25} g_{m18}}{g_{m19} g_{m5}} i_{m5} = i_{m24} + i_{m21} + i_{m20} + i_{m18} + i_{m7} + i_{m5} + i_{m8} + i_{m9} + i_{m10} + i_{m11} \tag{19}$$

where v_{dd} is the incremental voltage variation at power supply voltage V_{DD} and r_{ds26} is the source-drain resistance of the transistor M26. It is derived as

$$\frac{v_{reg}}{v_{dd}} \approx \frac{1}{g_{m24} g_{m21} r_5 r_{ds26}} \tag{20}$$

In a similar way, the voltage variation at the output node of BGR, i.e., v_{ref}, can be expressed as

$$v_{ref} = 0.5 v_{d4} + \sqrt{BG}(0.5 v_{d4} - 0.5 v_{d3}) \tag{21}$$

where v_{d4} and v_{d3} are, respectively, the incremental voltage variation at the emitter of Q3 and Q4. According to the circuit in Fig. 2, v_{d4} and v_{d3} are, respectively, expressed as

$$v_{d3} = g_{m11} i_{m5} r_{e3}/g_{m5} \tag{22}$$

$$v_{d4} = g_{m9} i_{m5} r_{e4}/g_{m5} \tag{23}$$

where r_{e3} and r_{e4} are, respectively, the emitter resistance of Q3 and Q4. According to Eq. (10) and Eq. (21) ~ Eq. (23), it is derived as

$$\frac{v_{ref}}{v_{reg}} = \frac{g_{m9} r_{e4} + \sqrt{BG} g_{m9} r_{e4} - \sqrt{BG} g_{m11} r_{e3}}{2 g_{m5}(1/g_{m5} + 1/g_{m4} + g_{m3} R_{S1} r_{ds3})} \tag{24}$$

So, the PSRR of the proposed BGR can be written as

$$\text{PSRR}_{dB} = 20\lg\left|\frac{v_{ref}}{v_{dd}}\right| = 20\lg\left|\frac{v_{ref}}{v_{reg}}\right| + 20\lg\left|\frac{v_{reg}}{v_{dd}}\right| \tag{25}$$

The equation shows that the PSRR of the proposed BGR will be improved significantly over a wide frequency range. However, in high frequency, the gate and source-drain transconductance of the MOS transistor, i.e., g_m and g_{sd}, can be modeled as[10]

$$g_m(\omega) = \frac{g_{m0}}{1 + j\omega\tau_1} \tag{26}$$

$$g_{sd}(\omega) = \frac{g_{sd0}}{1 + j\omega\tau_1} \tag{27}$$

where g_{m0} and g_{sd0} are, respectively, the gate and source-drain transconductance in low frequency; τ_1 is defined in Ref. [10]. So, as the frequency increases, |PSRR| of the proposed BGR will decrease.

4 Experimental results

The proposed BGR was fabricated in an HJTC 0.18μm 1P6M CMOS process. The micrograph is shown in Fig. 4, and the occupied chip area is 0.031mm^2 excluding pads and electrostatic-discharge

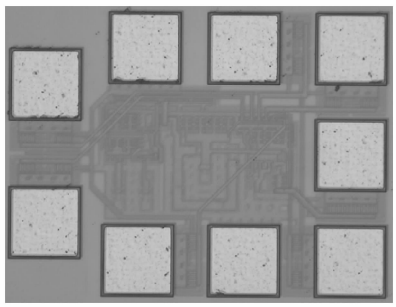

Fig. 4　Microphotograph of BGR without resistor

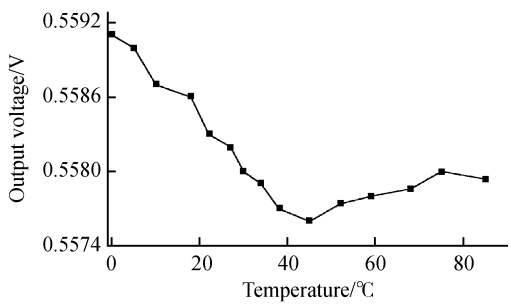

Fig. 5　Measured output voltage versus temperature

(ESD) protection circuits. The circuit was tested at 25℃, and the average output was 0.5582V. Figure 5 shows a plot of the output voltage versus temperature varying from 0 to 85℃ with a power supply voltage of 2.5V. The output voltage has a variation of 1.5mV. The measured supply dependence at 25℃ is shown in Fig. 6. The output voltage deviation of the proposed BGR is within 2mV when the power supply voltage V_{DD} changed from 2.4 to 4V.

The measured PSRR is shown in Fig. 7. The measurement condition is at room temperature without a filtering capacitor. The PSRR at 100Hz, 1kHz, and 10kHz are, respectively, −70, −62, and −43dB. The PSRR is sufficient for a typical on-chip voltage down converter.

Finally, Table 1 briefly compares the BGR proposed in this paper and the previous resistor-less BGRs. The proposed BGR reduces the output voltage variation and its output has high-PSRR performance.

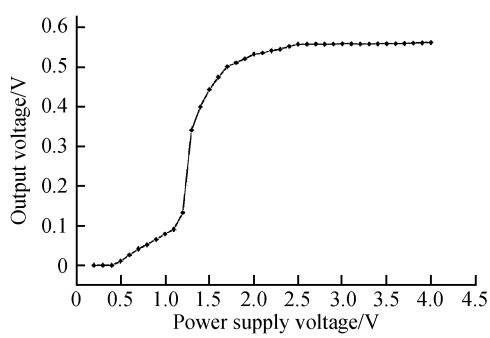

Fig. 6　Measured output voltage versus V_{DD}

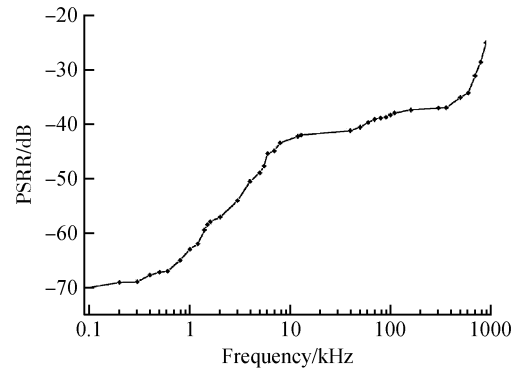

Fig. 7　Measured PSRR versus frequency

Table 1　Performance summary of the proposed bandgap references

Parameter		Ref.[5]	Ref.[7]	Ref.[8]	This work
Chip area/mm^2		0.4	−	0.1	0.031 (except ESD)
Supply voltage/V		3.7	2.5	1.8	2.5
Power dissipation/mW		1.4	0.3	−	0.26
Reference voltage/V		1.108	0.675	0.6151	0.5582
Temperature coefficient /(ppm/℃)		121	181	32.5	31.6
PSRR@25℃ /dB	100Hz	−45	−	−34.4	−70
	1kHz	−30	−	−34.3	−62
	10kHz	−15	−	−34	−43
	100kHz	−8	−	−23	−38

5　Conclusion

A CMOS BGR without resistors, which has an output below 1V, has been proposed. It uses an improved core circuit for the BGR without a resistor and pre-regulator, and achieves high PSRR performance. The architecture of the proposed BGR is simple and has a small silicon area. Experimental results show that the proposed BGR provides an output voltage with excellent stability, a low-temperature coefficient, and high PSRR performance. It is well suited for an on-chip CMOS voltage down converter.

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一种无电阻高电源抑制比的 CMOS 带隙基准源

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摘要：提出一种输出低于 1V 的、无电阻高电源抑制比的 CMOS 带隙基准源(BGR). 该电路适用于片上电源转换器. 用 HJTC 0.18μm CMOS 工艺设计并流片实现了该带隙基准源，芯片面积(不包括 pad 和静电保护电路)为 0.031mm^2. 测试结果表明，采用前调制器结构，带隙基准源电路的输出在 100Hz 与 1kHz 处分别获得了 -70 与 -62dB 的高电源抑制比. 电路输出一个 0.5582V 的稳定参考电压，当温度在 0～85℃范围内变化时，输出电压的变化仅为 1.5mV. 电源电压 V_{DD} 在 2.4～4V 范围内变化时，带隙基准输出电压的变化不超过 2mV.

关键词：CMOS 带隙基准；电流源；电源抑制比；预调整器
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