Design of a Frequency Divider with Reduced Complexity Based on a Resonant Tunneling Diode

Du Rui†, Dai Yang, and Yang Fuhua

(*Research Center of Semiconductor Integration, Institute of Semiconductors, Chinese Academy of Sciences, Beijing* 100083, *China*)

Abstract: A novel edge-triggered D-flip-flop based on a resonant tunneling diode (RTD) is proposed and used to construct a binary frequency divider. The design is discussed in detail and the performance of the circuit is verified using SPICE. Relying on the nonlinear characteristics of RTD, we reduced the number of components used in our DFF circuit to only half of that required using conventional CMOS SCFL technology.

Key words: frequency divider; D-flip-flop; RTD; reduced complexity
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1 Introduction

A resonant tunneling diode (RTD) is one of the fastest nanoelectronics devices. With the characteristic of negative differential resistance (NDR), RTD has extensive applications in ultra-high-speed ICs (integrated circuits) and can reduce the circuit complexity.

RTDs can be integrated with high-electron-mobility transistors (HEMTs) in ultra-high-speed applications and integrated with CMOS for the dominant position of ICs[1,2]. A typical structure of RTD integrated with FET is a monostable-to-bistable transition logic element (MOBILE). Due to its self-latching and multiple stability characteristics, it can be used to design a divider circuit.

We analyzed and compared three different DC models, one of which is a semi-experiential DC model that is optimized for Divider Circuit Design and Simulation. We also analyzed two kinds of MOBILE dividers that have been reported[3,4] and their design method is discussed in detail. Finally, a new kind of standard DFF divider is proposed.

2 Method and results

2.1 Set up of the DC model for RTD

For digital IC design, a DC model is required. But due to the fully nonlinear DC behavior, the SPICE model built for circuit simulation always brings bad convergence. There have been different limiting algorithms proposed to control the convergence in simulation[5]. However, by using the semi-experiential DC model[6], the convergence of simulation in our study is acceptable without those algorithms. Three different DC models are compared in Table 1.

As shown in Fig. 1, the DC curve of an actual RTD can be divided into four pieces: the PDR1 (positive differential resistance) region, the NDR (negative differential resistance) region, the valley region,

Table 1 Comparison of different RTD DC models

	Physics-based model[7]	Semi-experiential model[6]	Piecewise linear model
Simulation accuracy	Common: Character of valley region is not reflected	Good: Character of valley region is reflected	Common
Convergence	Bad: Curve is not smooth, NDR is too cragged	Common: Curve is smooth	Bad
Physical meanings of parameter	None	Some parameters have physical meanings	None

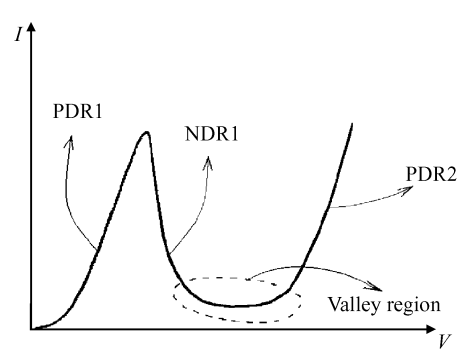

Fig. 1 DC characteristics of an actual RTD

† Corresponding author. Email: ddrr@semi.ac.cn
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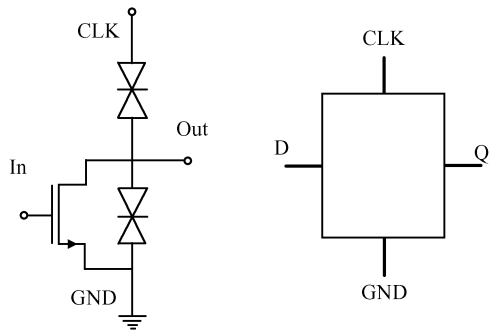

Fig. 2　Circuit configuration and the logic symbol of MOBILE

and the PDR2 region[8]. The mathematical expression of a physics-based model is composed of a resonant tunneling current term and a thermo-electron emission current term that has an exponential relation with the voltage crossed RTD[7]. However, the current of RTD unavoidably includes components of unelastic tunneling current[9], which, together with the NDR region of the resonant tunneling current, causes the valley region. If a piecewise linear model is used, although the accuracy can be fully optimized by increasing data points, the convergence will worsen due to the increase of unsmooth points.

Through practice, the semi-experiential model[6] is selected for simulation. The *I*-*V* equation is: $I = C_1 V^i \{a\tan[C_1(V - V_T)] - a\tan[C_2(V - V_N)]\} + C_3 V^j + C_4 V^k$. This experiential equation can be used to fit a particular RTD's DC characteristic, because V_T and V_N are evaluated directly. Usually we assume $i = 3$, $j = 5$, $k = 3$ because they are approximated and simplified from an exponential relation of a physics-based model[5].

By altering parameter C_1 linearly, the peak current and valley current also vary linearly. Through calculation, we found that the peak-valley current ratio (PVCR) is strongly affected by the parameter C_2. The characteristic of the PDR2 region is almost completely dependent on the parameter C_3. C_4 offers a good match near the valley point[6]. So, C_1, C_2 are adjusted earlier than C_3 and C_4 for a good match.

2.2　Design of a required MOBILE

A standard MOBILE[10] is composed of two serial RTDs and one FET (field effect transistor). The circuit configuration and the logic symbol is shown in Fig. 2. We customarily call the RTD connected parallel to the FET Load RTD and call the other the Drive RTD.

The core principle of a MOBILE is the adjustment of current by FET. If the current flowing in RTD is larger than its peak current, the RTD will be quenched because of the quantum effect. While the offset voltage is rising from zero, if there is neither current flowing into the input node nor current flowing out of the output node of MOBILE, then which RTD is quenched first is determined by the input voltage. After that the output level is fixed. From the figure, we can see that the output level is between zero and V_{CLK}. The logic characteristics of a bistable MOBILE are shown in Table 2.

Table 2　Logic characteristics of a bistable MOBILE

CLK	*D*	Q^{n+1}
1	X	Q^n
0	X	0
↑	1	0
↑	0	1

A MOBILE should work under a bistable state and be self-restoring, i.e., the circuit design requires that a MOBILE can be driven by its own output level. To obtain such a MOBILE, there are design rules to obey. To simplify the discussion, we always assume that the FET is exactly cut off when input is Low. If this is not satisfied, as a FET of depletion mode, it can also be used to construct a required MOBILE.

In a digital circuit, since input voltage is either low or high and a MOBILE is often driven by the other MOBILE, there are four operating points of a MOBILE circuit, which is demonstrated in Fig. 3. The initial value of the output voltage must be V_{H1} and V_{L1}. The value V_{H2} and V_{L2} are obtained when input is reversed during the latching state. But, it is always the case that $V_{H1} > V_{H2}$ and $V_{L1} < V_{L2}$.

First, the parameters of RTD are considered. The peak current of load RTD should be larger than that of drive RTD, which can be easily realized by controlling the emitter area in the layout design. Furthermore, when the vertical structure of the RTD is designed, in order to reduce the power dissipation and to

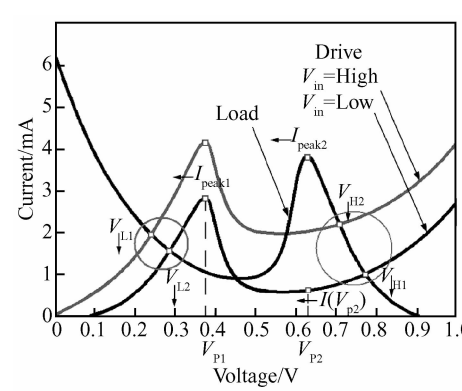

Fig. 3　DC Load diagram for MOBILE　The *x*-axis represents the voltage crossed drive RTD and the *y*-axis represents the current flow in it.

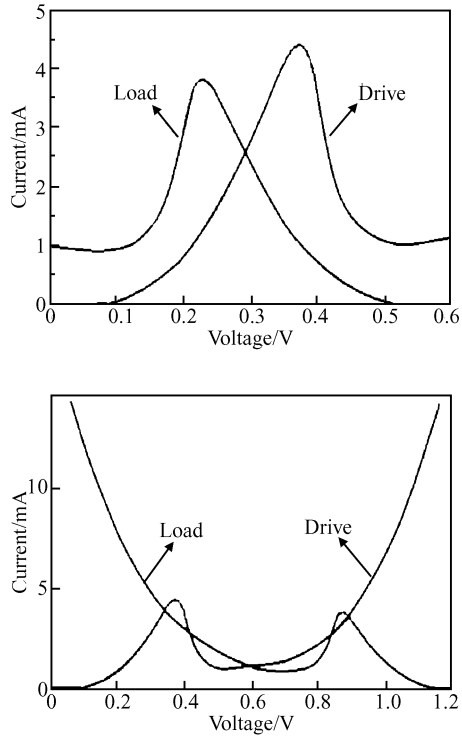

Fig. 4 Choice of offset voltage

improve the noise margin, we always try to reduce its threshold voltage and peak voltage. But a low peak voltage will lead to selecting a low offset voltage, which may make the output voltage become too low for practical application.

Second, an offset voltage V_{CLK} must be set to ensure that the circuit has two stable operating points. As V_{CLK} increases, the number of intersections of two DC load lines increases from one to at most five and then decreases from five to one (Fig. 4). We choose the offset voltage that makes the load lines have three intersections, two of which are in the PDR region. They are stable operating points because they are the valley points in the potential energy diagram[11]. To make a trade-off between the power dissipation and the noise margin, usually an offset voltage slightly larger than $2V_p$ is selected.

Finally, a proper FET must be designed to ensure the correct logic principle of MOBILE. From Fig. 3, we find two qualifications:

$$I_{ds} = I_{ds}(V_{gs}, V_{ds}) = I_{ds}(V_{H2}, V_{p1}) > I_{peak2} - I_{peak1} = \Delta I_{peak} \quad (1)$$

$$I_{ds} = I_{ds}(V_{gs}, V_{ds}) = I_{ds}(V_{H1}, V_{p2}) < I_{peak2} - I(V_{p2}) \quad (2)$$

where $I(V_{p2})$ is the current flow in the drive RTD when the voltage through it is V_{p2}.

Equation (1) ensures that the total current flowing in Drive RTD and the FET is larger than the current flowing in the Load RTD when the V_{gs} of the FET equals V_{H2}.

Equation (2) ensures that the output can be locked at H2 when the input turns from low to high. From the operation principle of MOBILE, the output will be always locked at L2 when the input is turned from high to low if the offset is set appropriately. Thus, it is not necessary to consider it separately.

If the FET is not strictly cut off when input is low, besides the qualifications similar to Eqs. (1) and (2) mentioned above, an additional qualification must be obeyed:

$$I_{ds} = I_{ds}(V_{gs}, V_{ds}) = I_{ds}(V_{L2}, V_{p1}) < I_{peak2} - I_{peak1} = \Delta I_{peak} \quad (3)$$

From Eqs. (1) and (3), the lowest allowable input high voltage and the highest allowable input low voltage both increase with the value of ΔI_{peak}. Thus according to the definition of noise margin, the noise margin of high voltage and low voltage can not be improved at the same time by adjusting the value of ΔI_{peak}.

Solving for parameters like the W/L of CMOS and the gate width of a shot-gate HEMT, we secure the design rules of the FET.

The DC model used in simulation is fitted to an experimental I-V curve from a typical double-barrier RTD[12]. Finally, we obtained two groups of parameters for simulation:

Load RTD: $V_T = 0.1\text{V}$, $V_N = 0.4\text{V}$, $i = 3$, $j = 5$, $k = 3$, $C_1 = 0.032$, $C_2 = 38.3$, $C_3 = 0.0035$, $C_4 = -0.0000358$

Drive RTD: $V_T = 0.1\text{V}$, $V_N = 0.4\text{V}$, $i = 3$, $j = 5$, $k = 3$, $C_1 = 0.0237$, $C_2 = 38.3$, $C_3 = 0.00242$, $C_4 = -0.0000264$

The parameters of the two RTDs are proportioned because their vertical structures are uniform.

The nMOS of the Schichman-Hodges Model is used in calculation. The gate-length is 1μm and V_T is 0.3V. Using the RTD model above, a proper range of W is found: $50\mu\text{m} \leqslant W \leqslant 100\mu\text{m}$.

2.3 Circuit design

Since MOBILE can work as an inverter and with characteristics of self-latching, it is similar to DFF to some extent. So MOBILE can be used to construct a binary divider.

Arai[3] designed a divider using two standard MOBILE based on RTD integrated with HEMT. The circuit configuration is shown in Fig. 5. An HEMT inverter with a resistor load is used to supply the feedback.

Matsuzaki[4] designed a divider using a standard MOBILE based on RTD integrated with HEMT and a "reversed MOBILE" to supply feedback, demonstrating an additional inverter is not necessary. The cir-

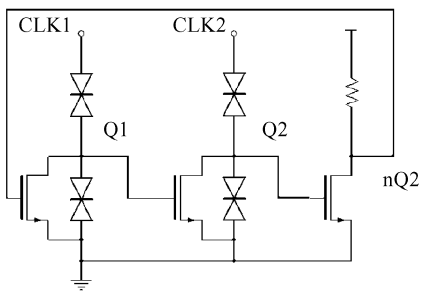

Fig. 5　Circuit configuration of the binary divider proposed by Kunihiro

cuit configuration is shown in Fig. 6. But in such a reversed MOBILE, the source electrode of the FET is not connected to ground. We assume the voltage through the drive RTD is V_X. The FET is turned on only when $V_X > V_{CLK} + V_T - V_g$. While V_T is positive, the FET is turned on only if V_X is big enough. It may not meet the condition that $I_{ds} + I_{peak(Drive\ RTD)} > I_{peak(Load\ RTD)}$. Therefore, a FET of depletion mode is used in this circuit.

Both dividers are verified by SPICE using the MOBILE model mentioned above. The results accord very well with the test.

We can infer timing diagrams of the two dividers from Table 2. The output is turned to low every falling edge of CLK but turned to high every other rising edge of CLK. So the circuits work as binary frequency dividers.

The two designs above reduce the complexity of the circuit compared with conventional SCFL technology. But this only refers to the core circuit. One problem is that the duty ratio of the clock can not equal 1∶1. Another is that a two-stage MOBILE binary divider always needs two phase clocks between which there is a certain phase difference ($w_0 < \Delta_\varphi < w_1$ or $w_1 < \Delta_\varphi < w_0$, where Δ_φ is the phase difference, w_0 is the low-level time length of CLK, and w_1 is the high-level time length of CLK) to continue working. So, it may need a clock buffer to perform an accurate delay. These limitations may make the design unsuitable for practical application.

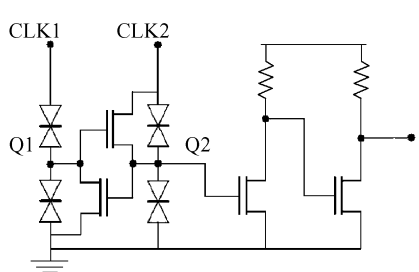

Fig. 6　Circuit configuration of the binary divider proposed by Matsuzaki

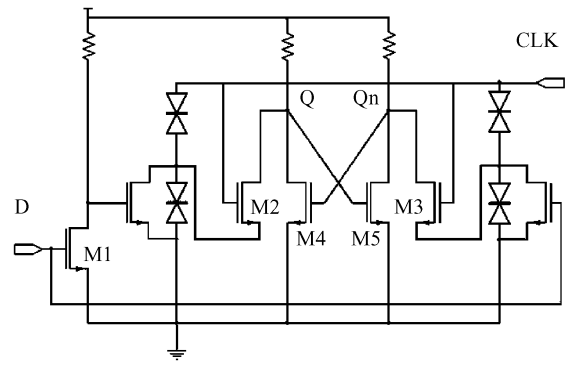

Fig. 7　A new configuration of an edge-triggered DFF based on MOBILE

Considering the traits of MOBILE, a new configuration of an edge-triggered DFF is designed, which is shown in Fig. 7. The DFF consists of two standard MOBILEs and a crossed structure working as a latch of the output. The output of MOBILE is connected to the gate of the FET, and so the DC input current is assumed to be equal to zero. With the previous analysis, this configuration ensures that the logic principle of MOBILE is correct. The FETs connected between output and latch (M2, M3 in Fig. 7) work as transfer gates: when CLK falls to low, the transfer gates are cut off and the outputs remain unchanged. When CLK is high, due to the self-latching character of MOBILE, the output does not change even if the input changes. Therefore, the output only alters at the rising edge of the CLK.

The logic characteristics of the proposed DFF are shown in Table 3. It is a standard logic characteristic of an edge-triggered DFF. Compared with a CMOS edge-triggered DFF, which have eight two-input NAND gates, our DFF uses fewer components, a decrease to only a half. The characteristic that MOBILE can work as an inverter with self-latching is fully utilized.

We can construct a standard binary divider with two D-Flip-Flops and the block diagram is shown in Fig. 8. In this circuit, two DFFs are driven by two-phase clocks that are opposite each other. One DFF works as a master latch and the other as a slave latch. The reversal output of the slave latch is connected to the input of the master latch to offer feedback. At the rising edge of the clock, the master latch is sampling and the slave latch is holding. At the falling edge of

Table 3　Logic characteristics of an edge-triggered DFF

CLK	D	Q^{n+1}
1	X	Q^n
0	X	Q^n
↑	0	0
↑	1	1

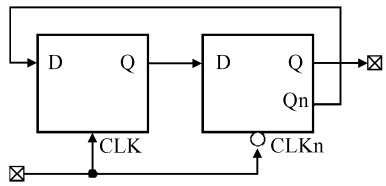

Fig. 8 Block diagram of a DFF binary divider

the clock, the master latch is keeping and the slave latch is sampling. So the output changes once every period of clock and a binary divide is realized. The SPICE verification is shown in Fig. 9.

For the V_{CLK} applied to MOBILE, the input resistor is not infinite and so an input current exists. Taking the static equivalent input impedance of MOBILE used for simulation as an example, the values of impedance are 123.7Ω at the points of intersection L1 and 780Ω at H1 in Fig. 3 by Ohm's law. Due to two-phase clocks required by our divider, if an inverter is integrated, either its output resistance should be decreased enough to avoid the output voltage being pulled down by the output current, or a clock buffer for inverting and amplifying is needed to create good coupling. The former method requires a FET with a very large W/L in the inverter, while the latter method will make the circuit much more complicated. A better solution is to diminish the emitter area of the RTD to at least one tenth in the manufacturing process, which will make the static equivalent input impedance larger than 1kΩ. This will make the problem become negligible. By estimation, an emitter area less than $2\mu m^2$ will be proper.

To solve the problem above, another protocol is proposed. Two FETs are added to the circuit. Their W/L is large enough that they can work as transfer gates. The circuit configuration is shown in Fig. 10. When they are turned on, the MOBILEs begin to work. Then the CLK is applied to the gate of the FET and the input resistance is large enough to couple well. Therefore, a simple inverter with a resistor load

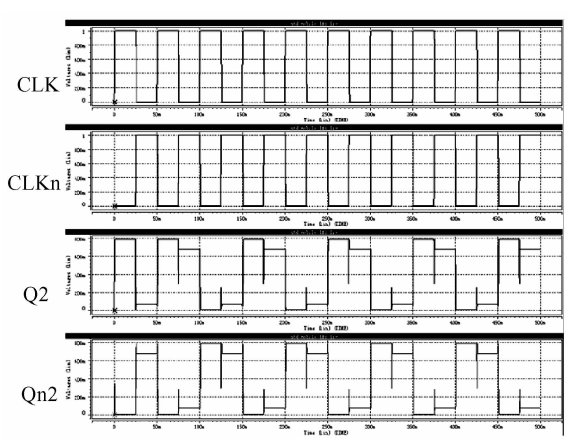

Fig. 9 Timing diagram of the DFF binary divider

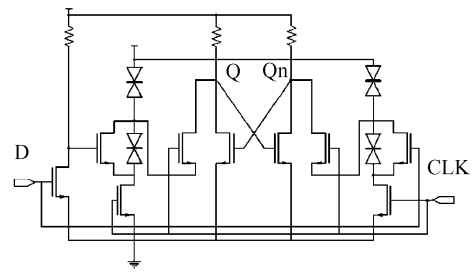

Fig. 10 A modified configuration of the edge-triggered DFF based on MOBILE

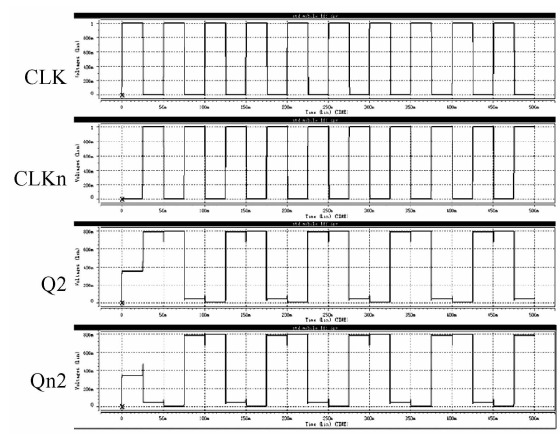

Fig. 11 Timing diagram of the modified DFF binary divider

or an active load will be proper for use. The costs are two transistors and an additional dc power supply. The SPICE verification of a binary divider composed of the DFF we modified is shown in Fig. 11.

3 Conclusion

We have designed two new types of edge-triggered DFFs based on resonant tunneling diodes integrated with FETs. These designs are used to construct a binary divider.

A DC model is used to verify the design by SPICE and the convergence is proven to be satisfactory. Compared with conventional CMOS SCFL technology, the complexity of the circuit is greatly simplified and low power consumption is achieved. We have realized the required MOBILE and the divider is under tape-out.

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一种利用共振隧穿二极管简化电路的分频器设计

杜　睿†　戴　杨　杨富华

（中国科学院半导体研究所 集成技术中心，北京　100083）

摘要：提出了一种基于共振隧穿二极管的新型边沿触发 D 触发器并将之用于构成二进制分频器.详细讨论了设计过程，用 SPICE 验证了电路的功能，并和已有的设计进行了比较.由于利用了共振隧穿二极管高度的非线性，同 CMOS 分频器相比，电路中元件的数量可以减少一半.

关键词：分频器；D 触发器；共振隧穿二极管；简化复杂度

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† 通信作者. Email: ddrr@semi.ac.cn

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