A Novel CMOS Current Mode Bandgap Reference*

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Abstract: A novel CMOS bandgap reference is presented. The output reference of this new current mode structure can be set to an arbitrary value above the bandgap voltage of silicon, avoiding offset in application. It also overcomes the systematic mismatch of conventional current mode bandgap references. The proposed bandgap reference has been implemented in UMC 0.18μm mixed mode technology. Under the supply voltage of 1.6V, the proposed bandgap reference provides an output reference of 1.45V and consumes 27μA of supply current. Using no curvature compensation, it can reach a temperature coefficient of 23ppm/℃ from 30 to 150℃ with a line regulation of 2.1mV/V from 1.6 to 3V and a PSRR of 40dB at DC frequency. The chip area of the bandgap reference (without pad) is 0.088mm^2.

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1 Introduction

High quality bandgap reference providing voltage or current independent of supply voltage and temperature is in great demand in analog and mixed mode integrated circuits design, such as data converters and DC-DC power converters.

Low supply voltage and high precision are two design trends for CMOS bandgap reference. To reduce the supply voltage, Jiang and Lee[1] used an operational trans-impedance amplifier to replace the operational trans-conductance amplifier in the bandgap reference. Banba, Leung, and Ker *et al*.[2~4] presented three different current mode structures which transform the addition of two voltages to an addition of two currents. Another advantage of these current mode bandgap references is that the output references can be adjusted to the proper value. To improve the precision, several high order curvature compensations are introduced. Leung *et al*.[5] developed a second-order curvature compensation using resistors with opposing temperature coefficients. Audy[6] further proposed a third order curvature compensation based on series and parallel combinations of two kinds of resistors. Malcovati *et al*.[7] proposed a new method, which generates a non-linear current to compensate the nonlinear V_{EB} of BJT.

For conventional bandgap reference, the output reference is a fixed value around 1.24V. In application, an operational amplifier (OPA) with voltage-voltage feedback is needed to amplify or attenuate the 1.24V bandgap voltage to the desired voltage reference. Because of the offset of CMOS OPA, although the bandgap reference is stable with temperature, the stability of the desired voltage reference is not very good.

Current mode bandgap references with arbitrary output references can solve this problem[2~4]. However, in these three current mode bandgap references, systematic mismatch is unavoidable, which will constrain the precision.

Although low supply voltage is a popular design, high supply voltage is also common in some high precision designs. Low supply voltage is not our goal in this work. The presented bandgap reference focuses on avoiding offset introduced by OPA in application and preventing systematic mismatch. The silicon verification in UMC 0.18μm mixed mode technology shows that under 1.6V voltage, the proposed bandgap reference can supply an arbitrary output reference above 1.24V (1.45V is adopted here as an example) with a temperature coefficient of 23ppm/℃ from 30 to 150℃.

2 Conventional bandgap references and their disadvantages

2.1 Conventional bandgap references with fixed output references and their disadvantages

A typical conventional CMOS bandgap reference

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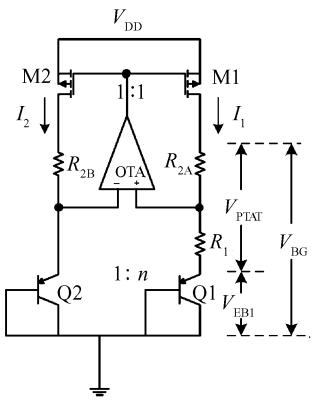

Fig. 1 A conventional bandgap reference with fixed output reference

circuit is shown in Fig. 1, where $R_{2A} = R_{2B} = R_2$. The output reference voltage is:

$$V_{BG} = V_{EB1} + \left(1 + \frac{R_2}{R_1}\right)\frac{KT}{q}\ln n \qquad (1)$$

where n is the ratio of the emitter area of Q1 and Q2. If the resistor ratio is proper, the second term in Eq. (1), which has a positive temperature coefficient, can cancel the negative temperature coefficient of V_{EB1}, leading to a fixed and stable output reference around 1.24V. However, 1.24V is often not our desired voltage reference, so an operational amplifier (OPA) with voltage-voltage feedback is needed to amplify or attenuate the 1.24V bandgap voltage to the desired voltage reference, as shown in Fig. 2. Taking into account the offset of the OPA, the desired reference voltage is:

$$V_{REF} = \frac{R_1 + R_2}{R_2}(V_{BG} - V_{OS}) \qquad (2)$$

The temperature coefficient of the V_{REF} is:

$$\frac{dV_{REF}}{dt} = \frac{R_1 + R_2}{R_2}\left(\frac{dV_{BG}}{dt} - \frac{dV_{OS}}{dt}\right) \qquad (3)$$

In CMOS technology, the input offset voltage is as high as 10mV and its temperature coefficient reaches $20\mu V/℃$. Although the temperature stability of the V_{BG} is very good, because of the offset voltage of the OPA, the temperature stability of the V_{REF} is much worse. So, a bandgap reference with an arbitrary output reference has the advantage of needing no OPA in

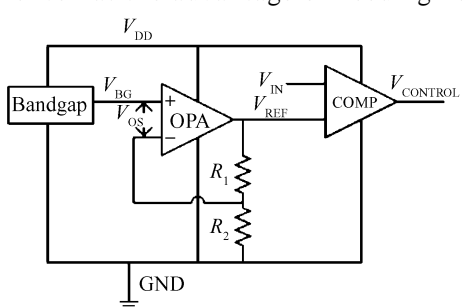

Fig. 2 Typical application of bandgap reference with fixed output reference

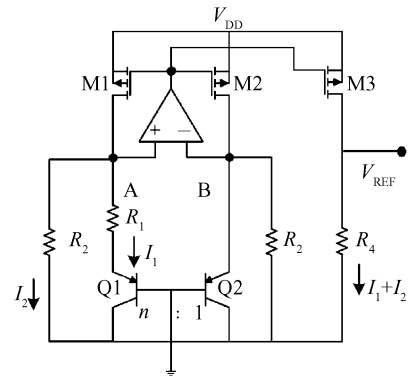

Fig. 3 A typical current mode bandgap reference

application.

2.2 Conventional current mode bandgap references and their disadvantages

In three current mode bandgap references, the output reference can be set to a special value[2~4]. One is shown in Fig. 3[2]. Unfortunately, systematic mismatch is found in this structure. The forward biased voltages of diodes and the voltages of nodes A and B are complementary-to-absolute-temperature (CTAT), leading to the proportional-to-absolute-temperature (PTAT) source-drain voltages of transistors M1 and M2. In UMC 0.18μm mixed mode technology, when temperature varies from -20 to 100℃, the source-drain voltages of transistors M1 and M2 increase 200mV. To some extent, the V_{REF} is independent of absolute temperature, which means the source-drain voltage of transistor M3 is also independent of absolute temperature. Comparing the source-drain voltages of transistors M1, M2, and M3, we find in the temperature range that the source-drain voltages of transistors M1, M2 are different from that of transistor M3 except for at one point, as shown in Fig. 4. Similar systematic mismatch also exists in the structures of Refs. [3,4].

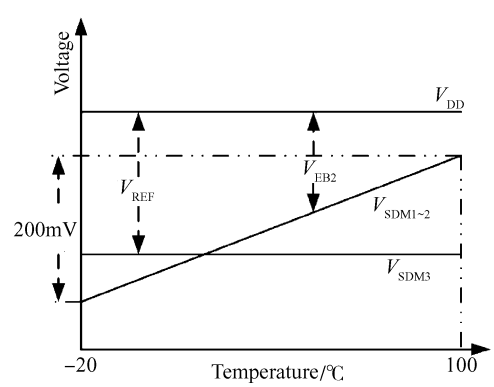

Fig. 4 Systematic mismatch of the current mode bandgap reference in Fig. 3

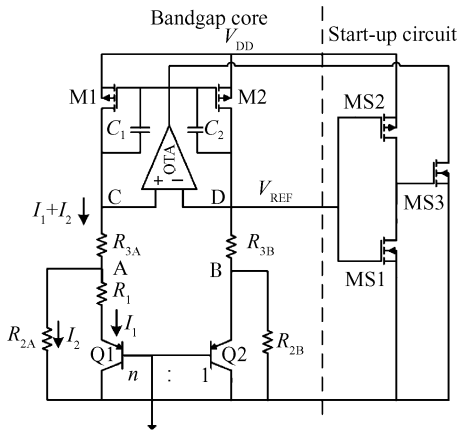

Fig. 5　Proposed current mode bandgap reference

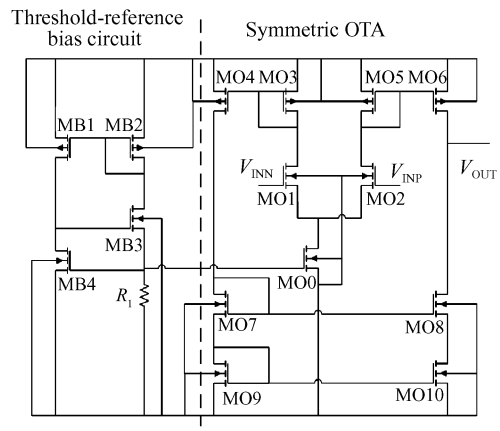

Fig. 6　Feedback OTA used in the circuit in Fig. 5

3　Proposed current mode bandgap reference

3.1　Novel current mode bandgap reference structure

The proposed current mode bandgap reference is shown in Fig. 5, where $R_{2A} = R_{2B} = R_2$, $R_{3A} = R_{3B} = R_3$. Because of the negative feedback loop formed by transistors M1, M2, and the feedback OTA, the voltages of nodes C and D are the same:

$$V_C = V_D \tag{4}$$

Because transistors M1 and M2 form a perfect current mirror, their currents are the same:

$$I_{M1} = I_{M2} \tag{5}$$

$$R_3 I_{M1} = R_3 I_{M2} \tag{6}$$

So, we can conclude that the voltages of nodes A and B are also the same:

$$V_A = V_B \tag{7}$$

The ΔV_{EB} between Q2 and Q1 is applied to R_1:

$$I_1 = \frac{\Delta V_{EB}}{R_1} \tag{8}$$

The current I_2 is proportional to V_{EB} of Q2:

$$I_2 = \frac{V_{EB2}}{R_2} \tag{9}$$

So the output reference V_{REF} can be written as:

$$V_{REF} = V_{EB2} + (I_1 + I_2)R_3 = V_{EB2} + \left(\frac{\Delta V_{EB}}{R_1} + \frac{V_{EB2}}{R_2}\right)R_3$$

$$= V_{EB2}\left(1 + \frac{R_3}{R_2}\right) + \Delta V_{EB}\frac{R_3}{R_1} \tag{10}$$

V_{EB} to some degree is CTAT while ΔV_{EB} is PTAT[5]:

$$\Delta V_{EB} = V_T \ln n = \frac{KT \ln n}{q} \tag{11}$$

$$V_{EB} = V_{BG}(T_r) + \frac{T}{T_r}[V_{EB}(T_r) - V_{BG}(T_r)] + (\eta - m)\frac{kT}{q}\ln\frac{T_r}{T} \tag{12}$$

where T is the absolute temperature, T_r is a reference temperature, V_{BG} is the bandgap voltage of silicon, η is a constant depending on doping level, and m is a constant depending on the temperature character of emitter current in BJT. If the resistors ratio satisfies the constraint described in Eq. (13), V_{REF} is approximately independent of temperature.

$$\left(1 + \frac{R_3}{R_2}\right)\Big/\frac{R_3}{R_1} = \frac{\mathrm{d}\Delta V_{EB}}{\mathrm{d}t}\Big/\frac{\mathrm{d}V_{EB2}}{\mathrm{d}t} \tag{13}$$

With Eqs. (10) and (13), a flexible and temperature stable reference voltage can be achieved. Because $(1 + R_3/R_2)$ is larger than 1, the V_{REF} is larger than the bandgap voltage of silicon.

3.2　Feedback OTA

The feedback OTA is shown in Fig. 6. To stabilize the gain of the OTA, a threshold-referenced bias circuit is used to bias the feedback OTA[8]. The bias current can be written as:

$$I = \frac{V_{th}}{R_1} + \frac{L}{R_1^2 \mu_n C_{ox} W} + \frac{1}{R_1}\sqrt{\frac{2V_{th}L}{R_1\mu_n C_{ox} W} + \frac{L^2}{(R_1\mu_n C_{ox} W)^2}} \tag{14}$$

where μ_n is the mobility of electrons and C_{ox} is the oxide capacitance; V_{th}, W, and L are the threshold voltage, width, and length of transistor MB4, respectively. The bias current is independent of supply voltage. To reduce the input offset voltage of the OTA, a symmetric OTA structure is chosen. The cascode current mirror is applied to increase the DC gain.

Simulation shows that the DC gain is 65dB, the GBW is 800kHz, and the phase margin is 85° with a load of 40pF. Although the feedback OTA is a one-stage amplifier, the negative feedback loop in the circuit in Fig. 5 is two-stage. To avoid oscillation after power on, two phase-compensation capacitances C_1 and C_2 are added to this bandgap circuit.

3.3　Start-up circuit

To prevent the bandgap circuit from working on

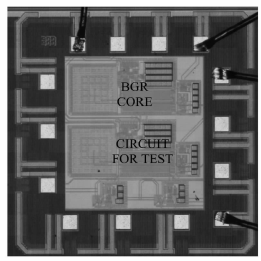

Fig. 7 Micrograph of the proposed bandgap reference die

the zero working point, a start-up circuit formed by MS1 ~ MS3 is needed. When the bandgap circuit works on zero working point, V_{REF} is zero. The gate voltage of MS3 is V_{DD}, which drives MS3 on, the output of the OTA is then pulled down, and the circuit starts up to the normal working point. When the circuit works on the normal working point, assuming proper sizes for MS1 and MS2, the gate voltage of MS3 is lower than the threshold voltage, cutting off MS3 and the start-up circuit does not affect the working state of the bandgap circuit.

4 Measurement results

The presented bandgap reference has been fabricated in a UMC 0.18μm mixed-mode process. The micrograph of the die is shown in Fig. 7. To save chip area, more than one core circuits are put into this die to share the power ring and ground ring. For better analysis, a core circuit for testing with some accessible inner nodes has also been fabricated. Each bandgap circuit occupies 0.088mm^2 of chip area. Figure 8 shows the measurement results of the dependence of the output reference voltage on temperature under different supply voltages. The measurement temperature range is from 30 to 150℃. With supply voltages of 1.6 and 1.8V, the bandgap reference reaches its best performance: a temperature coefficient of 23ppm/℃. When the supply voltage increases from 2.0 to 2.5V, the temperature coefficient of the reference increases from 34 to 40ppm/℃. The worst case is 46ppm/℃ when the supply voltage is 3.0V. The

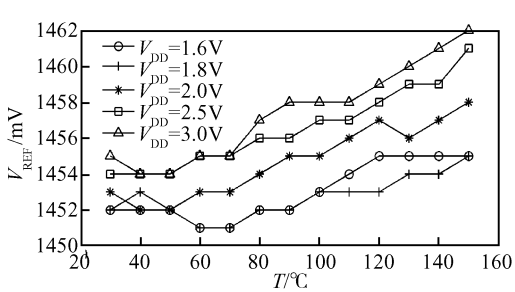

Fig. 8 Measurement results of dependence of the output reference voltage on temperature under different supply voltages

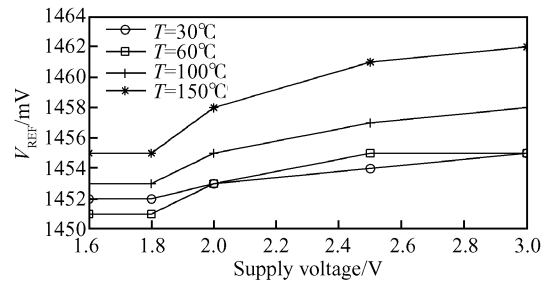

Fig. 9 Measurement results of dependence of the output reference voltage on supply voltage under different temperatures

main reasons that output reference varies with temperature are the mismatch between resistors, the non-zero temperature coefficient of the resistor, and the input offset voltage of the feedback OTA. When supply voltage is higher than 2.0V, the gain of the feedback loop decreases, causing a monotonically increasing output reference. The measurement results of dependence of the output reference voltage on supply voltage under different temperatures are shown in Fig. 9. The measurement supply voltage range is from 1.6 to 3V. We calculated that the line regulations are 2.1, 2.6, 3.6, and 5mV/V respectively under temperatures of 30, 60, 100, and 150℃. If supply voltage is higher than 3.0V or lower than 1.6V, the gain of the feedback OTA decreases sharply. Without a deep negative feedback loop, the output reference voltage varies greatly. With the supply voltage of 1.6V, the supply current is about 27μA and the power supply rejection ratio is about −40dB at DC frequency. To better evaluate this work, a comparison with other current mode bandgap references is listed in Table 1.

5 Conclusion

A novel CMOS bandgap reference, which can provide an arbitrary output reference voltage above 1.24V, has been presented in this paper. Systematic mismatch in conventional current mode structures and offset in application are avoided in this work. Measurement results show that with a supply voltage of

Table 1 Comparison of current mode bandgap references

	This work	Ref.[2]	Ref.[3]	Ref.[4]
Process	0.18μm CMOS	0.4μm Native	0.68μm CMOS	0.25μm CMOS
V/V	1.6	2.2	0.98	0.85
I/μA	27	2.2	18	28
V_{REF}/mV	1450	518	605	238
V_{REF} limitation	>1.24V	no	no	<1.24V
TC/(ppm/℃)	23	116	15	58
LR/(mV/V)	2.1	1.1	-	>10
PSRR	40dB@DC	-	44dB@10kHz	33dB@10kHz
Area/mm^2	0.088	0.1	0.24	0.019

1.6V, the proposed bandgap reference provides an output reference voltage of 1.45V with a temperature coefficient of 23ppm/℃ from 30 to 150℃. The supply current is 27μA and PSRR is 40dB at DC frequency. In the supply voltage range from 1.6 to 3.0V, the line regulation is 2.1mV/V at room temperature. To achieve better temperature stability, feedback OTA with higher gain and common-centroid layout are needed, and some high order curvature compensation can also be applied to this structure.

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一个新型 CMOS 电流模带隙基准源*

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摘要： 介绍了一个新型电流模带隙基准源，该带隙基准源的输出基准可以设计为任意大于硅材料的带隙电压(1.25V)的电压，避免在应用中使用运算放大器进行基准电压放大. 同时该结构消除了传统电流模带隙基准源的系统失调. 该带隙基准源已通过 UMC 0.18μm 混合信号工艺验证. 在 1.6V 电源电压下，该带隙基准源输出 1.45V 的基准电压，同时消耗 27μA 的电流. 在不采用曲率补偿的情况下，输出基准的温度系数在 30℃ 到 150℃ 的温度范围内可以达到 23ppm/℃. 在电源电压从 1.6 变化到 3V 的情况下，带隙基准源的输入电压调整率为 2.1mV/V. 该带隙基准源在低频(10Hz)的电源电压抑制比为 40dB. 芯片面积(不包括 Pads)为 0.088mm^2.

关键词： CMOS；带隙基准源；电流模

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