Gate Annealing of an Enhancement-Mode InGaP/AlGaAs/InGaAs PHEMT*

Li Ming†, Zhang Haiying, Xu Jingbo, Li Xiao, Liu Liang, and Fu Xiaojun

(*Institute of Microelectronics, Chinese Academy of Sciences, Beijing* 100029, *China*)

Abstract: For enhancement-mode InGaP/AlGaAs/InGaAs PHEMTs, gate annealing is conducted between gate structures of Ti/Pt/Au and Pt/Ti/Pt/Au. Comparison is made after thermal annealing and an optimum annealing process is obtained. Using the structure of Ti/Pt/Au, about a 200mV positive shift of threshold voltage is achieved by thermal annealing at 320℃ for 40min in N_2 ambient. Finally, a stable and consistent enhancement-mode PHEMT is produced successfully with higher threshold voltage.

Key words: enhancement-mode; InGaP/AlGaAs/InGaAs PHEMT; anneal; threshold voltage; ring oscillator
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1 Introduction

Recently, extensive research has focused on PHEMTs with low power consumption and low supply-voltage, which can be achieved with direct-coupled FET logic (DCFL) that requires both E- and D-mode devices. DCFL is one of the best logic technologies for large-scale (LSI) digital circuit applications because of its advantages over other technologies such as buffer FET logic (BFL) and source-coupled FET logic (SCFL). The advantages of DCFL include low power consumption, high speed, design simplicity (no voltage level shift), and the need for only one positive power supply[1~3].

However, the main disadvantage of DCFL is its low noise margin (V_m) (inherent limitations of barrier altitude), which is sensitive to threshold voltage variation. On the same wafer, the V_{th} of E-mode devices always swings around 0, disabling DCFL if $V_{th}<0$[4]. Therefore, ensuring E-mode PHEMT's positive threshold voltage is the key for fabrication of DCFL ICs.

Gate annealing is an effective method to raise the V_{th} and already been reported extensively internationally[5], but most reports focus on Pt/Ti/Pt/Au structures instead of Ti/Pt/Au. In this paper, by the comparison between the two metal structures, we present a practical gate annealing process to solve the $V_{th}<0$ problem. Finally, we achieve stable and consistent E-mode devices with $V_{th}>0$. A nine-stage ring oscillator based on DCFL has been made successfully, which is proof for our gate annealing technology.

2 Experiment

The structure of epitaxial materials is shown in Fig. 1. With 1.0μm GaAs E/D PHEMT technology from the Institute of Microelectronics of Chinese Academy of Sciences, device fabrication started with simultaneous mesa-isolation for the E- and D-mode devices using a conventional wet etching process. Ohmic contacts were formed using a new six-layer ohmic system (Ni/Ge/Au/Ge/Ni/Au). To eliminate the influence of the thermal anneal on the D-mode PHEMTs, a two-step process[6] for the E-mode and D-mode PHEMTs was chosen for the fabrication of the gate. The E-mode gate was fabricated first, and after a gate annealing process in N_2 ambient, the D-mode gate was produced.

Cap (n^+-GaAs)
D-mode barrier (i-$In_{0.5}Ga_{0.5}P$)
E-mode barrier (i-$Al_{0.22}Ga_{0.78}As$)
Planar Si-doped (δ doped)
Spacer (i-$Al_{0.22}Ga_{0.78}As$)
Channel ($In_{0.2}Ga_{0.8}As$)
Buffer (i-$Al_{0.22}Ga_{0.78}As$)
Superlattice AlGaAs/GaAs
Semi-insulating substrate (GaAs)

Fig. 1 Structure of epitaxial materials

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† Corresponding author. Email: liming@ime.ac.cn
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Metal 1		Metal 2	
Au	220nm	Au	220nm
Pt	80nm	Pt	80nm
Ti	50nm	Ti	50nm
n^+ GaAs cap		Pt	4nm
		n^+ GaAs cap	

Fig. 2 Two different gate metal structures

Figure 2 shows two different gate structures. Metal 1 includes Ti (50nm), Pt (80nm), and Au (220nm) from bottom to top, and metal 2 includes Pt (4nm), Ti (50nm), Pt(80nm), and Au (220nm) from bottom to top. Two metal structures are common nowadays. For preventing the degeneration of epitaxy and 2DEG at a high temperature, 320℃ was chosen as an experiment temperature. The annealing time was 40min.

Usually, the V_{th} of HEMT can be expressed as Eq. (1)[7], where V_{th} is the threshold voltage, Φ_b is the Schottky-barrier, ΔE_c is the difference of conduct-band between AlGaAs and InGaAs, N is the Si-doped concentration in Schottky-barrier, ε is the permittivity of Schottky-barrier, and D is the distance between channel and gate metal.

$$V_{th} = \Phi_b - \frac{\Delta E_c}{q} - \frac{qN_d D}{\varepsilon} \quad (1)$$

Therefore, higher Φ_b, lower ΔE_c, N, and D are effective methods to achieve higher threshold voltage. Through high temperature annealing, Ti of metal 1 and metal 2 diffuses into the barrier (AlGaAs), equivalent to the lower D in Eq. (1), and a positive shift of V_{th} is achieved.

3 Results and analysis

DC measurements were performed using a HP4155 semiconductor parameter analyzer. For metal structure 1 (Ti/Pt/Au), the drain current-voltage (I_D-V_{DS}) for 1 × 100μm E-PHEMTs before ('pre-anneal') and after ('post-anneal') the final gate anneal are both shown in Fig. 3. The maximum drain current of 323mA/mm (pre-anneal) and 304mA/mm (post-anneal) occur at V_{gs} = 0.9V and V_{ds} = 2V, showing the normally-off operation of the devices. The enhancement-mode nature of the devices is clearly seen in the DC transfer characteristics measured at V_{ds} = 2V, as shown in Fig. 3. Prior to the gate anneal, E-PHEMT devices exhibit a V_{th} of −0.02 V. After the gate anneal, the V_{th} increased to 0.2V while the I_{dss} is lowered slightly to 304mA/mm.

On the other hand, for metal structure 2 (Pt/Ti/Pt/Au), the drain current-voltage before ('pre-anneal') and after ('post-anneal') the final gate anneal are shown both in Fig. 4. The maximum drain current

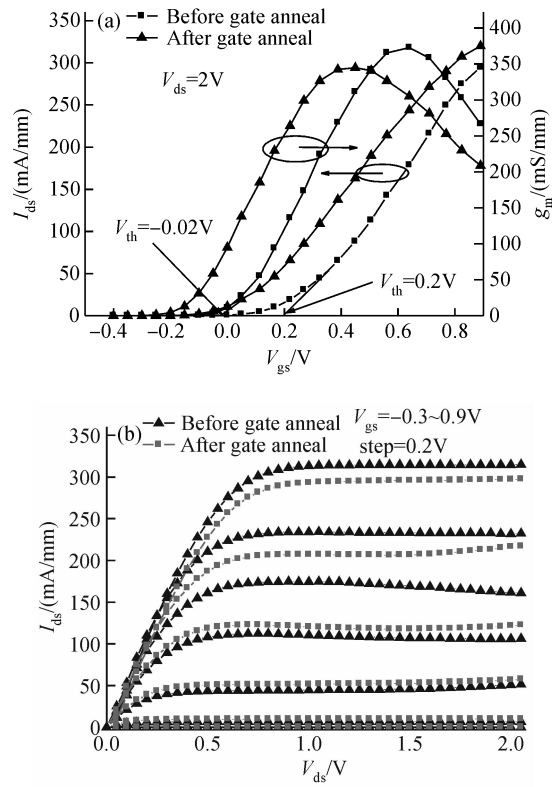

Fig. 3 Transfer characteristics & DC characteristics of 1μm E-PHEMT with Ti/Pt/Au gate (before and after gate anneal)

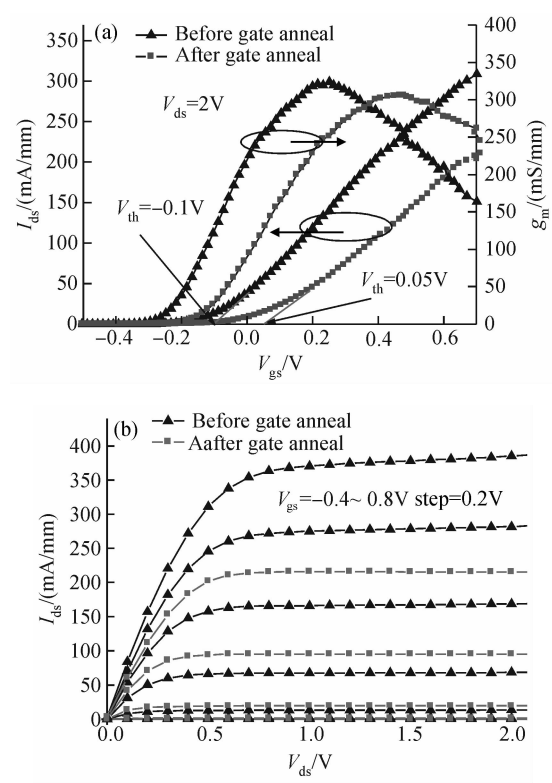

Fig. 4 Transfer characteristics & DC characteristics of 1μm E-PHEMT with Pt/Ti/Pt/Au gate (before and after gate anneal)

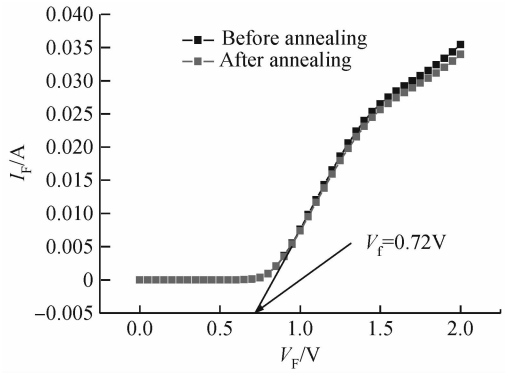

Fig. 5　*I-V* characteristic curve of gate Schottky barrier diode

of 334mA/mm (pre-anneal) and 210mA/mm (post-anneal) occur at $V_{gs}=0.7$V and $V_{ds}=2$V. The V_{th} of E-PHEMTs increased from −0.1V (pre-anneal) to 0.05V (post-anneal), while the I_{dss} is lowered tremendously to about 210mA/mm.

From the experimental results for the two kinds of metal structures after the gate annealing, threshold voltage (V_{th}) has improved significantly. The changes in these characteristics are attributed to a decrease in D between the metal gate and the InGaAs[8]. As shown in Fig. 3, the current of the metal structure 1 has no obvious decline after annealing, which indicates this anneal had little impact on Ohmic contacts, without degradation of 2DEG. However, Figure 4 also shows the current of the metal structure 2 has larger decline after annealing, which indicates the gate anneal had greater impact on the Ohmic contacts of our E-PHEMTs, with serious degradation of 2DEG[9].

Figure 5 is *I-V* characteristic curve of the gate Schottky barrier diode of metal structure 1 before and after annealing. The figure shows that the Schottky barrier almost has no deterioration after annealing at 320℃ and the Schottky barrier height remains at 0.7V. Finally, after comprehensive consideration of stability, Ti/Pt/Au was chosen as the metal structure for our E-mode devices.

Figure 6 is the nine-stages ring oscillator with the

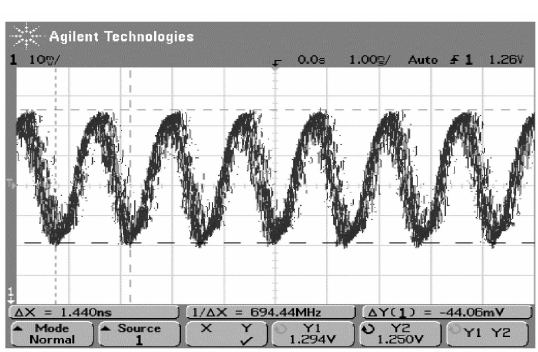

Fig. 6　Nine-stages ring oscillator

technology line of 1.0μm GaAs PHEMTs, including nine-stages DCFL inverters and a three-stage DCFL output buffer. From Fig. 6, when the input voltage is 1.5V, the central vibration frequency is 694MHz, the amplitude is 44mV, and the gate delay is 80.05ps. The ring oscillator produced by the gate anneal process ensures the threshold voltages (V_{th}) of the enhancement-mode devices are always above 0, which is a solid foundation for our latest production of E/D circuits.

4　Conclusion

Gate annealing was conducted to compare gate structures of Ti/Pt/Au and Pt/Ti/Pt/Au, and optimized annealing technology for the gate metal of PHEMT was obtained. Using a Ti/Pt/Au structure, the threshold voltage is moved positively to 200mV through annealing at 320℃ for 40min. Finally, stable and consistent enhancement-mode PHEMT devices has been made successfully, ensuring the threshold voltage (V_{th}) of enhancement-mode devices is always above 0. The ring oscillator produced proves that the annealing process is an effective way to make high-yield E-mode production and the DCFL circuit. These devices are suitable for integration with D-HEMTs for high performance digital circuitry applications.

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增强型 InGaP/AlGaAs/InGaAs PHEMT 栅退火工艺*

黎 明† 张海英 徐静波 李 潇 刘 亮 付晓君

(中国科学院微电子研究所，北京 100029)

摘要：针对 InGaP/AlGaAs/InGaAs PHEMT 器件，进行了 Ti/Pt/Au 和 Pt/Ti/Pt/Au 两种栅金属结构的退火实验，通过实验研究比较，得到了更适用于增强型器件的退火工艺，利用 Ti/Pt/Au 结构，在 320℃退火 40min，使器件阈值电压正向移动大约 200mV，从而成功制作了高成品率的稳定一致的增强型器件，保证了增强型器件阈值电压在零以上.

关键词：增强型 InGaP/AlGaAs/InGaAs PHEMT；退火；阈值电压；环形振荡器

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† 通信作者. Email：liming@ime.ac.cn

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