A Capacitor-Free CMOS Low-Dropout Regulator for System-on-Chip Application*

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Abstract: A stable CMOS low drop-out regulator without an off-chip capacitor for system-on-chip application is presented. By using an on-chip pole splitting technique and an on-chip pole-zero canceling technique, high stability is achieved without an off-chip capacitor. The chip was implemented in CSMC's 0.5μm CMOS technology and the die area is 600μm $\times$480μm. The error of the output voltage due to line variation is less than $\pm$0.21%, and the quiescent current is 39.8μA. The power supply rejection ratio at 100kHz is $-$33.9dB, and the output noise spectral densities at 100Hz and 100kHz are 1.65 and 0.89μV/$\sqrt{\text{Hz}}$, respectively.

Key words: low-dropout regulator; pole splitting; pole-zero cancelling; capacitor-free
EEACC: 1210; 2570
CLC number: TN432 **Document code**: A **Article ID**: 0253-4177(2008)08-1507-04

1 Introduction

Low-dropout voltage regulators (LDO) have demonstrated low noise, high-accuracy, and fast-response. Therefore, they are widely used. Portable electronic equipment including cellular telephones and laptop computers increase the need for efficient voltage regulation to prolong battery life. On-chip and local LDOs are used to power up sub-blocks of a system individually, which can significantly reduce crosstalk, improve the voltage regulation, and eliminate load-transient voltage spikes from the bond wire inductances. In addition, system-on-chip designs with on-chip and local LDO can significantly reduce both board space and external pins.

Researchers have proposed several approaches to improve the performance of LDOs. Fan *et al*. integrated a foldback current limiter into the error amplifier[1], which makes a special current limiting circuit unnecessary. Gupta *et al*. realized an LDO with a high power supply rejection ratio (PSRR) over a broad frequency spectrum[2] using an nMOS transistor to cascade a pMOS pass transistor. Rincon-Mora *et al*. discussed a way to optimize the pole-zero configuration[3] and proposed a Miller-compensation scheme to further improve the LDO stability[4]. Pedro *et al*. placed a MOS transistor in parallel with a resistor in the feedback network[5] to make the output voltage adjustable.

These works have effectively improved the performance of drop-out, quiescent current, PSRR, stability, and applicability. However, the off-chip capacitor with certain equivalent series resistance (ESR), which is the key factor for stability and high LDO performance, was not eliminated. This off-chip capacitor with ESR must be strictly chosen and requires additional pins and board space. Thus it is the main obstacle to a fully integrated LDO in system-on-chip design. To eliminate the off-chip capacitor, Leung *et al*. have recently proposed a damping-factor-control frequency compensation scheme[6]. However, this scheme is too complicated to work well under all process corners. In this paper, we first propose another approach to sustain LDO stability without an off-chip capacitor and then discuss the stability. Finally, we present the measurement results for important specifications such as line and load regulation, as well as line transient response.

2 Circuit design and theoretical analysis

A classical CMOS LDO is composed of an error amplifier, a pMOS pass transistor, a feedback resistive network and a voltage reference. The LDO of such a structure has two poles under unity-gain frequency (UGF). The high stability of the classical LDO is realized by off-chip pole-zero compensation, which is achieved by an off-chip capacitor along with its equivalent series resistance[6]. This implies that the classical LDO cannot be integrated effectively into system-on-chip design since it requires a large capacitor for stability. Therefore, we introduce an on-chip fre-

* Project supported by the National Natural Science Foundation of China (No. 90707005)
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Received 23 January 2008, revised manuscript received 11 March 2008

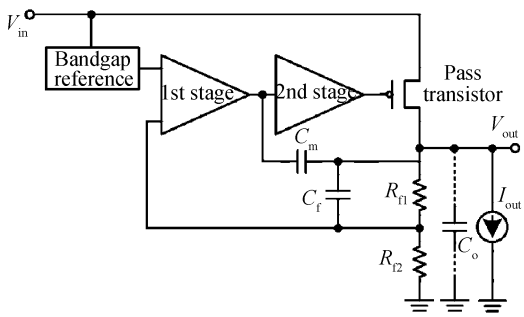

Fig. 1 Structure of the proposed LDO

quency compensation scheme to solve this problem.

2.1 Circuit structure

The structure of the proposed LDO is shown in Fig. 1. It is composed of a high-gain error amplifier, a high-gain high-output-swing stage, a pMOS pass transistor working in the linear region at dropout, a feedback resistive network, a CMOS bandgap reference, and two on-chip capacitors C_m and C_f for frequency compensation. The capacitance of the load capacitor C_O is very low and mainly from the parasitic capacitor of the output wire and pad.

The resulting structure is as a three-stage amplifier driving a capacitive load and a current load. The pMOS pass transistor with a certain output resistance can be taken as the third gain stage. The channel length and width of the pass transistor are 0.55 and 3000μm, respectively. Rincon-Mora placed a capacitor between the input and the output of the second stage[4] to implement frequency compensation. Because the gain of a single stage cannot be very high, the Miller compensation effect is not significant enough. Here, the gain of the third stage can be used to enhance the Miller compensation effect. Therefore, the compensation capacitor C_m is placed between the input of the second stage and the output of the third stage. So the dominant pole p_1 in Fig. 2 decreases and the pole splitting effect is achieved.

Due to the pole splitting effect, the open-loop bandwidth decreases and the transient performance

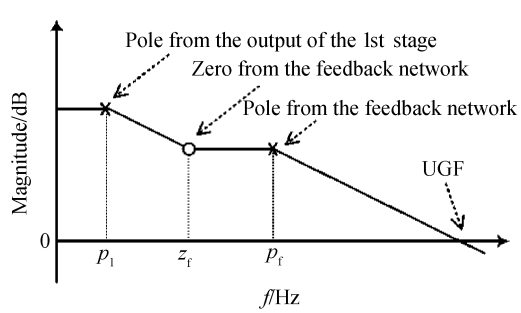

Fig. 2 Magnitude plot of the proposed LDO

degrades. To get a fast line and load transient response and minimize the overshoots, another compensation capacitor C_f is used in parallel with resistor R_{f1} in a feedback network to provide a high frequency bypass path for the loop gain[7]. This capacitor creates a pole-zero pair in the open-loop transfer function as follows:

$$H_f(s) = \frac{R_{f2}}{R_{f1}+R_{f2}} \times \frac{1+sC_fR_{f1}}{1+sC_f(R_{f1} /\!/ R_{f2})} \quad (1)$$

This analysis shows that one pole p_f and one zero z_f are created. These two poles are given by

$$p_f = \frac{1+R_{f1}/R_{f2}}{C_fR_{f1}} \quad (2)$$

$$z_f = \frac{1}{C_fR_{f1}} \quad (3)$$

respectively. The frequency of z_f is lower than the frequency of p_f. For a better compensation effect, R_{f2} should be much smaller than R_{f1}. This implies that the required reference voltage should be much smaller than the LDO output voltage. The zero created by the feedback network can also improve the PSRR performance and guarantee the stability of the LDO with an off-chip capacitor.

2.2 Stability analysis

Since there are four high impedance nodes in the structure illustrated in Fig. 1, there are four poles. The final open-loop transfer function, based on a small signal equivalent circuit, is given by

$$H(s) = \frac{A_{DC}\left(1+\frac{s}{z_f}\right)}{1+s\frac{C_g}{g_{m2}}+s^2\frac{C_gC_O}{g_{m2}g_{mp}}} \times \frac{1}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_f}\right)} \quad (4)$$

in which

$$A_{DC} = g_{m1}r_{O1}g_{m2}r_{O2}g_{mp}r_{op}\frac{R_{f2}}{R_{f1}+R_{f2}} \quad (5)$$

$$p_1 = \frac{1}{g_{m2}r_{O2}g_{mp}r_{op}C_mr_{O1}} \quad (6)$$

Here, A_{DC} is the low-frequency gain, p_1 is the dominant pole, and C_g and g_{mp} are the gate capacitance and the transconductance of the pass transistor, respectively. g_{m1}, g_{m2}, r_{O1}, r_{O2}, and r_{op} are the transconductances of the first stage and the second stage, the output resistances of the first stage and the second stage, and the output resistance of pass transistor, respectively.

We compare the second-order function in Eq. (4) with a standard second-order function given by

$$F(s) = 1+s\frac{2\zeta}{p_c}+\left(\frac{s}{p_c}\right)^2 \quad (7)$$

where ζ is the damping factor and p_c is the frequency of complex poles. Therefore, p_c and ζ are given by

$$p_c = \sqrt{\frac{g_{m2}g_{mp}}{C_gC_O}} \quad (8)$$

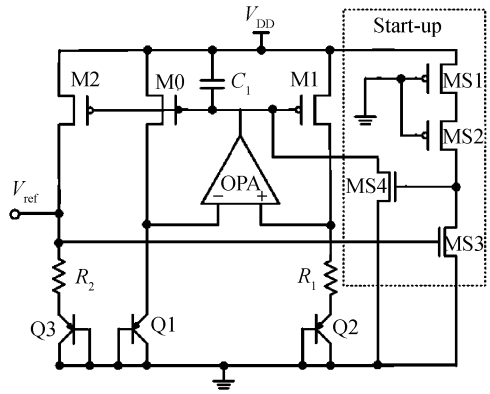

Fig. 3　Diagram of CMOS voltage reference

$$\zeta = \frac{1}{2}\sqrt{\frac{C_g g_{mp}}{g_{m2} C_O}} \tag{9}$$

The damping factor is critical to the LDO stability. If the damping factor is too small, a frequency peak occurs and pole-zero cancellation by separated zeros is not effective. If the damping factor is too large, the complex poles become separate poles and the loop bandwidth will degrade.

Since g_{mp} is large and C_O is very small, p_c is higher than UGF. Therefore, as illustrated in Fig. 2, there are two poles p_1, p_f and one zero z_f under UGF. So the phase margin is 90° in theory. Simulation results show that the phase margin ranges from 86° to 92° under five process corners, ±10% supply voltage variation, and temperature from −25 to +80℃.

When the LDO works with a large load capacitor, the frequency of complex poles goes low according to Eq. (8), and the UGF goes below p_f. Since the large load capacitor and its ESR creates a zero z_e, there are three poles (p_1 and two complex poles) and two zeros (z_f, z_e) under UGF. Therefore, the LDO is also stable with a large load capacitor.

2.3　Bandgap reference

The diagram of the bandgap voltage reference in CMOS technology is shown in Fig. 3. Here, the pnp transistor is realized with the vertical parasitic p-n junction in CMOS technology. The output reference voltage is given by

$$V_{ref} = v_{be3} + 2.77 V_T \frac{R_2}{R_1} \tag{10}$$

in which, v_{be3} has a negative temperature coefficient and V_T has a positive temperature coefficient. Choosing an appropriate value for R_1 and R_2 achieves zero temperature coefficient for V_{ref}.

An important issue in supply-independent biasing is the existence of a degenerate bias point[8]. In the circuit shown in Fig. 3, MOS transistors M0, M1, M2 carry zero current when the supply is turned on and may remain off indefinitely because the loop can supply a zero current in every branch. To solve this problem, a start-up circuit is drives the bandgap reference out of the degenerate bias point when the supply is turned on.

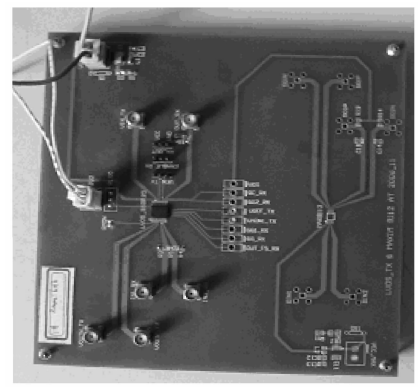

Fig. 4　Test board with packaged chip

3　Fabrication and measurements

The LDO has been implemented in standard 0.5μm CMOS technology from CSMC (Wuxi, China). The die area (not including pads) is 600μm × 480μm. The chip was tested without an off-chip capacitor and a photo of the test board is shown in Fig. 4.

The measured line regulation with different load currents is given in Fig. 5. As illustrated in the figure, the LDO is capable of operating from 4 to 7V, which covers a wide range of the typical battery voltage. A drop-out voltage of 200mV at a 40mA load current is achieved. The quiescent current is 39.8μA, which is sufficiently low for typical low-power applications. The line transient response of the supply voltage from 4.5 to 5.5V and the load transient response of load current from 1 to 40mA are also measured, and the results show that no oscillation occurs. The step response of the supply voltage from 0 to 5V is shown in Fig. 6. The figure indicates that the setup time of the output reference voltage is about 8ms. The performance of the LDO is summarized in Table 1.

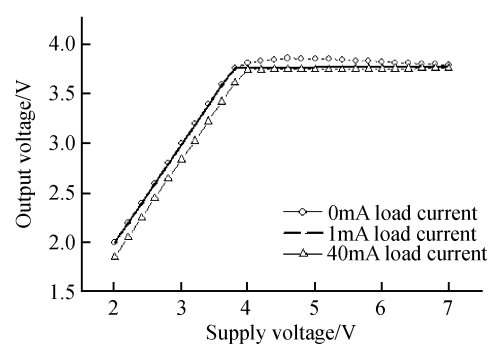

Fig. 5　Output voltage with respect to input voltage with different load currents

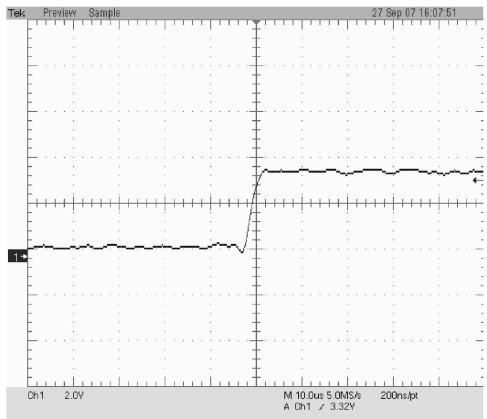

Fig. 6 Measured line transient response when the supply voltage changes from 0 to 5V

Table 1 Performance summary

Technology	0.5μm CMOS
Chip area (not including pads)	600μm×480μm
Quiescent current	39.8μA
Drop-out voltage	200mV
Preset output voltage	3.8V
Line regulation	4.6mV/V
Load regulation	0.43mV/mA
PSRR	−73.7dB @ 100Hz −33.9dB @ 100kHz
Output noise spectral density	1.65μV/$\sqrt{\text{Hz}}$ @ 100Hz 0.89μV/$\sqrt{\text{Hz}}$@ 100kHz

4 Conclusion

In this paper, a capacitor-free CMOS low-dropout regulator for system-on-chip design is designed and implemented in CSMC 0.5μm CMOS technology. The on-chip pole splitting technique and on-chip pole-zero cancelling technique are used to achieve high stability without an off-chip capacitor. This LDO also features high PSRR and low output noise spectral density.

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面向片上系统的无片外电容 CMOS 低压差稳压器*

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摘要：提出了一种面向片上系统、不依赖片外电容的 CMOS 低压差稳压器. 通过采用片上极点分离技术和片上零极点抵消技术，保证了没有片外电容情况下低压差稳压器的稳定性. 芯片通过华润上华 0.5μm CMOS 工艺进行了流片. 芯片核心区域(不包括焊盘)尺寸为 600μm×480μm. 输入电压变化造成的输出电压变化偏差在±0.21%以内. 静态电流为 39.8μA. 10kHz 处的电源抑制比为 −34dB. 100Hz 和 100kHz 处的输出噪声电流谱密度分别为 1.65 和 0.89μV/$\sqrt{\text{Hz}}$.

关键词：低压差稳压器；极点分离；零极点抵消；无片外电容
EEACC：1210；2570
中图分类号：TN432 **文献标识码**：A **文章编号**：0253-4177(2008)08-1507-04

* 国家自然科学基金资助项目(批准号：90707005)
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2008-01-23 收到，2008-03-11 定稿