Research and Design of an On-Chip High Efficiency Dual-Output Charge Pump*

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Abstract: To meet the demands for different supply voltage levels on SOC required by digital modules like CPU core and analog modules, a novel dual-output charge pump is proposed. The charge pump can output a step-up and a step-down voltage simultaneously with a high driving capability. The multiple gain pair technique was introduced to enhance its efficiency. The proposed co-use technology for capacitors and switch arrays reduced its cost. The charge pump was designed and fabricated in a TSMC 0.35μm mixed-signal CMOS process. A group of analytical equations were derived to model its static characteristics. A state-space model was derived to describe its small-signal dynamic behavior. Analytical predictions were verified by Spectre simulation and testing. The consistency of simulated results as well as test results with analytical predictions demonstrated the high precision of the derived analytical equations and the developed models.

Key words: charge pump; dual output; co-use technology; multi-gains
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1 Introduction

In modern integrated circuit (IC) design, processor and other digital modules are usually required to be integrated onto a chip together with analog modules to constitute a system on a chip (SOC). In such cases, very low supply voltages down to 1V are demanded by the processor and digital modules[1,2], while power supply voltages as high as 3.3 or 5V[3] are demanded by the analog modules such as amplifiers. Thus, on-chip power modules capable of providing two or more supply voltage levels are required by SOC, which has been recently applied to various portable products. Due to these demands, besides multi-level output and high-efficiency, low-cost and feasibility of integration are also requested for such power modules[4]. Research on high-efficiency multi-rail power supplies has aroused the interests of modern IC designers.

An inductor is necessary in traditional step-up/down switching power supplies, which is huge in volume, costly, and has weak immunity to electro magnetic interference (EMI). Meanwhile, a low dropout regulator (LDO) is proven to be a low efficiency solution since the voltage drop will give rise to extra power dissipation[5], especially when a large voltage difference exists between its input and output terminals. Therefore, a switched capacitor (SC) DC-DC converter (charge pump) becomes a good choice for such applications and has received more attention due to its low cost, good immunity to EMI, and high efficiency, which is applicable to a high-efficiency multi-rail power supply.

Recently, charge pumps have been adopted to constitute some system power supplies[6~8]. However, the reported work usually provides just one rail output[9] and cannot meet the demand of multi-rail power supply[5]. In this paper, a novel dual-output charge pump based on co-use technology is proposed. By adopting the capacitor sharing technique, it uses only four external capacitors and an array of switches to drive dual-output (step-up/down) and, thus, costs less than other schemes. Moreover, the use of multi-gain pairs including fraction gain satisfies the gain demands under different supply voltages and increases efficiency.

Although many modeling methods have been derived that include steady state analysis, the state-space averaging (SSA) method[10], and discrete time analysis[11], all of these were mainly applied to analyze the traditional switched power converter made of inductors. While analyzing an SC charge pump circuit, these methods are not explicit and accurate enough to describe the states of the circuit. In this paper, a new quantitative analytical method is developed for analy-

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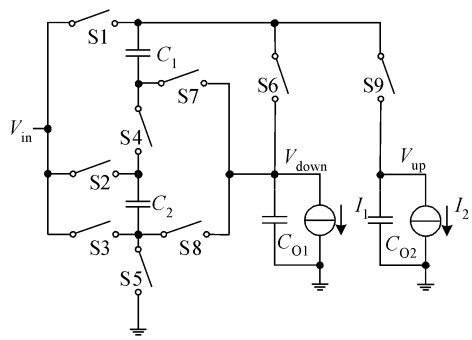

Fig. 1 Dual-output charge pump implementing 2/3-5/3 gain pair combination

zing the dual-output SC charge pump. By this method, a series of analytical equations were derived, which present the exact relationship among the input and output parameters and provides designers with an effective tool to find an optimum solution for a specific application.

2 Scheme of multi-gain pair's combination based on co-use technology

The simplest solution for a dual-output charge pump is the combination of two single-output charge pumps. It has a straightforward architecture and weak mutual interference. However, it needs two arrays of switched capacitors to realize the different gains, which demand more external capacitors and on-chip power switches and, thus, consume more chip area. Moreover, if regulated output voltages are demanded, two same regulated loops will be needed, which consequently increases the volume and cost. In this paper, based on co-use technology, a dual-output charge pump is proposed, which needs only one array of switched capacitors to realize the same multi-gain topology. It greatly decreases the number of on-chip switches and the external capacitors.

Figure 1 shows the diagram of the proposed dual-output charge pump with a 2/3-5/3 gain pair combination. Here a MOSFET switch array (S1～S9) is responsible for transforming the connections of the two fly capacitors (C_1 and C_2) that store and transfer electrical charge. C_{O1} and C_{O2} are the load capacitors, I_1 and I_2 are the load currents, V_{down} and V_{up} are the step-down and up output voltage, and 2/3 and 5/3 are the gains of the two output channels, respectively. The circuit is controlled by the three-phase non-overlap clock shown in Fig. 2. The switch sequence is listed in Table 1. A detailed description of the work states in different phases is shown in Fig. 3.

Phase 1: MOS switches S1, S2, S7, and S8 are turned on while the other switches are off. As shown in Fig. 3(a), paralleled fly capacitors C_1, C_2, and the load of the step-down path are in series. In this phase, C_1, C_2 are charged by source, and the step-down path is charged by the load current.

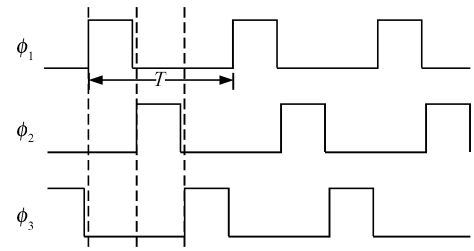

Fig. 2 Non-overlapping three-phase clock

Table 1 Switch sequence of the dual-output charge pump with 2/3-5/3 gain pair combination

	Phase 1	Phase 2	Phase 3
ON switches	1,2,7,8	3,4,9	4,5,6

Phase 2: Turn on S3, S4, and S9. As shown in Fig. 3(b), C_1, C_2, and V_{in} are in series to drive up the voltage. Part of the charges in C_1 and C_2 are transferred into the load of the step-up path and provide the output current.

Phase 3: Turn on S4, S5, and S6. As shown in Fig. 3(c), the series-connected C_1 and C_2 are in parallel with output capacitor C_{O1} to complete the periodic electricity balance and prepare for the next period.

In Phase 1 and Phase 3, the step-up path is not connected to the input source and the load current is supplied by C_{O2}. Similarly, in Phase 2, the load current

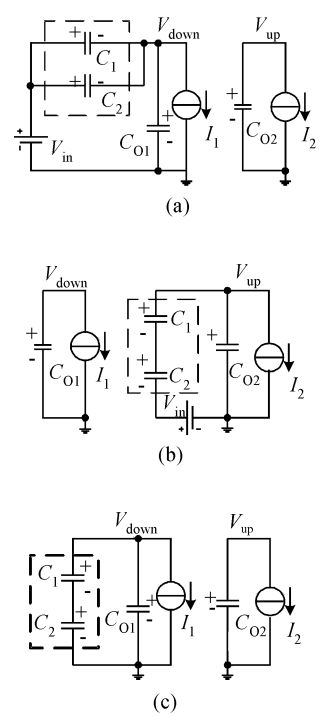

Fig. 3 Working diagram of dual-output charge pump with 2/3-5/3 gain pair combination (a) Phase 1; (b) Phase 2; (c) Phase 3

in the step-down path is provided by the charge in C_{O1}. In this circuitry, the two fly capacitors are shared by two output channels. The output capacitors C_{O1} and C_{O2} are also used to establish the charging path instead of an additional fly capacitor. Thus, the total number of external capacitors is reduced, which results in lower cost as well as a system volume smaller than other SC DC-DC converter topologies.

Over an operation period, the capacitors' voltages hardly change compared with their total electricity storage. Assuming the fly capacitor voltage is V_{C1} (equal to V_{C2} when the two fly capacitors are set symmetrical), and ignoring the on-resistance of the MOSFET switch and the DC fluctuations of capacitor voltage, a series of steady-state equations[12] will yield:

Phase 1:　$V_{in} - V_{C1} = V_{down}$　(1)

$V_{C1} = V_{C2}$　(2)

Phase 2:　$V_{in} + V_{C1} + V_{C2} = V_{up}$　(3)

Phase 3:　$V_{C1} + V_{C2} = V_{down}$　(4)

The solution is:

$$V_{down} = \frac{2}{3} V_{in} \tag{5}$$

$$V_{up} = \frac{5}{3} V_{in} \tag{6}$$

$$V_{C1} = V_{C2} = \frac{1}{3} V_{in} \tag{7}$$

From these results, the converter realizes simultaneous step up/down with gain pair of 2/3-5/3, as shown in Fig. 1. More detailed quantity analysis is given in section 3.

The power conversion efficiency of a switched capacitor DC-DC converter is approximately

$$\eta = \frac{V_{out}}{GV_{in}} \tag{8}$$

where G is the power conversion ratio, which is 2/3 for step-down and 5/3 for step-up in the proposed converter. It is necessary that GV_{in} should be larger than V_{out}, and the closer GV_{in} is to V_{out}, the higher the conversion efficiency is. By transforming the connection of the two fly capacitors C_1 and C_2, it is possible to get more combinations of different gain pairs, in order to provide more different power supply levels to meet the needs in the SOC applications. Based on the co-use technology proposed in this paper, the combinations of gain pairs can be fixed in a regulated power system with stable input voltage, which results in the reduction of the number of switches.

Extending the switch network shown in Fig. 1, more combinations of multi-gain pairs can be obtained to construct the dual-output charge pumps with programmable gains as shown in Fig. 4. Table 2 lists the possible dual-output charge pump topologies with 6 different combinations of multi-gain pairs produced by different switch sequences.

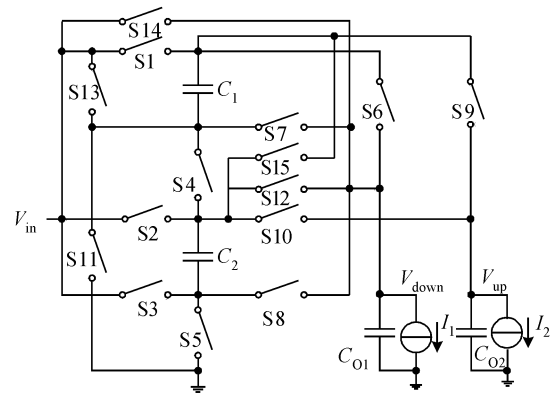

Fig. 4　Dual-output charge pump implementing multi-gain pairs combination

Table 2　Switch sequence of the dual-output charge pump implementing multi-gain pair's combination

Gain pairs	Phase 1(ON)	Phase 2(ON)	Phase 3(ON)
2/3,5/3	1,2,7,8	3,4,9	4,5,6
2/3,4/3	1,2,7,8	3,10	4,5,6
1/3,5/3	1,4,8	3,4,9	5,6,11,12
1/3,4/3	1,4,8	3,10	5,6,11,12
1/2,3/2	1,4,5,12	2,4,9	5,6,11,12
1,2	1,2,5,6,11	1,3,6,10,11	–
1,3	1,3,10,11,14	5,13,14,15	–
2,3	1,3,10,11	5,6,13,15	–

In order to provide a regulated output, a regulated loop could be added to the circuitry shown in Fig. 4. Figure 5 shows an example of a regulated output loop constituted by a dual-output charge pump with implementation of multi-gain pair's combination. By dynamically detecting the input voltage/current and the load current, the appropriate gain pair's combination will be chosen. This regulates the output according to the on-resistance of the switch. The structure in broken lines is the proposed design, the dual-output charge pump with multi-gain pair's combination.

3　Quantity analysis of dual-output charge pump

Steady state analysis, the state-space averaging

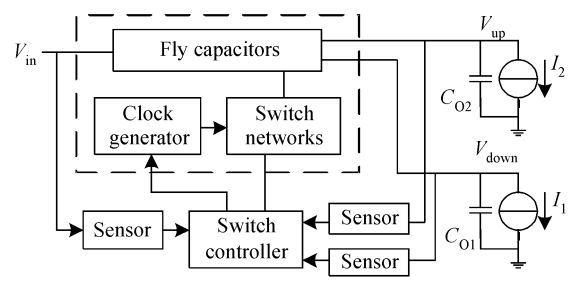

Fig. 5　Application to regulated loop of dual-output charge pump implementing multi-gain pair's combination

(SSA) method, and discrete-time analysis are all classical methods for analyzing the switching power supplies. These methods use a linear approximation of the voltage across the capacitor and the current passing through the inductor to simplify the calculation of switch power supply circuits. A modeling method of the charge pump using the linear approximation was given in Ref. [13]. But it seems unsuitable for the SC circuit without an inductor like that proposed since they show low precision in such cases. Therefore, a new method of analysis is proposed by an example of a dual-output charge pump with a 2/3-5/3 gain pair. The accuracy of the results derived by the two methods is compared.

3.1 Traditional linear model

Applying the method in Ref. [13], assuming the ripple of the output voltage is far less than the output voltage in a steady state, which is $\Delta V_O \ll V_O$, then the ripple can be ignored and the output voltage and the voltage across the switch capacitor can be considered as constant. Set the period time of each phase as T and the step-down/up voltage as V_1 and V_2 respectively, keep both load currents I_1 and I_2 constant, and assume the voltages across the two fly capacitors are both equal to V_C. In addition, set the charge/discharge current of fly capacitor C_1 (the same as C_2) as I_{1ch}, I_{2ch}, and I_{3ch} in Phase 1, Phase 2, and Phase 3, respectively, and the following equations can be derived according to the three phases:

$$V_{in} - I_{1ch}R_1 - V_C = V_1 \tag{9}$$

$$V_{in} + 2V_C - I_{2ch}R_2 = V_2 \tag{10}$$

$$2V_C - I_{3ch}R_3 = V_1 \tag{11}$$

where R_1, R_2, R_3 are the equivalent resistances of the charge/discharge path in Phase 1, Phase 2, and Phase 3, respectively.

In steady state, the rule of capacitor charge balance is applied: the net variation of the capacitor voltage over one period (equal to three switching periods in this topology) is zero. So:

$$\frac{I_{1ch}}{2}T = I_{2ch}T + I_{3ch}T \tag{12}$$

$$I_{2ch}T = I_1 \times 3T \tag{13}$$

$$I_{1ch}T + I_{3ch}T = I_2 \times 3T \tag{14}$$

From Eqs. (12) ~ (14), the equations are derived as:

$$I_{1ch} = 2I_1 + 2I_2 \tag{15}$$

$$I_{2ch} = 3I_2 \tag{16}$$

$$I_{3ch} = I_1 - 2I_2 \tag{17}$$

Substituting Eqs. (15) ~ (17) into Eqs. (9) ~ (11), results in:

$$V_1 = \frac{2}{3}V_{in} - \left(\frac{4}{3}R_1 + \frac{1}{3}R_3\right)I_1 - \left(\frac{4}{3}R_1 - \frac{2}{3}R_3\right)I_2 \tag{18}$$

$$V_2 = \frac{5}{3}V_{in} - \left(\frac{4}{3}R_1 - \frac{2}{3}R_3\right)I_1 - \left(\frac{4}{3}R_1 + \frac{4}{3}R_3 + 3R_2\right)I_2 \tag{19}$$

3.2 New analytical model

3.2.1 Analysis of conservation of charge in the steady state

Maintaining the same meaning of T, I_1, I_2, and I_{ich} ($i = 1,2,3$) as before, I_1 and I_2 are assumed constant. After the ith phase, the voltage variation across the switch capacitors C_k is marked as ΔV_{kj} ($k = 1,2$, $j = 1,2,3$) and the voltage variation of the load capacitor C_{Oj} is marked as ΔV_{Oji} ($j = 1,2$, $i = 1,2,3$), respectively. The changes of the capacitor voltages in different phases can be analyzed as follows.

In Phase 1, the capacitors C_1, C_2, and load capacitor C_{O1} are charged by the input voltage source with $0.5I_{1ch}$, $0.5I_{1ch}$, and $I_{1ch} - I_1$, respectively. The discharge current of C_{O2} is I_2. At the end of Phase 1, the voltage variations of the capacitors are:

$$\Delta V_{11} = \Delta V_{21} = \int_0^T 0.5I_{1ch}\mathrm{d}t \tag{20}$$

$$\Delta V_{O11} = \int_0^T (I_{1ch} - I_1)\mathrm{d}t \tag{21}$$

$$\Delta V_{O21} = -\int_0^T I_2\mathrm{d}t \tag{22}$$

Similarly, in Phase 2, they are:

$$\Delta V_{12} = \Delta V_{22} = -\int_0^T I_{2ch}\mathrm{d}t \tag{23}$$

$$\Delta V_{O12} = -\int_0^T I_1\mathrm{d}t \tag{24}$$

$$\Delta V_{O22} = \int_0^T (I_{2ch} - I_2)\mathrm{d}t \tag{25}$$

And, in Phase 3, they are:

$$\Delta V_{13} = \Delta V_{23} = -\int_0^T I_{3ch}\mathrm{d}t \tag{26}$$

$$\Delta V_{O13} = \int_0^T (I_{3ch} - I_1)\mathrm{d}t \tag{27}$$

$$\Delta V_{O23} = -\int_0^T I_2\mathrm{d}t \tag{28}$$

Using the law of conservation of capacitor charge in steady state, the solution is

$$\int_0^T I_{1ch}\mathrm{d}t = 2(I_1 + I_2)T \tag{29}$$

$$\int_0^T I_{2ch}\mathrm{d}t = 3I_2T \tag{30}$$

$$\int_0^T I_{3ch}\mathrm{d}t = (I_1 - 2I_2)T \tag{31}$$

3.2.2 Analytical equations of large-signal

Considering the ESR (equivalent series resistance) of the capacitor in the charge/discharge path in the actual circuit and the on-resistance of power switch, the charge and discharge currents approximately attenuated exponentially from the beginning

of each phase. In order to derive a more accurate model, the linear approximation is not adopted for the large-signal analysis of a charge pump.

In this analysis, assume that the fly capacitors C_1 and C_2 are the same as the capacitance of C, R_i (i = 1,2,3) is the equivalent resistance of the charge and discharge path in phase i (including the on-resistance of power switches and ESR of the capacitors), C_{iq} (i = 1,2,3) is the equivalent capacitance in phase i, V_{Ci} (i = 1,2) is the initial voltages of C_1 and C_2 at the beginning of phase i, and V_{ji} (j = 1,2; i = 1,2,3) is the initial voltages of load capacitors C_{Oj} at the beginning of phase i. I_1 and I_2 are still the load currents of the step-down/up channels, respectively. According to the circuit superposition theorem, the charge/discharge current is decided by both input voltage and the load current. So in Phase 1, the current is:

$$I_{1ch} = \frac{V_{in} - V_{c1} - V_{11}}{R_1} e^{\frac{-T}{R_1 C_{1q}}} + \frac{2C}{2C + C_{O1}} I_1 \tag{32}$$

where,

$$C_{1q} = \frac{1}{(1/2C + 1/C_{O1})} \tag{33}$$

And substituting Eq. (18) into Eq. (15), we obtain:

$$C_{1q}(V_{in} - V_{c1} - V_{11})(1 - e^{\frac{-T}{R_1 C_{1q}}}) + \frac{2C}{2C + C_O} I_1 T = 2(I_1 + I_2)T \tag{34}$$

Similarly, in Phase 2, we obtain:

$$I_{2ch} = \frac{V_{in} + 2V_{c2} - V_{22}}{R_2} e^{\frac{-T}{R_2 C_{2q}}} + \frac{0.5C}{0.5C + C_O} I_2 \tag{35}$$

$$C_{2q} = 1/(2/C + 1/C_O) \tag{36}$$

Substituting Eq. (21) into Eq. (16),

$$C_{2q}(V_{in} + 2V_{c2} - V_{22})(1 - e^{\frac{-T}{R_2 C_{2q}}}) + \frac{0.5C}{0.5C + C_O} I_2 T = 3I_2 T \tag{37}$$

In Phase 3, we obtain:

$$I_{3ch} = \frac{(2V_{c3} - V_{13})}{R_3} e^{\frac{-T}{R_3 C_{3q}}} + \frac{0.5C}{0.5C + C_O} I_1 \tag{38}$$

$$C_{3q} = 1/(2/C + 1/C_O) \tag{39}$$

And substituting Eq. (24) into Eq. (17):

$$C_{3q}(2V_{c3} - V_{13})(1 - e^{\frac{-T}{R_3 C_{3q}}}) + \frac{0.5C}{0.5C + C_O} I_1 T = (I_1 - 2I_2)T \tag{40}$$

In a steady state, the initial voltage of each capacitor is in a phase equal to the final voltage of the last phase. In this design, assuming $C_{O1} = C_{O2} = 10C$, then the initial voltage of Phase 2 is derived:

$$V_{C2} = V_{C1} + \frac{\int_0^T \frac{I_{1ch}}{2} dt}{C} = V_{C1} + \frac{(I_1 + I_2)T}{C} \tag{41}$$

Similarly:

$$V_{12} = V_{11} + \frac{(I_1 + 2I_2)T}{10C} \tag{42}$$

$$V_{22} = V_{21} - \frac{I_2 T}{10C} \tag{43}$$

$$V_{C3} = V_{C2} - \frac{3I_2 T}{C} \tag{44}$$

$$V_{13} = V_{12} - \frac{I_1 T}{10C} \tag{45}$$

$$V_{23} = V_{22} + \frac{2I_2 T}{10C} \tag{46}$$

By substituting Eqs. (28) ~ (33) into Eqs. (21), (24), and (27), the relationships among each parameter are acquired, where the initial voltages of fly capacitors and the output capacitors in each phase are:

$$V_{C1} = \frac{1}{3}V_{in} + \frac{T}{600C}\left[\left(\frac{401}{\gamma} - 400 - \frac{221}{\alpha}\right)I_1 + \left(840 - \frac{840}{\gamma} - \frac{240}{\alpha}\right)I_2\right] \tag{47}$$

$$V_{11} = \frac{2}{3}V_{in} + \frac{T}{600C}\left[\left(400 - \frac{401}{\gamma} - \frac{442}{\alpha}\right)I_1 + \left(\frac{840}{\gamma} - 840 - \frac{480}{\alpha}\right)I_2\right] \tag{48}$$

$$V_{21} = \frac{5}{3}V_{in} + \frac{T}{600C}\left[\left(400 - \frac{442}{\alpha} + \frac{802}{\gamma}\right)I_1 + \left(2940 - \frac{480}{\alpha} - \frac{1680}{\gamma} - \frac{3723}{\beta}\right)I_2\right] \tag{49}$$

where $\alpha = 1 - e^{\frac{-T}{R_1 C_{1q}}}$, $\beta = 1 - e^{\frac{-T}{R_2 C_{2q}}}$, $\gamma = 1 - e^{\frac{-T}{R_3 C_{3q}}}$.

In most applications, the on-resistance of MOS switches and capacitors could be considered constant, resulting in constant coefficients α, β, γ, which consequently leads to a linear relationship among output voltages, input voltage, and load current. Based on the linear relationship, designers can optimize the charge pump according to input voltages and load current requirement.

3.2.3 Small-signal model

In order to apply the proposed dual-output charge pump, the small-signal model is required to further derive the transfer function of the regulated loop.

To use state-space averaging, it needs to have an input vector $\boldsymbol{u} = [v_{in}, v_{G1}, v_{G2}, i_1, i_2]^T$, a state vector $\boldsymbol{x} = [v_C, v_1, v_2]^T$, and an output vector $\boldsymbol{y} = [v_1, v_2]^T$, where v_{in} is the input voltage, v_{G1} is the gate voltage of S1 and S2, v_{G2} is the gate voltage of S9, i_1 and i_2 are load current; v_C, v_1, v_2 are the small signal voltage of the capacitors C_1, C_{O1}, C_{O2}, respectively; and v_1, v_2 are the output voltage of the step-down/up path. The assumption of $C_o = 10C$ is still adopted. Finally, the state equations are expressed as:

$$\dot{x} = Ax + Bu, y = Cx + Du \tag{50}$$

where the coefficients are:

$$A = \begin{bmatrix} -\frac{1}{3C}\left(\frac{1}{2}g_2 + 2g_3 + 2g_4 + 2g_5\right) & -\frac{g_2}{6C} + \frac{g_5}{3C} & \frac{g_4}{3C} \\ -\frac{g_2}{30C} + \frac{2g_5}{30C} & -\frac{(g_2 + g_5)}{30C} & 0 \\ \frac{2g_3}{30C} + \frac{2g_4}{30C} & 0 & -\frac{g_4}{30C} \end{bmatrix}$$

$$B=\begin{bmatrix} \frac{g_1}{3C}+\frac{1}{2}\times\frac{g_2}{3C}-\frac{g_3}{3C}-\frac{g_4}{3C} & -\frac{g_1}{3C} & \frac{g_3}{3C} & 0 & 0 \\ \frac{2g_1}{30C}+\frac{g_2}{30C} & -\frac{2g_1}{30C} & 0 & -\frac{1}{10C} & 0 \\ \frac{g_3}{30C}+\frac{g_4}{30C} & 0 & -\frac{g_3}{30C} & 0 & -\frac{1}{10C} \end{bmatrix}$$

$$C=\begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

$$D=0$$

The solution of the matrix equation is:

$$y=[C(sI-A)^{-1}B+D]u \tag{51}$$

This is the small-signal model. Based on this, the transfer functions between output voltage and controlled gate voltage are derived as:

$$\frac{v_2}{v_{G2}}=\frac{-4g_1}{P(s)}[30C^2s^2+C(30g_5+21g_4+20g_3)s+g_4g_5] \tag{52}$$

$$\frac{v_2}{v_{G2}}=\frac{-3g_3}{P(s)}[20C^2s^2+C(4g_2+14g_5)s+g_2g_5] \tag{53}$$

where

$$P(s)=1800C^3s^3+60C^2(21g_2+20g_3+6g_4+21g_5)s^2+2C(20g_3g_5+26g_2g_4+41g_4g_5+45g_2g_5+20g_2g_3)s+3g_2g_4g_5$$

and g_1, g_3 are the transconductance of the switch S1 and S9, and g_2, g_4, and g_5 are the reciprocal of the equivalent resistance in charge/discharge path in phases 1, 2, 3, respectively.

4 Simulation and test results

The proposed dual-output multi-gain charge pump was designed and fabricated in a TSMC 0.35μm 5V mixed-signal CMOS process. It was simulated by Cadence Spetre simulator. The topology of the charge pump with a 2/3-5/3 gain pair is shown in Fig. 1. The schematic is shown in Fig. 6 in detail, in which C_3 is a small on-chip capacitor to provide a body-bias voltage V' for all the pMOS switch transistors and the non-overlapping three-phase clock shown in Fig. 2 is adopted as the controlled clock sequence.

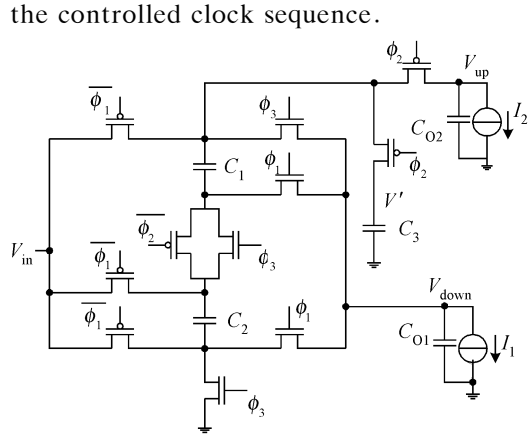

Fig. 6 Schematic of the dual-output charge pump with 2/3-5/3 gain pair combination

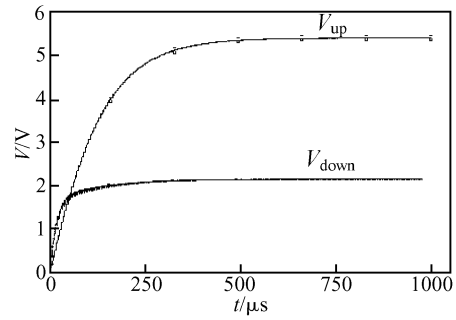

Fig. 7 Transient output waves of 2/3-5/3 gain pair combination

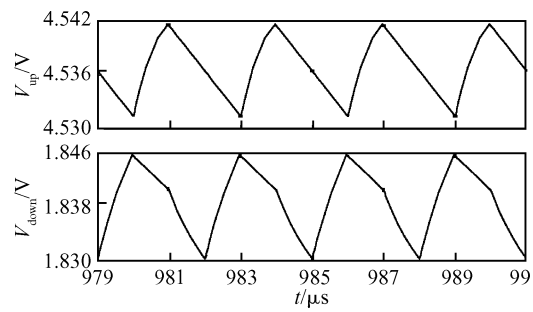

Fig. 8 Simulation results of dual output charge pump under condition 4

The simulation results prove that the proposed charge pump realizes the step-up and down dual-output, as shown in Fig. 7. Figure 8 shows the ripples of the output voltage. In the 2/3-5/3 gain-pair combination, the ripples are less than 11 and 16mV, respectively, in the step-up/down output, which are within the acceptable range.

Figure 9 shows the simulation results of the output response when the load steps, in which I_1 is the load current of the step-down channel and V_{up} is the output voltage of the step-up channel. The results show that while the load steps, the fluctuation of the output voltages in both channels is limited within the magnitude of tens of multi-volts. Therefore, both channels of the proposed charge pump can output stable voltages independently to load fluctuation of either its channels.

To further verify the proposed analytical method, simulations were also carried out under several typical conditions, which are listed in Table 3. The

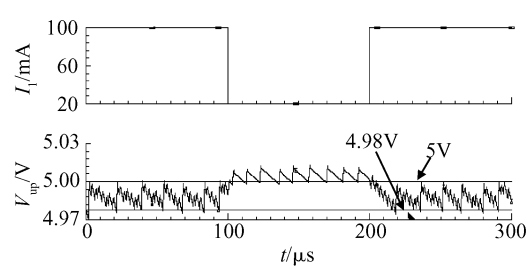

Fig. 9 Simulation results of transient response under load step

Table 3　Simulation conditions of dual output charge pump

I_{load}	Condition 1	Condition 2	Condition 3	Condition 4
I_1/mA	10	10	50	50
I_2/mA	10	50	10	50
V_{in} = 3.0V, $C_1 = C_2 = 1\mu$F, $C_{O1} = C_{O2} = 10\mu$F				

simulation results are compared with the calculated results using the proposed model (model 2) and the traditional model (model 1). The results listed in table 4 show that the proposed analytical model is more precise than the traditional one by almost one magnitude, and that the simulation results are consistent with predictions of the new model.

Figure 10 shows the die micrograph of the proposed dual-output charge pump.

The test results are shown in Fig. 11.

The test conditions are: the power supply voltage $V_{in} = 3.25$V, the load current of channel 2 $I_2 = 0$mA, and the load current of channel 1 I_1 is shifted between 1 and 100mA at the rise/fall speed of 80mA/μs and shift frequency of 1000Hz.

In Fig. 11, V_{up} is the output of channel 2, which is an altered waveform after a 5V DC offset, V_{down} is the output waveform of channel 1 with a DC offset of 1.8V, and I_1 is the load current of channel 1. The top curve is the digital signal that controls the gain shift. Compared with Fig. 9, the test results are very close to the simulation results. Thus, the proposed circuit succeeded in simultaneously providing two regulated output voltages for step-up and step-down, and that under large load steps both channels keep output voltages steady.

Table 4　Simulation results versus model calculation predictions

	Condition	Simulation /V	Model 1 /V	Model 2 /V	Error of Model 1	Error of Model 2
V_{down}	1	1.96622	1.97687	1.96622	0.54%	0.05%
	2	1.91024	1.96114	1.91061	2.66%	0.02%
	3	1.88751	1.90010	1.89242	0.67%	0.26%
	4	1.83026	1.88437	1.83586	2.95%	0.31%
V_{up}	1	4.90879	4.90194	4.90700	0.14%	0.04%
	2	4.50708	4.52545	4.50644	0.41%	0.01%
	3	4.93483	4.88621	4.93056	0.99%	0.02%
	4	4.53656	4.50972	4.53504	0.59%	0.03%

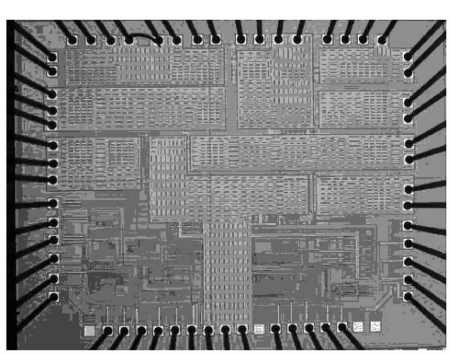

Fig. 10　Microphotograph of die

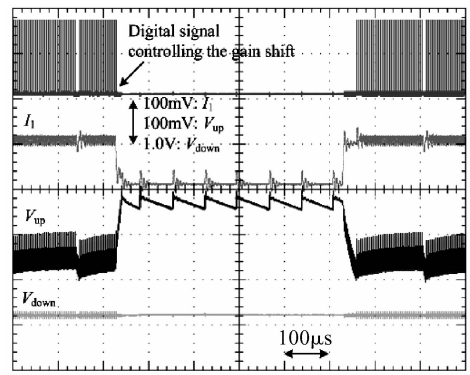

Fig. 11　Tested results of transient response under load step

5　Conclusion

In this paper, a novel architecture for a dual-output charge pump based on co-use technology was proposed. It simultaneously provides step-up and a step-down output voltages with driving capability. A multi-gain pair is implemented to meet the gain demand of different input voltages and improve its efficiency. The co-use technology of switch array and external capacitors reduce the cost of the chip and the application circuitry. Meanwhile, a modeling method was proposed for analyzing the dual-output charge pump. Both large-signal and small-signal models were derived to describe explicitly the performances of the charge pump. The simulation results showed that the performances of proposed circuit were consistent with expectations. They also demonstrated that the derived equations can give accurate predictions for outputs of the charge pump and that the proposed analytical model is valid. The proposed circuit was designed and fabricated in a TSMC 0.35μm mixed-signal CMOS process and all design hypotheses were verified by the tested results.

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高效率双通路片上电荷泵的研究与设计*

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摘要：针对现代系统芯片中处理器核等数字模块和模拟模块对于不同电平电源供电的需要，提出一种基于复用技术的新型双通路电荷泵实现方案.该电荷泵能同时提供具有驱动能力的升压和降压模式电压输出，且可实现可变增益组合，以便根据检测到的输入电压自动调整增益组合以提高工作效率.开关阵列和电容的复用降低了芯片和应用电路的成本.文章给出了电荷泵的拓扑结构和用于量化分析的大信号解析公式和小信号模型.电路在 TSMC 的 0.35μm 混合信号 CMOS 工艺下设计完成.仿真验证和流片测试的结果表明所提出的设计目标均已实现，所获结果与解析公式的计算高度一致，证明了模型以及分析方法的正确性.

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