A Frequency-Independent Equivalent Circuit for High-k Stacked Monolithic Transformers

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Abstract: A new 2-Π lumped element equivalent circuit model for high-k stacked on-chip transformers is proposed. The model parameters are extracted with high precision, mainly based on analytical methods. The developed model enables fast and accurate time domain transient analysis and noise analysis in RFIC simulation since all elements in the model are frequency independent. The validity of the proposed model has been demonstrated by a fabricated monolithic stacked transformer in TSMC's 0.13μm mixed-signal (MS)/RF CMOS process.

Key words: high-k; stacked on-chip transformer; frequency-independent; equivalent circuit
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1 Introduction

Recently, monolithic transformers have been widely employed as important elements to enhance the performance of many kinds of RF blocks, including low noise amplifiers (LNA), voltage-controlled oscillators (VCO), and power amplifiers (PA)[1~3]. There are three different on-chip transformer realizations, namely, the tapped, the interleaved, and the stacked[4]. The stacked can provide the highest coupling factor (k) and the best area efficiency, but has a lower self-resonance frequency (SRF). As an essential tool for circuit design, accurate equivalent circuit models of transformers, using lumped RLC elements, efficiently characterize their electrical performances for circuit simulation. Several models of stacked transformer have been presented in the past decade[4,5]. However, current models are frequency-dependent because some elements in the models depend on frequency. It is difficult to incorporate frequency-dependent elements in SPICE-type simulators[6]. In addition, frequency-dependent models are not compatible with time domain transient analysis. Thus, it is important to investigate a frequency-independent model for stacked transformers. In this paper, the on-chip high-k stacked transformer is introduced. Then, a lumped element frequency-independent model with high accuracy is presented. A stacked transformer is realized in TSMC's 0.13μm RF/MS CMOS process. The S-parameter of the realized transformer is measured with an Agilent E8363B VNA. The measured results agree well with the modeling parameters.

2 High-k stacked monolithic transformer

Figure 1 shows a stacked structure monolithic transformer. It uses multiple metal layers and exploits both vertical and lateral magnetic coupling to provide the highest coupling factor (k) and the best area efficiency. The k factor can reach 0.9 or more, and the occupied chip area can be reduced significantly. The main drawback of this structure is the high port-to-port capacitance, and consequently a lower SRF. But, the low SRF can be improved by increasing the oxide thickness between spirals in modern silicon-based multi-metal-level processes. In practice, this can be implemented by selecting proper metal levels. The k factor must be decreased when the oxide thickness is increased. However, the change of port parasitic capacitance is much more sensitive than the k factor[4]. Therefore, decreasing the k factor is usually acceptable when the oxide thickness is increased to improve the SRF.

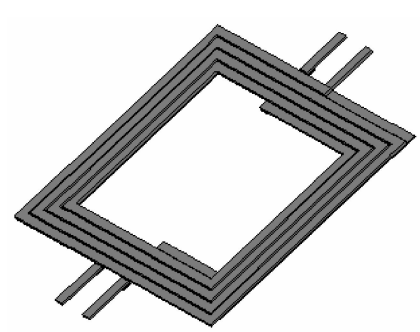

Fig. 1 Stacked structure monolithic transformer

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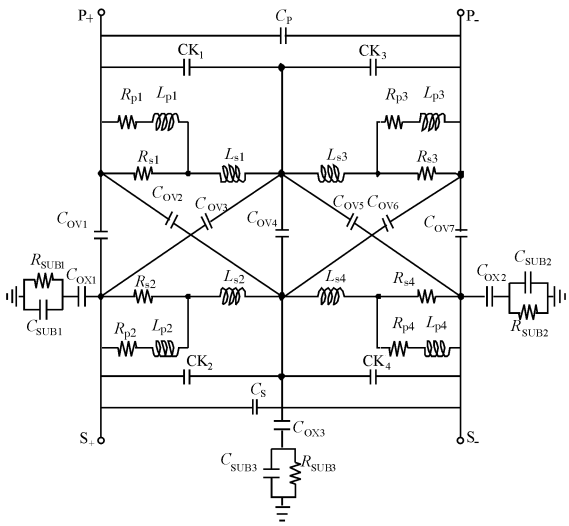

Fig. 2 Frequency-independent equivalent circuit for a stacked on-chip transformer in which all mutual inductances are not shown

3 Frequency independent equivalent circuit

The electrical performance of a transformer can be characterized by frequency domain network parameters, such as the *S*-, *Y*-, or *Z*-parameters. Yet an equivalent circuit is indispensable for circuit design due to the fact that the frequency domain network parameters cannot be employed in the time domain simulation or noise analysis. Moreover, as mentioned above, the equivalent circuit should be frequency-independent. The proposed equivalent circuit for a stacked on-chip transformer is sketched in Fig. 2. There are a number of elements in the circuit model, and their physical meanings and how to extract their values according to the device's geometric dimensions will be presented in detail.

As shown in Fig. 2, based on the ladder circuit representation, a 2-Π equivalent circuit model is built to capture the distributed characteristics of the monolithic transformer. First, the DC current is uniformly distributed inside the primary and secondary conductors, and can be characterized by R_{si} and L_{si} ($i=1,2,3,4$) in series with mutual inductances denoted by M_{ij} (not shown in Fig. 2) between each two self inductances (L_{si}, L_{sj}, $i,j=1,2,3,4,i<j$). As the frequency increases, the skin and proximity effect[7] will push the AC current to the metal surface, which results in a frequency dependent loss and inductance in the metal conductor. Unless frequency dependent components are employed, a simple RL series (R_{si} and L_{si}) branch can not model this effect. Therefore, an additional RL ladder (R_{pi} and L_{pi}) in parallel to the R_{si} ($i=1,2,3,4$) and twelve mutual inductances M_{pij} (not shown in Fig. 2 either) between L_{si} and L_{pj} ($i,j=1,2,3,4,i\neq j$) are introduced to model the frequency dependent loss and inductance. There are two kinds of parasitic capacitances that lead to the stacked on-chip transformer's lower SRF. One comes from horizontal electric field and the other is due to the vertical electric field. The capacitance CK_i ($i=1,2,3,4$) represents the coupling between the adjacent metal tracks of the primary or secondary coils of the transformer, respectively. The horizontal electric field coupling contributes to those capacitances. The overlap capacitance due to vertical electric field coupling between primary and secondary coils can be represented by C_{OVi} ($i=1\cdots7$). The other part of vertical capacitances is C_p and C_s, which represent the overlap capacitance between the spiral and underpass metal lines. The lossy capacitive coupling between the secondary of the stacked transformer and conductive substrate can be modeled by three RC subcircuits $\{C_{oxi}, R_{SUBi}, C_{SUBi}, i=1,2,3\}$.

In the proposed model, the most important aspect is the extraction of model parameters. The parameters extraction steps in this paper are mainly based on analytic methods. The components of the ladder subcircuits, L_{si}, R_{si}, L_{pi}, R_{pi} ($i=1,2,3,4$) can be calculated by[8]:

$$R_{pi} = K_R R_{si},\ L_{pi} = K_L L_{si} \tag{1}$$

$$R_{si} = (1 + 1/K_R)\ R_i^{dc} \tag{2}$$

$$L_{si} = L_i^{dc}/[1 + K_L(1 + K_R)^{-2}] \tag{3}$$

where K_L and K_R are two introduced coefficients acquired by fitting optimization. R_i^{dc} and L_i^{dc} are the DC resistance and inductance of the ith spiral, respectively. R_i^{dc} is equal to the product of the metal sheet resistance and the aspect of the metal line (total metal length/metal width). L_i^{dc} can be calculated by an analytical equation[5]. The transformer mutual inductances M_{ij} ($i,j=1,2,3,4,i<j$) can be estimated using the expressions $M_{ij}\approx \mathrm{Imag}(Z_{ij})/\omega$, where Z_{ij} are the elements of the *Z*-parameter matrix, which is converted from the measured *S*-parameter matrix, while ω should be low (in this paper, $\omega=2\pi\times100\mathrm{MHz}$). Calculating the proximity effect mutual inductances M_{pij} ($i,j=1,2,3,4,i\neq j$) by an analytical formula is difficult. M_{pij} is obtained also by fitting iteration. However, the variables to be fitted can be reduced to four using a symmetric layout. The lateral coupling capacitance CK_i ($i=1,2,3,4$) can be obtained by Gupta's fringing capacitance curves for coplanar rectangular coupled bars[9]. The total overlap capacitance between primary and secondary coils, C_{OV}, can be estimated by $A\,\varepsilon / t_{OX} + P\,C_{PS}$, where ε and t_{OX} are the oxide dielectric constant and thickness between primary and secondary, respectively. A is the area of the spirals,

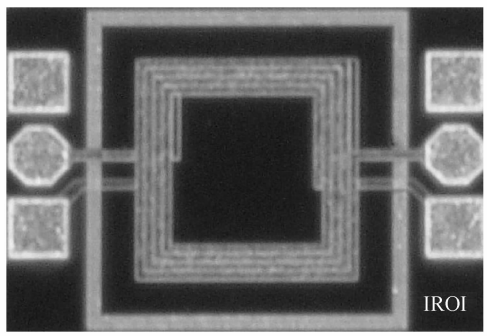

Fig. 3　Micrograph of the implemented transformer

and P is the length of the shorter of the primary or secondary. C_{PS} is the per-unit-length specific capacitance whose value is obtained also by Gupta's fringing capacitance curves. The C_{OVi} ($i = 1 \cdots 7$) is equal to 1/8 C_{OV} for $i \neq 4$ and 1/4 C_{OV} for $i = 4$. C_P and C_S can be evaluated approximately by the commonly used parallel plate capacitor formula. The components related to the capacitive coupling between substrate and the secondary, $\{C_{oxi}, R_{SUBi}, C_{SUBi}, i = 1, 2, 3\}$ can be determined by a series of analytical formulas derived by Huo *et al*.[10] with the knowledge of transformer layout and process technology.

4　Experimental verification

For demonstration, a stacked monolithic transformer has been fabricated in TSMC's 0.13μm RF/MS CMOS process. Figure 3 shows the micrograph of the implemented transformer. The outer diameters of both the primary and secondary are 300μm and the width of metal line is 10μm. The spacing of adjacent metal lines is 2μm and the turns of the primary and secondary are four. The S-parameters of the implemented transformer have been measured up to 5GHz by an Agilent E8363B VNA. The extracted equivalent circuit parameters of the transformer are as follows: $L_{si} = 3.4$nH, $L_{pi} = 1.3$nH, $M_{ij} = 3.1$nH (where subscript $i, j = 1, 2, 3, 4, i < j$). $R_{s1} = R_{s3} = 3.3\Omega$, $R_{s2} = R_{s4} = 12.5\Omega$, $R_{p1} = R_{p3} = 1.6\Omega$, $R_{p2} = R_{p4} = 6.0\Omega$. $M_{p12} = M_{p14} = M_{p32} = M_{p34} = -1.61$nH, $M_{p21} = M_{p41} = M_{p23} = M_{p43} = -0.67$nH, $M_{p13} = M_{p31} = 1.90$nH, $M_{p24} = M_{p42} = -1.85$nH. $CK_1 = CK_3 = 317$fF, $CK_2 = CK_4 = 109$fF. The total overlap coupling capacitance C_{OV} is 6.1pF. C_P and C_S are 36.8fF and 34.4fF, respectively. The values of the substrate components are: $C_{OX1} = 91.5$fF, $C_{OX2} = 109.4$fF, $C_{OX3} = 200.9$fF; $C_{SUB1} = 13.7$fF, $C_{SUB2} = 15.9$fF, $C_{SUB3} = 29.5$fF; $R_{SUB1} = 771.0\Omega$, $R_{SUB2} = 663.4\Omega$, $R_{SUB3} = 340.8\Omega$. Figures 4 and 5 show comparisons between the modeled and measured S-parameters. The S_{11} and S_{22} of both are shown in Fig. 4. Figure 5 shows the modeled and measured

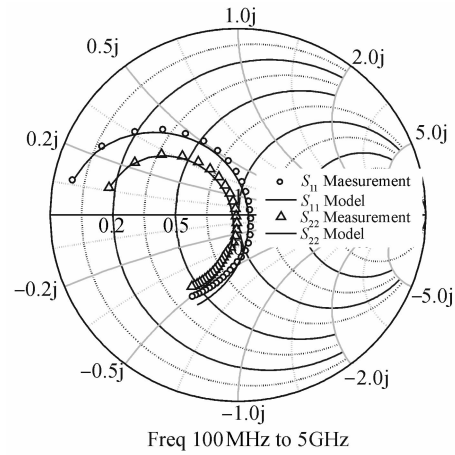

Fig. 4　S_{11} and S_{22} of the fabricated stacked transformer

S_{21}. The modeled results show a high agreement with the measured up to 5GHz. As a matter of fact, the SRF of the fabricated transformer is lower than 2GHz and the operating frequency is about 1GHz. Thus, the proposed equivalent circuit has better accuracy in RFIC simulation.

5　Conclusion

In this paper, a new 2-Π frequency-independent equivalent circuit model for high-k stacked on-chip transformers has been developed. The model parameters are extracted mainly based on analytical methods. Since all components are frequency independent, it is fully compatible with time domain transient analysis. An on-chip stacked transformer has been fabricated in TSMC's 0.13μm RF/MS CMOS process to demonstrate the validity of the proposed model. Agreement was achieved between the measured and modeled S-parameters up to 5GHz, which is much higher than SRF.

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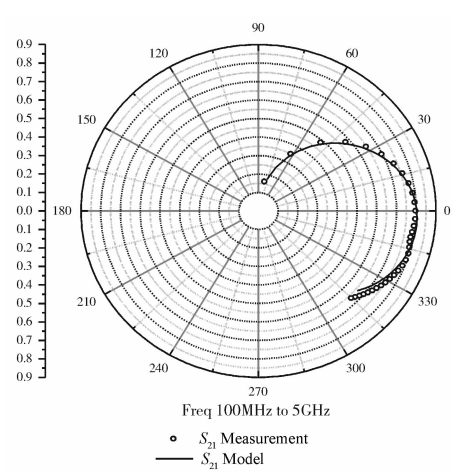

Fig. 5　S_{21} of the fabricated stacked transformer

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高耦合系数层叠结构片上变压器的频率无关等效电路

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摘要：针对高耦合系数层叠结构的片上变压器提出了一个新型 2-Π 集总元件等效电路模型. 主要基于解析公式提取了该模型的元件参数. 由于该模型中全部元件取值均与工作频率无关，因此该模型完全可以用于射频集成电路设计中的时域瞬态仿真及噪声分析. 为了验证该模型的精度，采用台湾半导体制造有限公司(TSMC)提供的 0.13μm 混合信号/射频 CMOS 工艺实际制作了一个高耦合系数层叠结构片上变压器，并使用 Agilent E8363B 矢量网络分析仪测量了其 S 参数. 测量结果表明该模型在高于两倍自谐振频率范围内均能够与测试结果很好地符合.

关键词：层叠结构；片上变压器；频率无关；等效电路

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