A 1.8V CMOS Direct Conversion Receiver for a 900MHz RFID Reader Chip*

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Abstract: A direct conversion receiver with optimized tolerance to local carrier interference is designed and implemented in a 0.18μm 1P6M mixed-signal CMOS process for a 900MHz RFID reader transceiver. A baseband amplifier with series feedback topology is proposed to achieve passive mixer buffering, baseband DC cancellation, and signal amplification simultaneously. The receiver has a measured input 1dB compression point of −4dBm and a sensitivity of −70dBm when 10dB SNR for digital demodulation is required. The receiver is integrated in a reader transceiver chip and consumes 90mA from a 1.8V supply.

Key words: direct conversion receiver; DC cancellation; reader; RFID
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1 Introduction

Due to the moderate reading distance and communication speed, 900MHz ultra-high-frequency (UHF) band radio frequency identification (RFID) applications are now growing rapidly in daily life, e.g., supply chains, storage management, tracing/tracking, and anti-counterfeiting[1]. The mainstream RFID air interface standards adopted by industry are EPC-global Class 1 Generation 2 UHF RFID specification[2] and ISO 18000-6C[3]. Local radio regulations allocate and restrict the usage of radio spectrum, for instance, ETSI 302 208 in Europe[4], FCC part 15 in the United States[5], and 800/900MHz RFID application regulation in China[6].

A passive tag UHF RFID system works similar to a radar system: an electromagnetic wave is emitted from the reader and then scattered back together with the tag's information. The communication procedure is composed of a down-link phase and an up-link phase in time division duplex mode. But the difference for normal half-duplex systems is that the reader needs to continue transmitting an unmodulated carrier to energize tags in the up-link phase. Furthermore, in a single antenna reader, which is preferred in most cases due to size and cost considerations, the power amplifier and the receiver are connected to the same antenna. Normally, a directional component like a circulator or directional coupler is used to separate the transmitted and received signal, with isolation below 30dB. That brings 0dBm carrier leakage from transmitter (TX) to receiver (RX), when power amplifier is transmitting 30dBm power to antenna. This high power leakage increases the receiver noise floor (mainly composed of phase noise, thermal noise and flick noise in CMOS circuit) and compresses the signal gain, therefore, finally reducing the receiver's sensitivity.

In this paper, we present an input compression point optimized direct conversion receiver that is based on a passive mixer. We discuss the system specifications and architecture and describe the circuit implementation.

2 System architecture

When only the free space path loss is taken into account, the received power at the tag and reader antenna can be expressed as

$$P_{\mathrm{r,tag}} = P_{\mathrm{PA}} G_{\mathrm{TX}} G_{\mathrm{tag}} \left(\frac{\lambda}{4\pi d}\right)^2$$
$$P_{\mathrm{r,reader}} = P_{\mathrm{PA}} G_{\mathrm{TX}} \eta \left(\frac{\lambda}{4\pi d}\right)^4 G_{\mathrm{RX}} \quad (1)$$

where $P_{\mathrm{r,tag}}$ and $P_{\mathrm{r,reader}}$ is the power received by the tag and reader, respectively, $P_{\mathrm{r,PA}}$ is the output power of the reader's power amplifier, G_{TX}, G_{RX}, and G_{tag} are the gains of the TX antenna, RX antenna, and tag antenna, respectively, η is the ratio of backscattered power to incidence power at the tag, and $(\lambda/4\pi d)^2$ is

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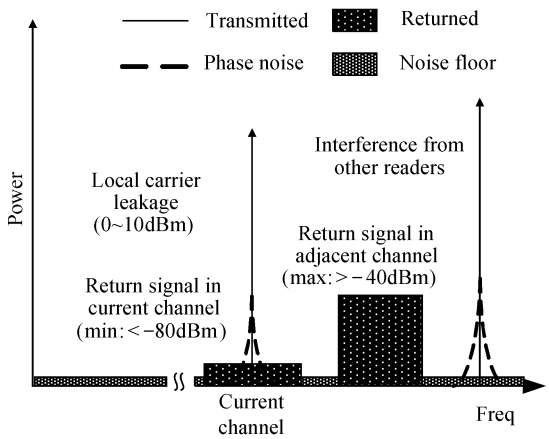

Fig. 1　Reader received signal spectrum

the free space path loss where λ is the wave length and d is the distance. This induces an instructive conclusion that the tag received power fades with distance in 6dB/Oct while the reader received power fades in 12dB/Oct.

In a normal multi-reader environment, the reader receiver encounters signal, noise, and interference (as shown in Fig. 1). The interferences, including local carrier leakage, adjacent reader transmitted signal, and tag backscattered signal responding to other readers, is the most serious source of degrading reader performance.

In a real application scenario, considering the environment reflection and antenna's voltage standing wave ratio (VSWR), 20dB TX-RX isolation is reasonable (actually, in the worst case, 15dB can be observed in measurement). For a single antenna reader, the carrier leakage at receiver input can be 10dBm (0.7V RMS, or 1V amplitude on 50Ω load) when transmitting 30dBm power.

The adjacent reader transmitted power can not be isolated by the circulator and will feed directly into the receiver. Fortunately, Equation (1) shows the power loss is relatively large in the region near the antenna, e.g., 25dB at 0.5m and 31dB at 1m. So we make the assumption that the maximum interference from a nearby reader is comparable to the local carrier leakage in common cases.

To reject the local carrier interference, one simple solution is first to down convert the carrier to the baseband and then remove it at a low frequency, rather than at radio frequency. The direct conversion receiver (DCR) is preferred because to cancel a large interference at DC is easier than to cancel one at a non-zero intermediate frequency. The direct conversion structure also makes the system with same TX and RX frequency concise. The similarity of transmitting waveform and the local oscillation for down conversion provided by DCR helps to correlate phase noise cancellation at down-conversion. The transceiver architecture is shown in Fig. 2.

After the influence of carrier leakage is removed at the baseband, a low pass filter (LPF) with 3dB bandwidth at 3MHz is used to reject adjacent channel interference and out-band noise. This filtering is necessary before the signal is further amplified, especially in a multi-reader environment. A 60B dynamic range automatic gain control (AGC) with internal DC offset cancellation adjusts the signal strength for the signal digitization in a 2nd order, 32 over-sampling ratio (OSR) sigma-delta ADC. To the advantage of the over-sampling ADC, the LPF before AGC can accomplish anti-aliasing easily. The channel selection is done in the digital domain.

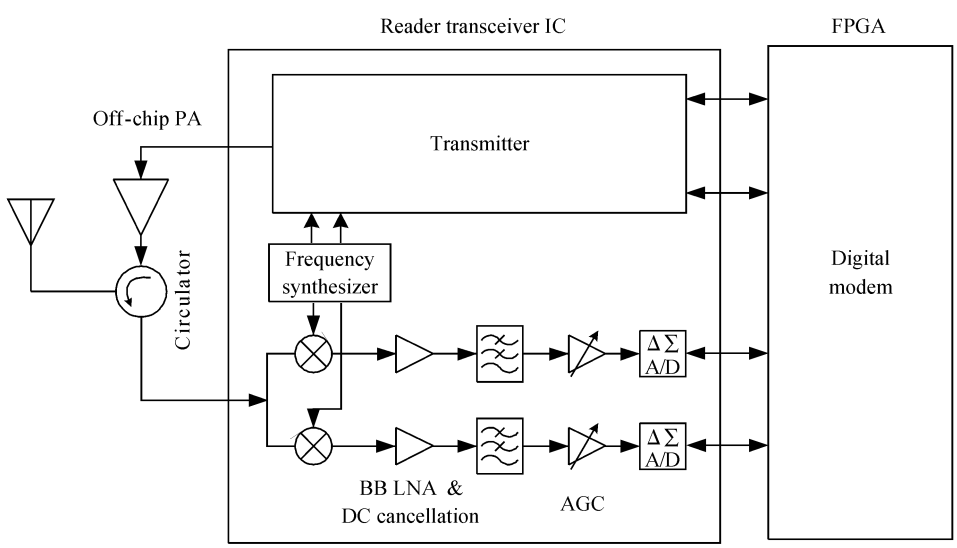

Fig. 2　Direct conversion architecture of RFID reader transceiver chip

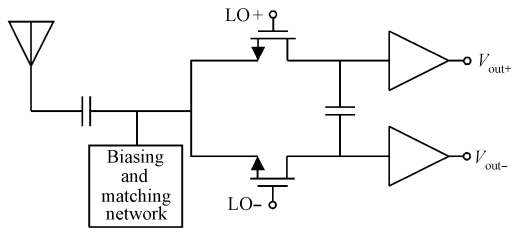

Fig. 3 Single balanced passive mixer

3 Circuit implementation

To tolerant high power carrier leakage, the receiver should have a high input compression point and a limited front-end gain. A passive mixer is used as the first stage for its high linearity, low flicker noise, and low power consumption. A single balanced structure is adopted to eliminate single ended to differential conversion balun and produces 6dB more gain than the double balanced structure[7]. The LO feed through problem in the single balanced mixer is not critical in the presence of large carrier leakage, which has the same frequency and is much larger. In absence of LNA driving and for low noise consideration, the passive mixer works in voltage switching mode[8], which requires the following stage has a high input impedance, as shown in Fig. 3.

The mixer output buffer can be merged to baseband amplifiers, when series feedback structure with high input impedance is used for DC cancellation instead of the commonly used parallel feedback current steering scheme. The structure of the baseband amplifier is shown in Fig. 4, where G_1, G_2 is the gain of the first and second stage, and A_1, A_2, A_3 is the open loop gain of the three OPAMPs, respectively. In the first stage, R_1 and C_1 provide the DC path to store the DC value while the signal is amplified. To avoid influencing the signal amplification, R_1 and C_1 should be large enough to set the high pass pole low. In this design, $R_1 = 100\text{k}\Omega$ and $C_1 = 10\text{nF}$. A small resistor R_4 is used in parallel with R_1 to set the signal gain, together with R_3. When $R_4 \ll R_1$, $R_3 \gg Z(C_1)$, where $Z(C_1)$ is the impedance of C_1, the pass-band gain of the first stage can be estimated as: $G_1 \approx 1 + R_4/R_3$. C_3 is added to flatten the frequency response in the pass-band. For instance, the first stage signal gain is approximately 12dB when $R_3 = 100\Omega$, $R_4 = 300\Omega$.

In the second stage, a Miller capacitor is used in the feedback path to extract the DC portion. Similar to the first stage, C_2 and R_2 set the position of the high pass pole, which should be consistent with the first stage. In this case $R_2 = 100\text{k}\Omega$, $C_2 = 10\text{nF}$. The small signal transfer function of the low pass filtering in the feed back loop is:

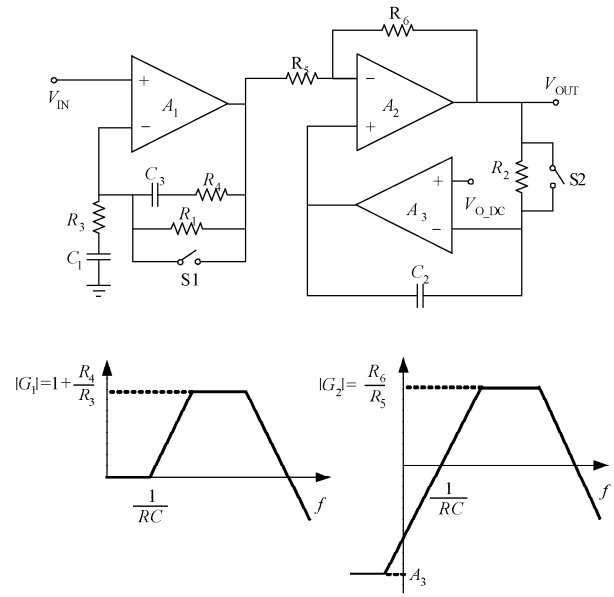

Fig. 4 DC cancellation and baseband amplifier

$$A_F(s) = \frac{A_3}{1 + s(A_3 + 1)R_2C_2} \tag{2}$$

where s is the Laplace operator. The DC gain is A_3, and the 3dB frequency is lowered by A_3 times as $1/A_3R_2C_2$ due to the Miller effect. When frequency increases, the gain of the feedback path drops and brings litter infection on the signal amplification. So the second stage signal gain is mainly determined by R_5 and R_6. VO_DC is the DC reference, which sets up the output DC voltage.

The signal bandwidth of each stage is determined by both the high pass pole from DC cancellation and the low pass pole from the bandwidth limitation of the OPAMPs. The former equals the signal gain divided by the time constant in the feedback path. The latter equals the OPAMP gain bandwidth product (GBW) divided by the signal gain, as shown in Fig. 4.

The first stage performs the mixer output buffering and provides 12dB gain to suppress the noise in following stages while keeping the DC component unchanged. The second stage cancels the DC and provides 20dB gain. In this way, mixer buffering, DC canceling, and signal amplification is accomplished in one block.

Lowering the high pass pole lessens the impact on the signal, but increases the settling time. This problem becomes serious at the transmitting-receiving transition time where the baseband DC voltage hops because transmission is alternating between a modulated and unmodulated carrier that have different carrier powers. A low frequency high pass pole, e. g., below 10kHz, makes the settling time too long to capture the backscattered signal. A speed up circuit is added in Fig. 4. The switches S1, S2, in parallel with

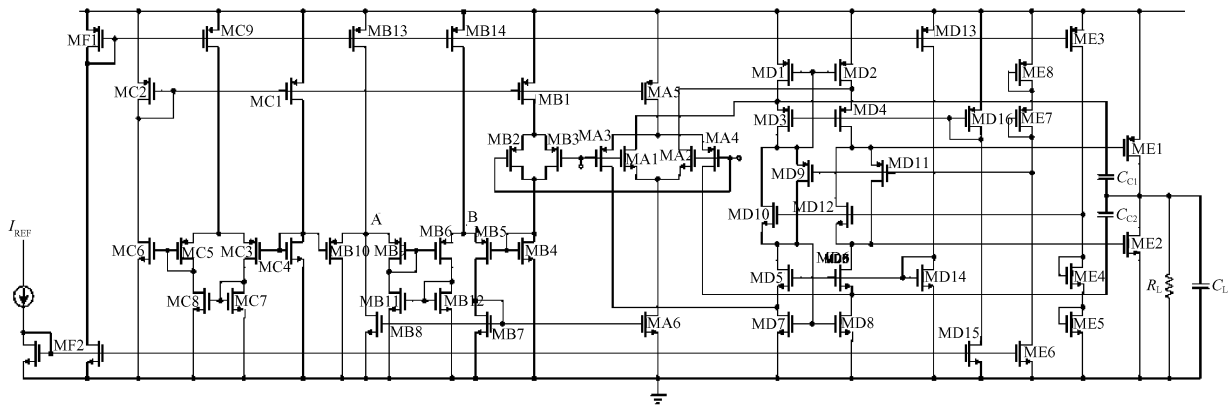

Fig. 5　Rail-to-rail amplifier

the large resistors R_1, R_2, will close at the beginning of the receiving phase to bypass the large resistor and set the high pass pole to higher frequency. After the DC component of the input is extracted and cancelled by the negative feedback, the switches will open to retrieve the signal gain.

To accommodate hundreds of millivolt DC inputs without significantly influencing the small signal gain, a 2-stage rail-to-rail amplifier is used as the elementary amplifier, as shown in Fig. 5. MA1～MA4 is the complementary input transistor to implement rail-to-rail input. MB1～MB14 is the transconductance equalization circuitry. MC1～MC9 is the calculating circuitry to equate the transconductance of pMOS and nMOS input pair. MD1～MD16 is the first stage, in form of a folded cascode. ME1～ME8 is the second stage, biased in class AB by the floating voltage source MD9～MD12 for testing purposes.

An analog filter with 3MHz 3dB bandwidth is used for anti-aliasing and noise interference rejection. Meanwhile, channel selection filtering is done in the digital baseband by a FIR filter. Considering the digital timing recovery requirement to the received signal waveform, a 4th order Bessel filter with constant group delay is designed. The Akerberg-Mossberg Biquad structure is adopted for its high tolerance to technology variation.

An automatic gain control (AGC) with built-in DC-offset cancellation is designed to adjust the input signal of ADC to 600mVpp. The 60dB dynamic range can cover the reader requirement for backscattering signal from －80 to －40dBm and give some margin. When large interference from the adjacent channel is considered, for instance, 0dBm at the second adjacent channel, the receiver dynamic range requirement needs to be extended by an extra 40dB, and this total 80dB requirement should be allocated carefully from the RF front end to the baseband.

We use a sigma-delta over sampling ADC idue to its simplicity and compatibility with deep sub-micron technology. Its high sampling rate also releases the requirement on the anti-aliasing filter. A single loop 2nd order sigma-delta modulator with 1bit quantizer for an 8bit 32 OSR sigma-delta ADC is designed. The 2nd order modulator is used because of its stability and low analog complexity. However, the power consumption is also increased because a higher over sampling ratio is required.

The highest up-link data rate is 640kHz, occupying 1.28MHz bandwidth for both FM0 and Miller coded signals. Considering the tag clock frequency excursion, 2MHz signal bandwidth is used as the design specification. Consequently, a 128MHz clock is required for 32 OSR, which requires a fast OPAMP (GBW = 780MHz in this design). A 2-stage fully differential folded cascade is designed with a 90dB DC gain, 1.4Vpp output swing, 400V/μs slew rate, and 68° phase margin, and the current consumption is 7mA. The whole modulator power consumption is 30mW.

A fractional-N frequency synthesizer is designed to cover the 860～960MHz band, providing LO for TX/RX and driving the clock generator. An in-band phase noise of －80dBc/Hz is achieved in 60kHz bandwidth. The current consumption is 10mA.

4　Measurement results

The receiver is integrated in a reader transceiver chip that also includes a frequency synthesizer and a transmitter. The chip is fabricated in an SMIC 0.18μm CMOS 1P6M mixed signal process. The chip area is 3.2mm × 3.5mm and the receiver occupies about 6mm^2. The receiver consumes 90mA from a 1.8V supply. The chip micrograph is shown in Fig. 6.

To measure the conversion performance, an ASK modulated carrier with a given modulation depth is

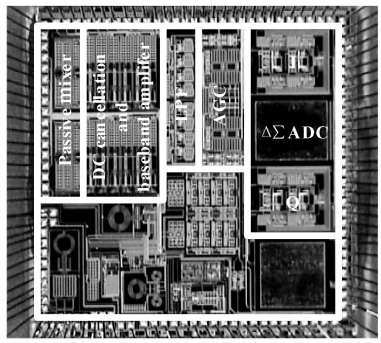

Fig. 6 Chip micrograph

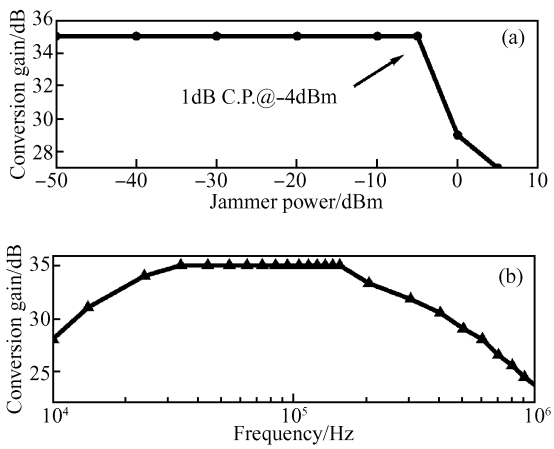

Fig. 7 Measured input P_{1dB} and conversion gain

amplified and fed into the receiver to emulate the carrier leakage and signal. The measured conversion gain is 35dB (passive mixer + baseband amplifier), and the input 1dB compression point is −4dBm (when the carrier jammer is −4dBm, small signal gain drops by 1dB), as shown in Fig. 7.

When a pure carrier generated by reader transmitter and amplified by an off-chip PA is fed into receiver, the noise performance of the receiver with strong carrier jammer can be measured. Figure 8 shows that the baseband DC cancellation amplifier output noise is about −70dBm/1kHz when −5dBm

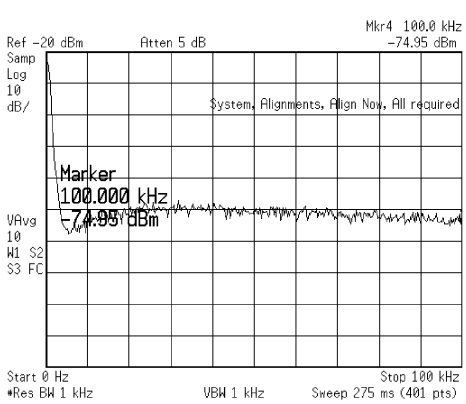

Fig. 8 Baseband amplifier output noise with −5dBm carrier jammer

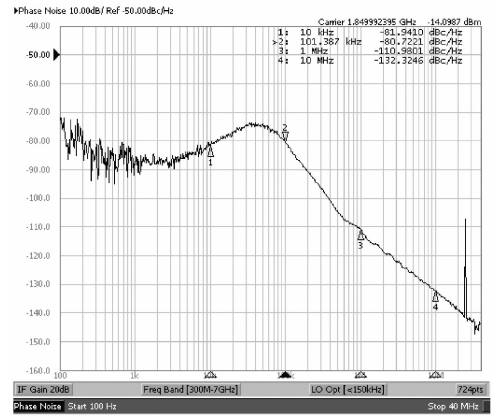

Fig. 9 Measured phase noise of fractional-N frequency synthesizer

carrier leakage is present at the receiver. With a 34dB front-end gain, the receiver sensitivity is −70dBm in the 250kHz channel bandwidth, when 10dB SNR is required for demodulation.

The fractional-N frequency synthesizer with 60kHz bandwidth achieves an in-band phase noise of −80dBc/Hz, and a spot phase noise of −110dBc/Hz at 1MHz offset and −132dBc/Hz at 10MHz offset, consuming 10mA of current from a 1.8V supply. The measurement result is shown in Fig. 9.

The time domain waveform at the output of LPF and AGC is shown in Fig. 10 (a), where a complete analysis is captured. The ADC output data is acquired by an Altera FPGA, and displayed in SignalTap. Figure 10 (b) shows the detail of a digitized RN16 returned by tag. The OSR remains at 8 after decimation for further processing.

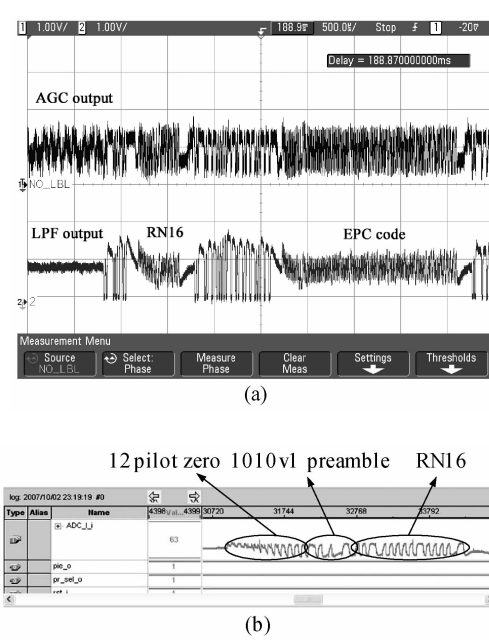

Fig. 10 Time domain waveform of output signal of LPF and AGC (a) and digitized RN16 with preamble in 8 OSR (b)

Table 1　Performance summary and comparison

	Scott *et al*.[9]	Ickjin *et al*.[10]	Wang *et al*.[11]	This work
Supply	N/A	1.8V	N/A	1.8V
Technology	0.18μm SiGe	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS
Sensitivity@ jammer	−78～−85dBm@ 0dBm	−70dBm@ N/A	−70dBm@ −5dBm	−70dBm@ −5dBm
Input P_{1dB}	11dBm	8dBm	3.5dBm	−4dBm
Power	Total:1.5W	RX:4mA	RX:105.6mW	RX:90mA

In Table 1, the main performances are summarized and compared with several reader transceiver ICs published in recent years. This work shows a comparable receiving performance in a CMOS process with a 1.8V supply.

5　Conclusion

A 0.18μm CMOS direction conversion receiver is designed and validated for an integrated 900MHz RFID reader transceiver chip. The whole receiver consumes 90mA of current from a 1.8V supply, and occupies about 6mm^2 of chip area. Measurements show a −70dBm sensitivity is achieved in the presence of a −5dBm carrier jammer, when 10dB SNR is required for demodulation.

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一种用于 900MHz 射频识别(RFID)读写器芯片的 1.8V CMOS 直接变频接收机*

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摘要：设计了针对解决 900MHz RFID 读写器收发机芯片中本地载波干扰问题而优化的直接变频接收机，并在 0.18μm 1P6M 混合信号 CMOS 工艺上实现验证.设计中使用了一种串联反馈结构的基带放大器以达到同时实现无源混频器输出缓冲，直流消除以及信号放大的功能.实际测量显示，该接收机的输入 1dB 压缩点为 −4dBm，当中频信号解调信噪比要求为 10dB 时，可达到的灵敏度为 −70dBm.该接收机与整个收发机集成在同一块芯片中，使用 1.8V 电源电压，工作时静态电流为 90mA.

关键词：直接变频接收机；直流消除；读写器；射频识别

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