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A Ka Broadband High Gain Monolithic LNA with a Noise Figure of 2dB

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Abstract: A four-stage monolithic microwave integrated circuits (MMIC) low noise amplifier (LNA) operating from 23 to 36GHz is reported using commercially available 0.15μm PHEMT technology. The LNA is self-biased. To achieve a low noise characteristic, careful optimizations of gate width are performed to reduce gate resistance. Absorption circuits and an elaborate bias structure with a resistor-capacitor network are employed to improve stability. Multiple resonance points and negative feedback technologies are used to widen the bandwidth. Measurements show a noise figure (NF) of less than 2.0dB, and the lowest NF is only 1.6dB at a frequency of 31GHz. In the whole operation band, the LNA has a gain of higher than 26dB, and an input return loss and output return loss of more than 11 and 13dB, respectively. The output power at 1dB compression gain of 36GHz is about 14dBm. The chip area is 2.4mm×1mm.

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1 Introduction

LNA is one of the key components in a receiver system. With the development of millimeter wave (MMW) wireless communication, more high performance MMW LNAs are required for MMW systems. The NF is the most important factor with respect to the sensitivity of the receiver system. Moreover, high gain, small reflection, and stability are also strictly required. Because of high density of two-dimensional electron gas (2-DEG) and high electron mobility, a PHEMT with a T-gate is suitable for a high gain and low noise amplifier.

As reported in previous papers, 0.15μm PHEMT technology can obtain an NF of 1.6dB at a single frequency point of 28GHz and the gain is 22.8dB[1]. However, it is not easy to get both a low NF and a high gain for a broadband LNA. Though lower NF and wider bandwidth can be achieved simultaneously with more costly 0.1μm PHEMT technology and a balanced amplifier structure[2,3], it occupies a larger chip area than a single-ended amplifier. In this work, an LNA without a balanced structure is successfully designed in 0.15μm PHEMT technology, and it simultaneously achieves high gain, low noise, and broadband characteristics. This LNA has the best characteristics among the single-ended amplifiers reported up to now[1,4,5].

2 Circuit design

Since the transistors in this technology are depletion PHEMTs, they are often biased by two power supplies. In order to make it more convenient for application, we use a self-bias structure to bias the PHEMTs, as shown in Fig. 1. Thus, only one positive power supply is needed. However, the PHEMT layout has two symmetrical source nodes. To avoid asymmetry when RF current flows in the two source nodes, the same two capacitors C_s should be placed at each side of the source nodes, also as shown in Fig. 1.

The main issue for LNAs is the NF. The first stage and second stage transistors have the greatest impact on the NF. From the noise model equivalent circuit of the PHEMT shown in Fig. 2[6], the gate resistor R_g is one of the most important factors that influence the NF and the gate resistor R_g should be as

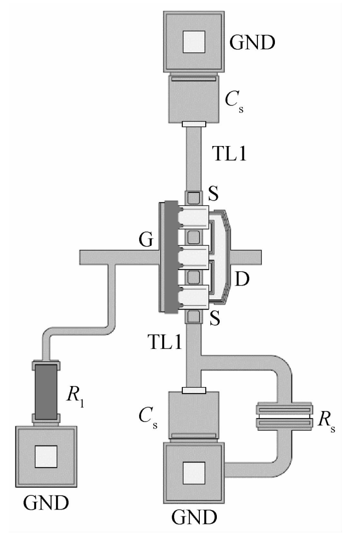

Fig. 1　Self-bias structure and absorption circuit

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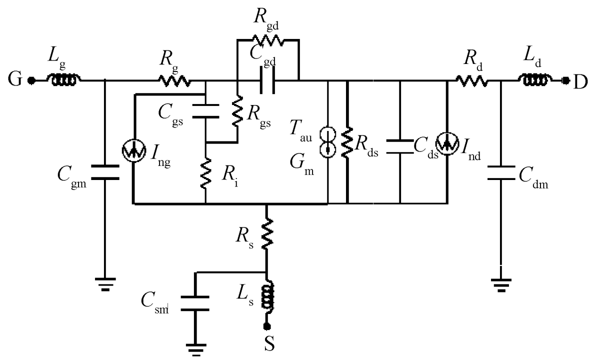

Fig.2 Noise model equivalent circuit of PHEMT

Table 1 NF_{min} and associated gain simulation results of different PHEMTs

N	$W_U/\mu m$	NF_{min}/dB	G_{assoc}/dB
1	120	1.905	4.73
2	60	1.344	6.016
4	30	1.018	6.263
6	20	0.872	6.205

small as possible.

In the design kit, R_g is given by Eq.(1).

$$R_g = 0.069 \times W_U / N \tag{1}$$

where W_U is the unit gate width of the PHEMT. So if the total gate width (W) is fixed, R_g is in square inverse proportion to the number of gate fingers (N). Supposing the total gate width is fixed as 120μm, we simulated the minimum NF (NF_{min}) and associated gain (G_{assoc}) with different finger numbers and unit gate width. The simulation results are shown in Table 1. After careful optimization, we select 6 fingers and a 20μm unit gate width for the first stage and second stage transistors.

Stability is also significant for LNAs. Because of the parasitic effect of the resistor and the capacitor in the self-bias circuit, oscillation is easy to generate[7]. In fact, for a multi-stage high gain amplifier, stability is a challenge. As shown in Fig. 1, an absorption circuit structured by a resistor in series with a micro-strip is set at each gate node of the last three stages.

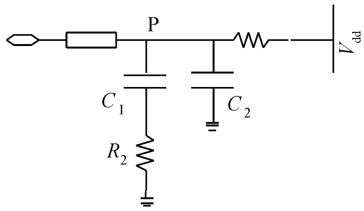

Fig.3 Bias circuit of first stage

We do not put the resistor at the first stage, otherwise it will increase the NF. Some trade-offs between stability and NF has been made when determining the value of the resistors. For the three resistors, smaller resistances should be chosen for the second stage, and the resistances in the third and the fourth stages are increased step by step. They are respectively 3, 18, and 60Ω. The absorption circuit can efficiently suppress the high gain in the low frequency band and prevent oscillation. The drain bias structure for the first stage we adopted can also prevent low frequency band oscillation[8], which is especially suitable for broadband amplifiers[9]. As shown in Fig. 3, a 5Ω TaN resistor R_2 is added between the capacitor C_1 and ground, and capacitor C_2 is directly connected to ground, where C_1 is 0.7pF and C_2 is 2pF.

Four stage PHEMTs are used to construct the circuit and a high gain of more than 26dB can be obtained. Four different resonance frequency points can be set in the circuit. Therefore, combining the four resonance points creates a broadband characteristic. In addition, as shown in Fig. 1, the micro-strip TL1 at source node is equivalent to an inductor, and the capacitor C_s is for the bypass. So TL1 has a function of current-voltage feedback, which can widen the bandwidth and improve the stability as well. As a result, the LNA achieves a broadband operation band from 23 to 36GHz.

Figure 4 is the schematic of the LNA, and the fabricated monolithic LNA micrograph is shown in Fig. 5. The chip size is 2.4mm×1mm.

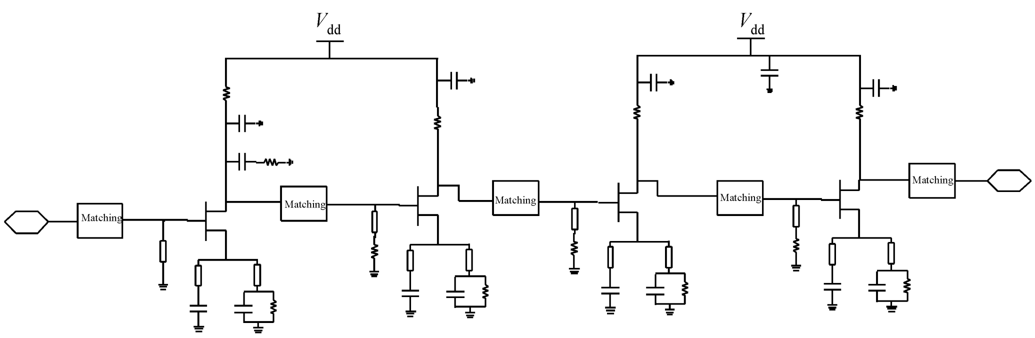

Fig.4 Schematic of the LNA

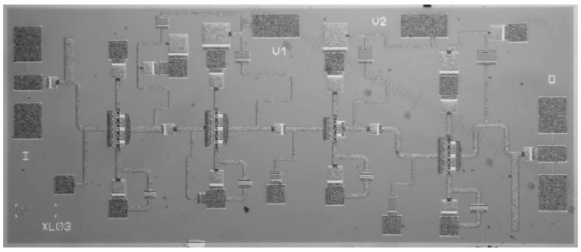

Fig.5　Micrograph of the LNA chip

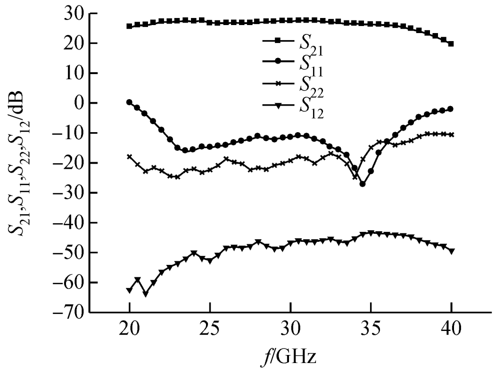

Fig.6　Measured *S*-parameters

3　Experimental results

The performance of the monolithic LNA was measured on a CASCADE Model 12000 probe platform with a DC bias of 3.0V. The total DC current was 71mA. The *S*-parameters were measured on a HP8722D network analyzer, which is shown in Fig. 6. The noise figure was measured on an AV3985 noise analyzer. The measure range of the noise analyzer AV3985 is separated into two bands: up to 26.5GHz and from 26.5 to 40GHz. For this LNA, NF measurement is separated into two parts, as shown in Fig. 7.

Figure 6 shows that in the band from 23 to 36GHz, the gain is higher than 26dB, the input return loss is more than 11dB, and the output return loss is more than 13dB. Figure 7 shows that the NF is less than 2.0dB over the whole operation band, and at a frequency of 31GHz, it is only 1.6dB.

At the same time, we measured the P_{1dB} at 36GHz with the network analyzer. Figure 8 displays a P_{1dB} of 14dBm.

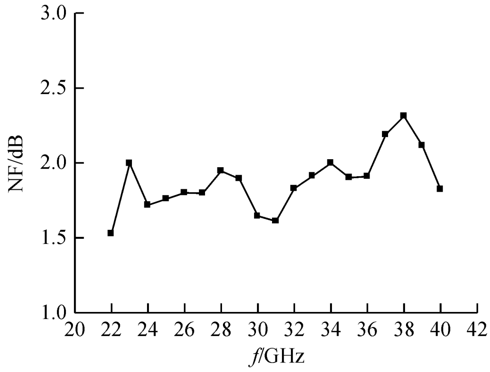

Fig.7　Measured noise figure

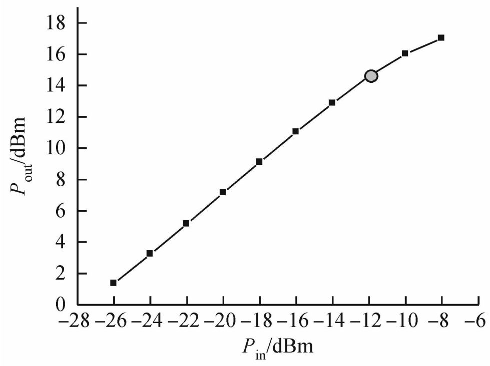

Fig.8　Measured P_{1dB} at 36GHz

A comparison of the main performances of in-market and published Ka-band MMIC LNAs is summarized in Table 2.

Table 2 demonstrates that our LNA with 0.15μm PHEMT technology has better characteristics than the single-ended LNA in Ref.[5] on NF, gain, reflection, and operation bandwidth. Our LNA is cascaded with 4-stage PHEMTs rather than the 3-stage PHEMTs in Ref.[5], so the former can get adequate gain and the matching for the first stage PHEMT is mainly designed for optimal NF. Also different from Ref.[5], the two source nodes of the first stage PHEMT in this work are both connected to ground, which can reduce the source resistance (R_s), lowering the NF. Moreover, the resistor at the input of the first stage is a main source of noise, so there is no resistor at the gate node of the first stage PHEMT in our design, unlike the design of Ref.[5], in which there is a resistor as an ab-

Table 2　Comparison among Ka-band MMIC LNAs in-market and published

Reference	Technology	*f*/GHz	Gain/dB	NF/dB	Input RL/dB	Output RL/dB
[7]	0.15μm PHEMT 3MI	28～36	23	2.3	≥8	≥8
[8]*	0.1μm PHEMT	24～40	24(typical)	1.7(typical) (Max.2.1)	12	14
[9]*	0.1μm HEMT	20～40	20	≤2.5	—	—
This work	0.15μm PHEMT	23～36	≥26	≤2	≥11	≥13

* balanced amplifier

sorption component. For these reasons, a lower NF than Ref. [5] has been obtained. In this work, we adopt the structure of a single-ended amplifier. This structure avoids the NF increase caused by the input LANGE coupler, which is often used in a balanced amplifier. Compared with the two balanced LNAs in Refs. [2,3], which are fabricated with more costly 0.1μm technology, our LNA shows an approximately equal, or even lower NF. In addition, our LNA occupies less chip area than these two balanced amplifiers.

4 Conclusion

A Ka broadband LNA with high gain and low noise figure was reported in this paper. Optimization of gate width was adopted to reduce the NF. To improve the stability, we designed absorption circuits and an R-C bias network. We used multiple resonance points and source negative feedback technologies to widen the operation bandwidth. In the band from 23 to 36GHz, the NF is less than 2.0dB, the gain is higher than 26dB, the input return loss is more than 11dB, and the output return loss is more than 13dB.

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2dB噪声系数的Ka波段宽带高增益单片低噪声放大器

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摘要: 报道了一种基于商用0.15μm赝配高电子迁移率晶体管工艺的单片低噪声放大器,工作频率范围为23～36GHz.它采用自偏置结构.对晶体管栅宽进行了优化设计减小栅极电阻,以得到低的噪声系数.采用吸收回路和加电阻电容网络的直流偏置结构提高电路稳定性,用多谐振点方法和负反馈技术扩展带宽.测试结果表明,其噪声系数低于2.0dB,在31GHz处,噪声系数仅为1.6dB.在整个工作频带范围内,增益大于26dB,输入回波损耗大于11dB,输出回波损耗大于13dB.36GHz处的1dB压缩点输出功率为14dBm.芯片尺寸为2.4mm×1mm.

关键词: 微波单片集成电路;低噪声放大器;Ka波段;噪声系数;高增益

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