A Fully Integrated Low Power Transmitter in an 802.11b Transceiver System

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Abstract: A fully integrated low power transmitter for an IEEE 802.11b transceiver system is implemented in SMIC 0.18μm technology. The direct-conversion transmitter includes two Chebyshev I low pass filters, two PGAs, a SSB mixer, and a PA driver. The transmitter provides a gain control of 32dB in 3dB steps. The maximum output power is −3.4dBm and the EVM is 6.8%. The power consumption of the transmitter is only 57.6mW with a 1.8V power supply. The chip area of the transmitter is 1.6mm×1.6mm.

Key words: 802.11b; direct-conversion; class A & C amplifier
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1 Introduction

In recent years, there has been increasingly rapid development in wireless networks. Wireless networks are seen as the technology that will enable the most convenient link between existing wired networks and portable computing and communication equipments, such as laptop computers and PDAs, at offices, hotels, companies, and campuses[1]. IEEE 802.11b is one of the wireless local area network (WLAN) standards using the unlicensed 2.4GHz ISM band. It provides the maximum data rate of 11 Mbps operating within 100 meters.

In this paper, a fully CMOS integrated low power transmitter for 802.11b WLAN applications is presented. Two transmitter architectures are also discussed.

2 Transmitter architecture

There are two categories of transmitter architectures: direct-conversion transmitters[2,3] and two-step transmitters[4,5]. The latter is superior on I/Q matching since its quadrature modulation is performed at lower frequencies[6]. However, the need of an image rejection filter, which is difficult to implement in integrated form, makes it less attractive than the direct-conversion transmitter. In this paper, the direct-conversion transmitter architecture, shown in Fig. 1, is exploited. It consists of two Chebyshev I low-pass filters, two programmable gain amplifiers (PGAs), an SSB mixer, and a PA driver. In order to relax the PA's pull on the voltage controlled oscillator (VCO) frequency, VCO runs at twice the carrier frequency. Then we use a divide-by-two circuit to generate quadrature LOs.

3 Circuit implementation

3.1 Reconstruction filter

The output of DAC needs a reconstruction filter to attenuate the higher order spectral copies and wide band noise to an acceptable level before frequency up-conversion in the mixer. A fourth-order Chebyschev I filter is implemented, which is a cascade of four leapfrogs realized by opamp R-C integrators, as shown in Fig. 2. A 4bit word is used to tune the cutoff frequency from 6 to 15MHz to compensate for process, voltage, and temperature (PVT) variations. The filter is simulated with an in-band ripple of 0.5dB at a nominal bandwidth of 10MHz.

3.2 PGA

A shunt-shunt feedback amplifier is designed to

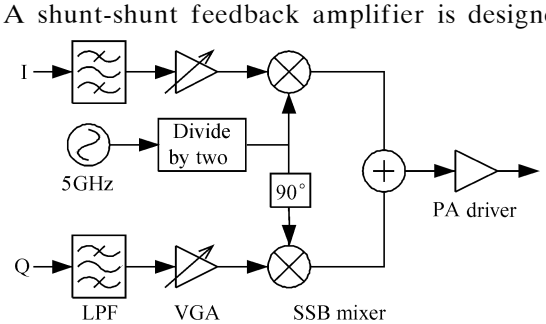

Fig. 1 Transmitter architecture

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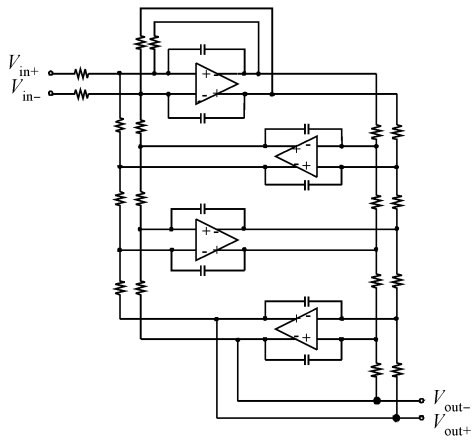

Fig. 2 Chebyshev I filter

realize power control, as shown in Fig. 3(a). The gain of the amplifier equals the ratio of the feedback resistor to the input resistor. A 3bit word is used to tune the gain from 0 to −20dB in 3dB steps, as shown in Fig. 3(b). There is a compromise between the number of the control steps and the stability of the amplifier. The more control steps are, the greater the phase delay of the feedback signal is, and the less stable the amplifier is.

3.3 SSB mixer

The SSB mixer consists of a linear transconductance input stage and a double balanced Gilbert cell[7], as shown in Fig. 4. The transconductance input stage is the main source of nonlinearity. In this paper, a high linearity transconductance stage is implemented with a negative feedback loop and a cascade current mirror. The linearity of the Gilbert cell is sensitive to

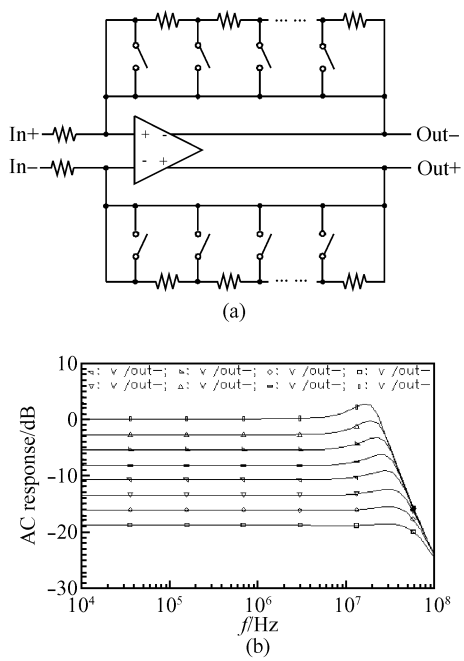

Fig. 3 Programmable gain amplifier (a) Circuit architecture; (b) AC simulation result

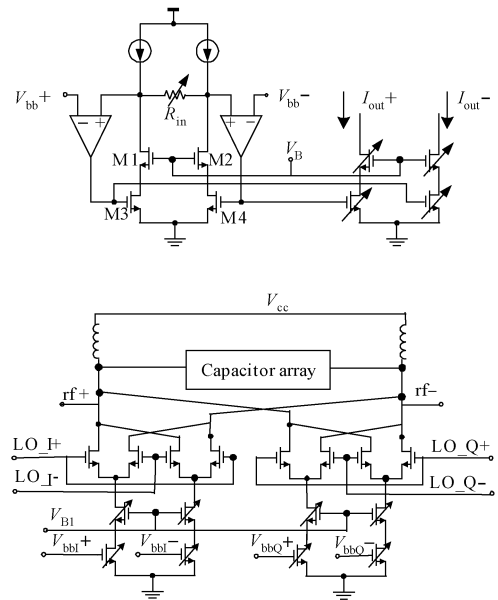

Fig. 4 SSB mixer

the amplitude of the LO. As shown in Fig. 5, (I) when $A_{LO}<1.8\Delta V_{in}$, I_{out} is very sensitive to A_{LO}, and thus, the output of the mixer is sensitive to the I/Q mismatch, which will deteriorate the sideband rejection ratio and decrease the overall EVM performance of the transmitter; (II) when $A_{LO}>2\Delta V_{in}$, I_{out} reaches the saturation region and a larger A_{LO} has little improvement in the conversion gain of the mixer but consumes much more power in LO buffers. Considering the parasitic capacitances, when a gate is overdriven, the common source voltage is overdriven too, which results in a spike in current. In the extreme case, this spike can cause transistors to leave the saturation region[8]. In conclusion, an appropriate compromise among linearity, conversion gain, and power consumption is obtained when $2\Delta V_{in} < A_{LO} < 2.5\Delta V_{in}$. The mixer achieves an IIP3 of 25dBm at the maximum gain of 0dB. The total gain control range is 12dB, with 3dB steps, by changing the input resistor and the current gain of the current mirror.

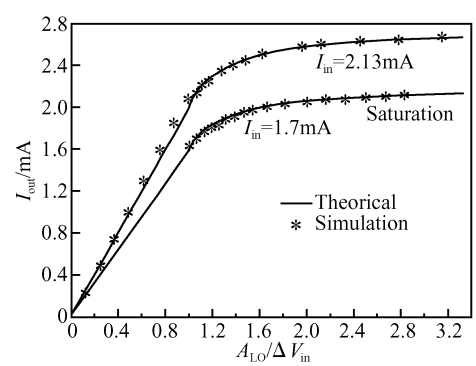

Fig. 5 Mixer's output current versus LO amplitude

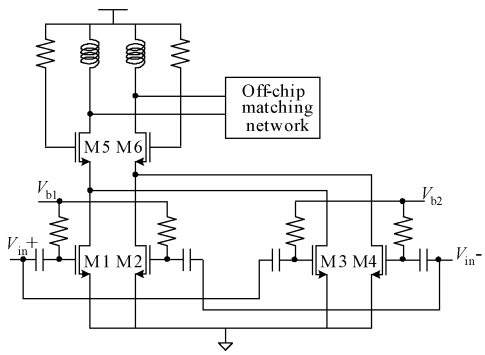

Fig. 6　PA driver

3.4　PA driver

The PA driver is a parallel combination of a class A and a class C pseudo-differential amplifier, as shown in Fig. 6. In the pseudo-differential pair, the sum of V_{gs} remains constant as long as the input voltage is perfectly differential, which makes it outperform the differential pair in linearity. One drawback of this design is lack of input common mode rejection. The cascade structure is used to alleviate the oxide breakdown problem and to improve the input-output isolation. With a proper ratio of sizes between class A biased M1 (M2) and class C biased M3 (M4), a parallel class A & C amplifier achieves a larger linear range and a much lower power consumption. The transconductance of the class A & C amplifier is a combination of the transconductance of the class A and class C amplifiers.

$$g_{mA\&C} = g_{mA} + g_{mC} \tag{1}$$

As seen in Fig. 7(a), the class A amplifier is the main transconductance contributor at low signal levels. However, the g_m of the class A amplifier starts to decrease rapidly as the input signal level increases. In contract, the g_m of the class C amplifier increases as the input signal level increases, thus compensating the gain compression of the class A amplifier. The 1dB compression point improves from 3.7 to 5.6dBm with an additional class C amplifier, as shown in Fig. 7(b). The dc power consumption increases little since the biasing voltage of the class C amplifier is lower than the threshold voltage of the transistor. The current consumption of the class A & C amplifier is 8mA.

4　Measurement results

A fully integrated low power transmitter in an 802.11b transceiver system is implemented in SMIC 0.18μm CMOS technology. The die area of the transceiver is 2.7mm × 4.2mm, in which the transmitter area is 1.6mm × 1.6mm. The power consumption of the transmitter is only 57.6mA with a supply voltage of 1.8 V. The die photo is shown in Fig. 8 and the PCB test board photo is shown in Fig. 9.

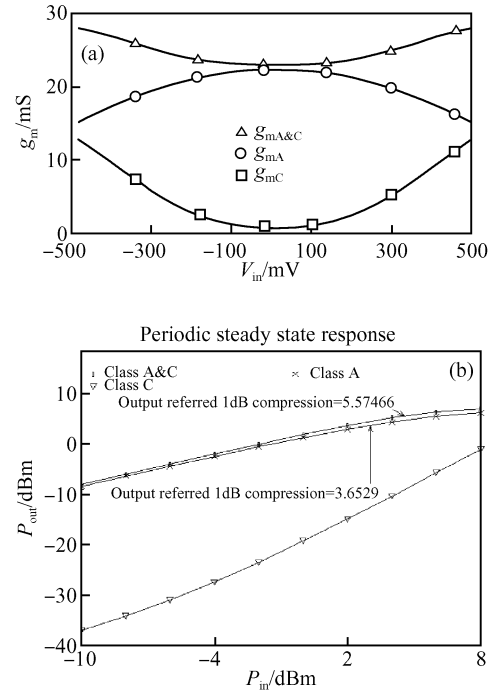

Fig. 7　(a) Transconductance; (b) 1dB compression point

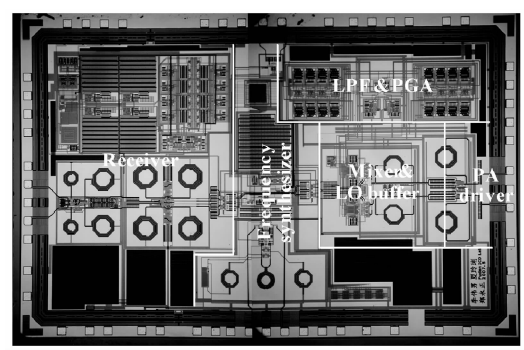

Fig. 8　Transceiver chip microphotograph

An off-chip matching network is designed to match the differential PA driver output to 100Ω, and then a balun (TDK HHM1520) is used to convert the differential signal to a single-ended signal. As seen in Fig. 10, S_{22} is less than −13dB from 2.4 to 2.48GHz.

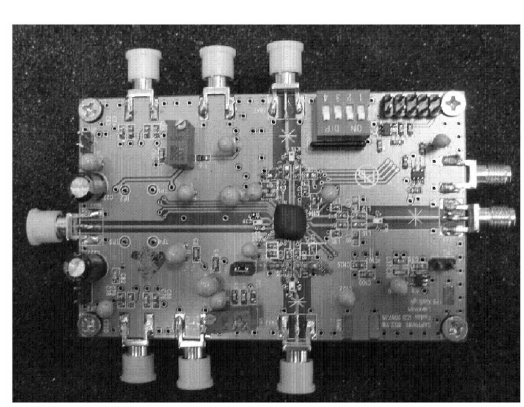

Fig. 9　PCB test board photo

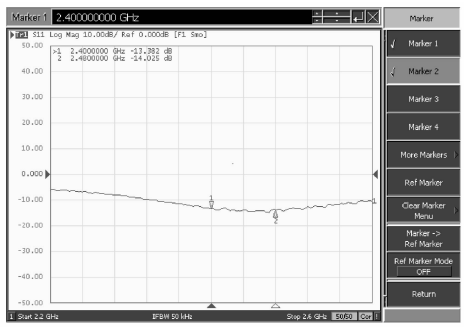

Fig. 10 S_{22} trace of transmitter

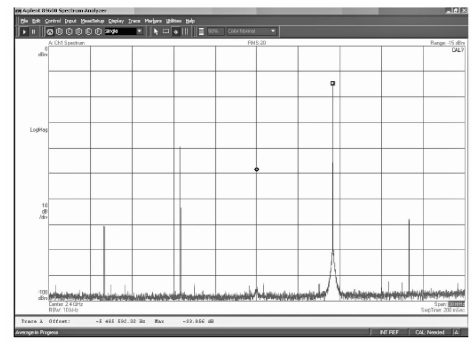

Fig. 12 Carrier and sideband suppression ratio

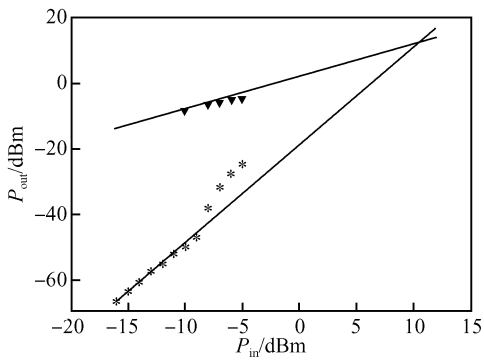

Fig. 11 OIP3 measurement result

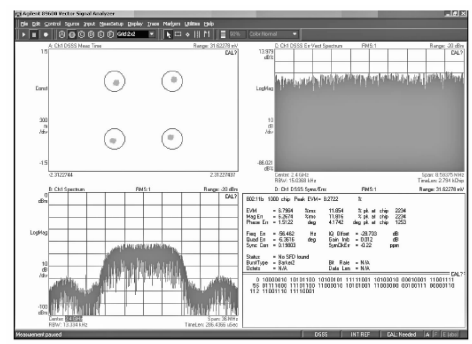

Fig. 13 EVM test

Figure 11 illustrates the measurement result of the third-order output intercept point (OIP3) by a two-tone test. The OIP3 of the transmitter is 12.7dBm. Figure 12 presents the carrier suppression and sideband suppression performance of the transmitter. With a 6MHz and 670mV peak-to-peak amplitude quadrature input signal, the carrier and sideband suppression ratio is 34 and 25dB, respectively.

Figure 13 indicates that the measured error vector magnitude (EVM) of the transmitter is 6.8% with a QPSK modulated input signal. The transmitter output spectrum at the output power of −6.4dBm is shown in Fig. 14. Considering the 3dB power loss of balun and cable, the maximum output power of the transmitter is −3.4dBm. A summary of the measured results and a comparison with previously published papers is shown in Table 1.

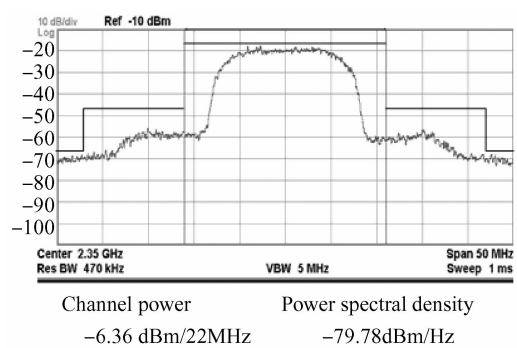

Fig. 14 Transmitter output spectrum

Table 1 Summary of transmitter performance and comparison

Reference	[3]*	[4]	[9]*	[10]*	[11]*	This work	Spec
Supply voltage/V	1.8	2.5	2.8	1.8	1.2	1.8	N/A
Power/mW	126**	182.5**	128.8**	66	125**	57.6	N/A
Maximum output power/dBm	0	0	−5	+6	+9.5	−3.4	+24***
EVM	/	/	/	/	/	6.8%	35%
OIP3/dBm	/	/	+15	+19.5	/	+12.7	N/A
Carrier suppression ratio/dBc	/	36	35	/	/	34	N/A
Sideband suppression ratio/dBc	>30	33	40	/	/	25	N/A
Die area/mm^2	4×4	3.1×3.1	4.6	1****	10	1.6×1.6****	N/A
Technology	0.18μm	0.25μm	0.25μm SiGe BiCMOS	0.18μm	0.13μm	0.18μm	N/A

* Working in 802.11b mode

** All Tx Chain

*** The output spectrum needs to be compliant with the spectrum mask as shown in Fig. 14, then an off-chip PA is used to amplify the output power to 24dBm

**** Die area of transmitters, in other references they are die area of transceivers

5 Conclusion

This paper presents a fully integrated low power transmitter for 802.11b application in SMIC 0.18μm technology. The mixer and PA driver are two power hungry blocks in a transmitter. In the mixer, a tradeoff is made between the linearity and power consumption. An innovative class A & C PA driver is designed to achieve better performance while consuming the same power compared to traditional class A PA drivers. These low power techniques lead to only 57.6mW total power consumption of the transmitter from a 1.8V supply voltage. The EVM of the transmitter is only 6.8%, much lower than the 35% required by the IEEE 802.11b standard. The maximum output power is −3.4dBm, and an off-chip PA can be used to further amplify the output power. The sideband suppression ratio is 25dB, which is not very good due to the mismatch of the layout.

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802.11b 收发系统中的全集成低功耗发送机设计

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摘要： 基于 SMIC 0.18μm CMOS 工艺，设计了一个应用于 IEEE 802.11b 收发系统的全集成低功耗发送机. 直接转换发送机包括两个 Chebyshev I 型低通滤波器，两个可编程增益放大器（PGA），一个单边带混频器和一个功率预放大器. 发送机以 3dB 为步长提供 32dB 增益，其最大输出功耗为 −3.4dBm，EVM 为 6.8%. 工作在 1.8V 电源电压，发送机的功耗仅 57.6mW. 发送机芯片面积为 1.6mm×1.6mm.

关键词： 802.11b；直接转换；A&C 类放大器

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