Electrical Characteristics and Reliability of Ultra-Thin Gate Oxides (<2nm) with Plasma Nitridation

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Abstract: MMT (modified magnetron typed) plasma nitridation and NO anneal are used to treat ultra-thin gate oxides in MOSFETs (metal-oxide-semiconductor field effect transistors). Dual-peak and single-peak N distributions are formed after nitridation. The dual-peak N distribution shows excellent electrical properties and superior reliability in terms of drain current, channel carrier mobility, and TDDB characteristics. The results indicate a means to extend silicon oxynitride as a promising gate dielectric for developing ultralarge scale integrated (ULSI) technology.

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1 Introduction

Ultra-thin gate oxides (<2nm) are used for high-speed core transistors to achieve a high current drive. The fabricated thin gate oxides have always been susceptible to boron penetration, deteriorating the p-channel MOSFET's performance. Extensive efforts are currently underway to identify alternative gate dielectrics for conventional silicon dioxide. N incorporation in the gate oxide can suppress boron penetration[1], and the location of N in the film impacts the electrical properties of the gate oxides[2]. The N introduced in the nitridation process also results in other merits, including high reliability in time-dependent dielectric breakdown (TDDB), suppression of interface state generation caused by hot-carrier injection[3], and a large drain current in n-channel MOSFETs at high gate voltage[4]. Therefore, nitrided oxide films as gate dielectrics in MOSFETs have been widely investigated. Due to the difficulties of integrating high k gate dielectrics, there is motivation to extend the use of nitrided gate oxides to at least the 65nm node, in particular for high-performance applications.

The conventional nitridation process is thermal annealing with N-included precursors such as NO, N_2O, and NH_3. At present, amongst the different oxide nitridation techniques available, plasma nitridation is the most promising because of the ability to incorporate large N concentrations without promoting a significant increase in film physical thickness for SiO_2. The second advantage is that the N atoms are located further away from the Si-SiO_2 interface. This has encouraged an evolution of plasma nitridation techniques, including continuous-wave decoupled plasma nitridation (CW)[5] and pulsed radio frequency DPN (pRF)[6]. The impetus for improvement has been to achieve low equivalent oxide thickness (EOT) with low gate leakage current (J_g) while maintaining high effective carrier mobility.

In this work, MMT (modified magnetron typed) plasma nitridation and conventional NO anneal in furnace are employed to fabricate gate dielectric films with both dual-peak and single-peak N distributions for 0.13μm logic device applications. The process of MMT nitridation controls the N profile for the gate dielectric. It introduces a high N concentration at the oxide surface (the polySi-SiO_2 interface) as an effective barrier to suppress boron penetration and the gate tunneling current through the gate dielectric. The NO anneal in furnace leads to a light nitridation at the SiO_2-Si interface for reliability improvements. On the other hand, the nitridation process results in a higher dielectric constant for the gate dielectric, causing a decrease in the equivalent oxide thickness.

Electrical characteristics and reliability of these gate dielectric films are investigated subsequently. The dual-peak N distribution shows higher channel carrier mobility in n-channel and p-channel MOSFETs than the single-peak N distribution. The TDDB test also demonstrates the superior reliability for this dual-peak N distribution.

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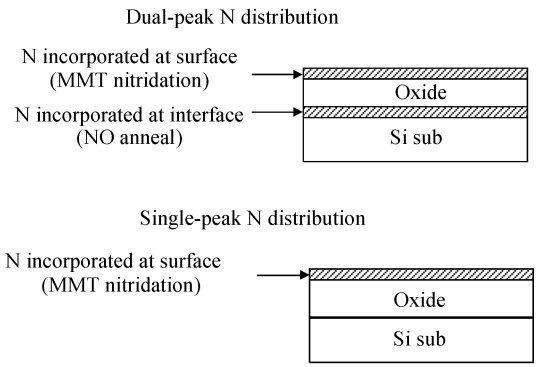

Fig. 1 Schematic illustration of dual-peak and single-peak N distribution

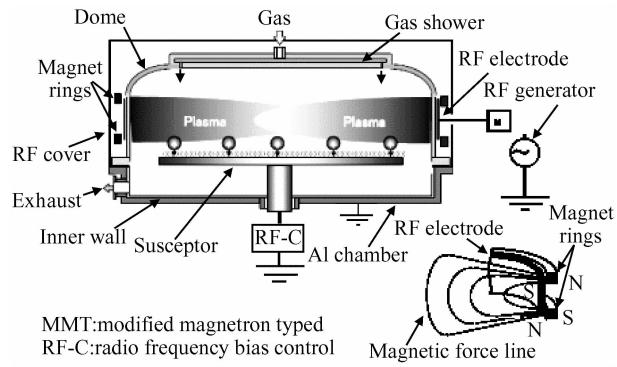

Fig. 2 Cross-sectional drawing of MMT plasma system

2 Experiment

Both n-channel and p-channel MOSFETs were fabricated with width/length = 100μm/10μm on p-type 〈100〉 silicon substrates. The MOSFETs were fabricated in 0.13μm twin-well CMOS technology and within the active region defined by the shallow trench isolation (STI) process. Prior to oxidation, the wafers were all treated by a standard RCA-cleaning followed by HF dipping and rinsing in de-ionized water. Then, the wafers were processed by furnace with thermal gate oxides of various thicknesses at 700℃, respectively. After the oxidation, some were processed with NO anneal in furnace, while the others were not. The NO anneal led to the incorporation of N at the SiO_2-Si interface. Next, the MMT plasma nitridation process was employed to incorporate N into the oxide surface. Therefore, gate oxides were formed with dual-peak and single-peak N distributions, as illustrated in Fig. 1.

The MMT low-temperature plasma processing system developed by Hitachi Kokusai Electric Inc. is an alternative nitridation technique to fabricate integrated circuits. In contrast to the plasma sources used in the past, MMT plasma is produced using an MMT RF (radio-frequency) discharge method featuring a newly devised cylindrical multipolar magnetic field electrode. This discharge mechanism produces high-density wide area uniform plasma over a wide pressure range. The magnetic force lines around the MMT plasma chamber restrict the flow of the high energy particles, allowing only the low energy particles to diffuse into the oxide films, thereby minimizing the surface damage sustained by the dielectric films[7]. The amount of impinging ions can easily be controlled in the MMT process by adjusting the impedance of the susceptor surface, making it possible to incorporate a large amount of nitrogen atoms into the film. The MMT nitridation was carried out in N_2 ambient. Figure 2 shows a schematic diagram of the MMT plasma system.

The N concentrations in these samples after nitridation were tested by secondary ion mass spectroscopy analysis (SIMS). The optical oxide thickness were measured by the Rudolph ellipsometer (MatrixS200D). Table 1 summarizes the process split and corresponding optical thickness (sample No. 01～04 for oxide thickness of 1.8nm; No. 05～08 for oxide thickness of 1.5nm; No. 09～12 for oxide thickness of 1.2nm).

The effective channel carrier mobility μ_{eff} was determined from high frequency C-V data (frequency = 100kHz) and the linear-region I_d-V_g characteristics, where I_d is the drain current and V_d = 0.05V is the drain voltage. The pulse source was supplied by a HP 8111 pulse generator. The current-voltage (I-V) measurements and time-dependent dielectric breakdown test were carried out using an HP 4156C analyzer. All measurements were performed in ambient atmosphere.

3 Results and discussion

3.1 Drain current

Figures 3 and 4 show the drain current I_d and the gate leakage current I_g versus gate voltage applied V_g obtained at drain voltage V_d = 100mV for all the gate oxides with a thickness of 1.8nm. A phenomenon of I_d degradation when V_g exceeds 1.0V is observed for

Table 1 Split for nitridation of gate oxides

Sample No.	Description	N concentration/atom%		Oxide thickness /nm
		MMT nitridation (at the surface)/%	NO anneal (at the interface) /%	
01/05/09	Double N peak	10	2	1.84/1.48/1.26
02/06/10	Single N peak	5	—	1.84/1.48/1.26
03/07/11	Single N peak	13	—	1.84/1.48/1.26
04/08/12	Double N peak	6	1	1.84/1.48/1.26

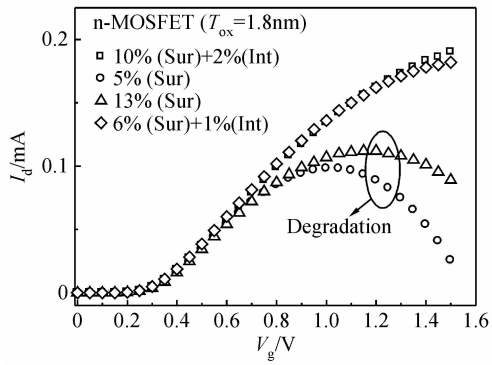

Fig. 3　Drain current of gate oxides (1.8nm) with dual-peak and single-peak N distribution

gate oxides with single-peak N distribution. This may be attributed to the gate leakage in this region as shown in Fig. 4, and thus a considerable loss of channel carriers through gate dielectric. The samples with dual-peak N distribution demonstrate excellent resistance against this electrical degradation.

3.2　Channel mobility

The impact on channel carrier mobility is a significant consideration for gate dielectrics. Equations (1)～(4) are used for effective channel carrier mobility (μ_{eff}) and effective electric fields (E_{eff}), respectively[8].

$$\mu_{eff} = \frac{I_d / V_d}{(W/L) Q_{inv}} \tag{1}$$

$$Q_{inv} = \int C_{gc}(V_{gs})\,dV_{gs} \sim C_{ox}(V_g - V_t) \tag{2}$$

$$E_{eff} = (\eta Q_{inv} + Q_B) \tag{3}$$

$$Q_B = \sqrt{2 q \varepsilon_{Si} N_B (2\Phi_B - V_{bs})} \tag{4}$$

where Q_{inv} is the inversion charge, C_{gc} is the gate to channel capacitance, V_{gs} is the gate to source voltage, C_{ox} is the oxide capacitance, V_t is the extrapolated threshold voltage, η is 1/2 for n-channel MOSFETs and 1/3 for p-channel MOSFETs, Q_B is the substrate doping concentration, Φ_B is the potential between the Fermi level and the intrinsic level, and V_{bs} is the potential between the bulk and the source.

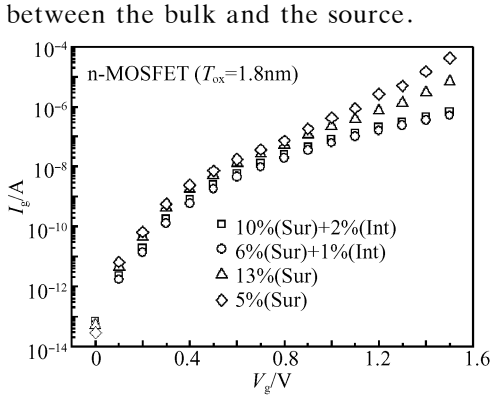

Fig. 4　Gate leakage current of gate oxides (1.8nm) with dual-peak and single-peak N distribution

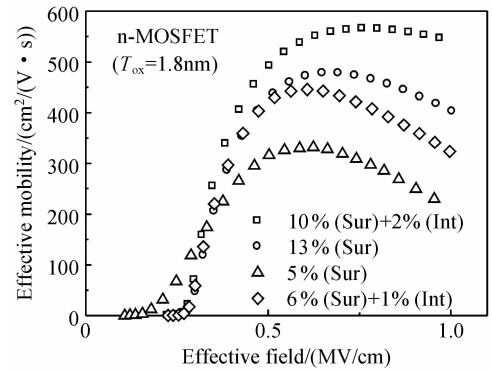

Fig. 5　Effective channel electron mobility versus effective electric field for n-MOSFET (oxide thickness = 1.8nm)

Figure 5 shows the effective electron mobility for n-MOSFETs with an oxide thickness of 1.8nm. This figure shows that the effective electron mobility increases with elevated N concentration in dielectric films. The peak effective electron mobility of the sample with dual-peak N distribution (10% at oxide surface, 2% at SiO_2-Si interface) is 18% higher than the one with single-peak N distribution (13% at oxide surface).

Figure 6 shows the effective hole mobility for p-MOSFETs with an oxide thickness of 1.8nm. When comparing all samples, no significant variation of the μ_{eff} behavior could be detected for either dual-peak or single-peak N distribution as the degree of nitridation increased. The peak effective electron mobility of the sample with dual-peak N distribution is 7% ～ 8% higher than the one with single-peak N distribution.

The Coulomb scattering induced by the interface trapped charge plays an important role in carrier transportation in MOSFET channels. The Coulomb scattering is large at the peak of mobility, but it becomes much smaller when the semiconductor strongly inverted because of the screening effect due to the inversion charge[9].

For the n-MOSFETs, the increase of electron effective mobility as nitrogen concentration increases

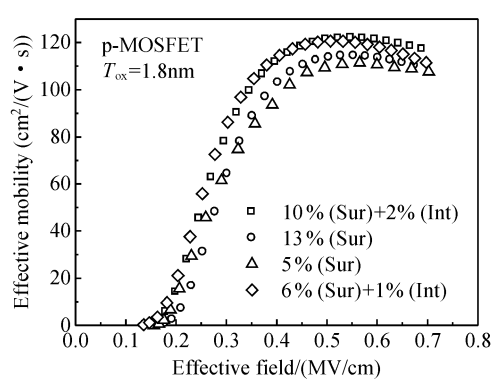

Fig. 6　Effective channel electron mobility versus effective electric field for p-MOSFET (oxide thickness = 1.8nm)

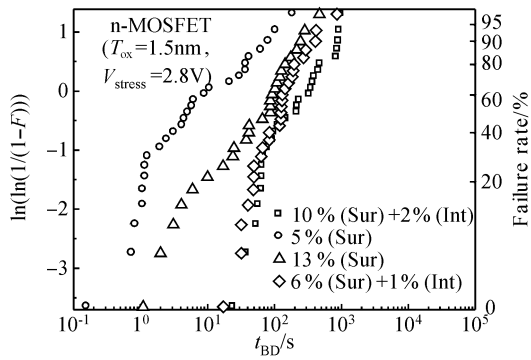

Fig. 7 Weibull plots of TDDB characteristics for n-MOSFETs with 1.5nm nitrided oxides

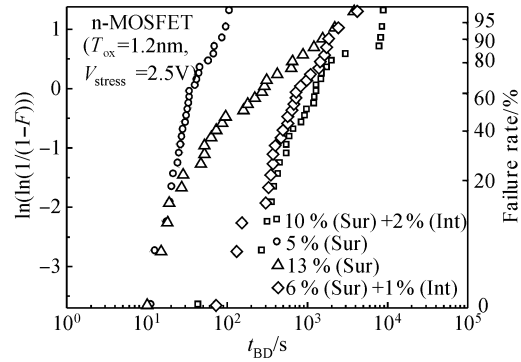

Fig. 8 Weibull plots of TDDB characteristics for n-MOSFETs with 1.2nm nitrided oxides

can be attributed to the resistance to the gate leakage current and thus keeps the mobile electrons in the inversion layer from escaping. The improvement of gate dielectrics with dual-peak N distribution is attributed to the suppression of Coulomb scattering by interface trapped charge. The N incorporated appropriately at the SiO_2-Si interface could effectively improve the interface property. For the case of p-MOSFETs, the trapped holes rapidly tunnel out of the dielectric, which results in an additional effective carrier scattering mechanism, and then in the observed reduction in hole effective mobility for all fields. The degradation of μ_{eff} in single-peak N distribution is attributed to Coulomb scattering from the worse interface property.

3.3 TDDB

The TDDB test is usually used to evaluate the intrinsic behavior and forecast the lifetime at a certain operation voltage. To shorten the test time, accelerated tests apply stress much higher than the condition under which devices are actually operated. The time-to-breakdown (t_{BD}) scales inversely with the voltage being tested. For a gate oxide thinner than 2nm, the first quasi-breakdown is considered as the failure point. The statistics of the gate oxide breakdown are described by the Weibull distribution as follows.

$$F(t) = 1 - \exp\left(-\frac{1}{\alpha}t^{\beta}\right) \tag{5}$$

where α is a constant, β is the Weibull slope, t is the stressed time, and F is the cumulative failure rate. Figures 7 and 8 exhibit the Weibull plotted TDDB characteristics for n-MOSFETs with a nitrided oxide thickness of 1.5nm (under stressed voltage V_{stress} = 2.8V) and 1.2nm (under stressed voltage V_{stress} = 2.5V), respectively.

The characteristic lifetime, 63%-time-to-breakdown (t_{BD} 63%) (the time when 63% devices have failed), is used for quantitative evaluation on the breakdown characteristic. Table 2 lists the Weibull slope (β) and the 63%-time-to-breakdown (t_{BD}) (obtained from the Weibull distribution plots) for both dual-peak and single-peak N distribution with an oxide thickness of 1.5 and 1.2nm. The samples with dual-peak N distribution (10% N at oxide surface + 2% at SiO_2-Si interface) are much higher than the others.

This result indicates that the N incorporated at the interface plays an important role in the breakdown characteristic. These N acts as a barrier to H atoms that migrate to the cathode and causes the interface to weaken by depassivating Si—H bonds[10]. Furthermore, the N incorporated at the interface relaxes the strain in the dielectric, therefore decreasing the probability of defect creation and propagation to the cathode[11]. During NO annealing of oxides, the nitridation species preferentially react with the defects in the oxides, such as Si dangling bonds and/or the Si—O—Si strained bonds to form Si—N related structures. Formation of the mismatched Si—N structure in the oxide network distorts and weakens the nearby Si—O bonds, resulting in a weak structure with more "breakable" bonds. Under stress, these weak bonds break and the traps formed migrate to the SiO_2-Si interface, thereby enhancing interface state generation and softening the SiO_2-Si interface. The increase in N at the interface increases the number of strong Si—N bonds and reduces strained Si—O bonds, thus making an interface state generated by bond breaking less probable.

Table 2 Weibull slop (β) and time-to-breakdown (t_{BD} 63%)

Sample No.	Condition	Thickness /nm	V_{stress} /V	β	t_{BD}63% /s
05	10%(Sur)+2%(Int)	1.5	2.8	1.012	324.2
06	5%(Sur)			0.594	15.77
07	13%(Sur)			0.832	88.8
08	6%(Sur)+1%(Int)			1.136	174
09	10%(Sur)+2%(Int)	1.2	2.5	0.858	1943
10	5%(Sur)			1.765	46.97
11	13%(Sur)			0.643	341.4
12	6%(Sur)+1%(Int)			1.19	981

4 Conclusion

This paper demonstrates the effect of ultra-thin gate oxides with plasma nitridation and NO annealing. The nitrided gate oxides with dual-peak and single-peak N distributions were evaluated by electrical and reliability methods. We observed that all nitrided oxides with a dual-peak N distribution exhibit significantly superior electrical properties over those with a single-peak N distribution. The results indicate a means for extending the use of silicon oxynitride as the gate dielectric for the further development of CMOS technology.

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基于等离子体氮化工艺的超薄栅氧化膜的电学特性和可靠性

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摘要：介绍了利用 MMT 等离子体氮化工艺和炉管 NO 退火氮化工艺制备的超薄栅介质膜的电学特性和可靠性.结合两种氮化工艺在栅介质膜中形成了双峰和单峰的氮分布.通过漏极电流、沟道载流子和 TDDB 的测试,发现栅介质膜中双峰的氮分布可以有效提高器件的电学特性,更为重要的是可以极大提高器件的击穿特性.这指明了延长掺氮氧化膜在超大规模集成电路器件栅介质层中应用的寿命,使之有可能进一步跟上技术的发展.

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