A New Cochlear Prosthetic System with an Implanted DSP*

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Abstract: This paper proposes a cochlear prosthetic system with an implanted digital signal processor (DSP). This system transmits voice-band signals with a low data rate through the wireless link, free of the data-rate limitation and suitable for future development. By optimizing the speech processing algorithm and the DSP hardware design, the implanted DSP manages to execute the continuous interleaved sampling (CIS) algorithm at a clock frequency of 3MHz and a power consumption of only 1.91mW. With an analytic power-transmission efficiency of the wireless inductive link (40%), the power overhead caused by the implanted DSP is derived as 2.87mW, which is trivial when compared with the power consumption of existing cochlear prosthetic systems (tens of milliwatts). With the DSP implanted, this new system can be easily developed into a fully implanted cochlear prosthesis.

Key words: cochlear prosthesis; low power; algorithm optimization; digital signal processor; power-transmission efficiency
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1 Introduction

A cochlear prosthesis is an electronic device implanted in the inner ear that can restore normal hearing to profoundly deaf people[1]. Figure 1 shows a classic structure for existing commercial cochlear prostheses. It consists of an external part and an implant. Normal sound is first picked up by the external microphone and digitized. The digital signal processor (DSP) is then used to analyze the sound and encode results into stimulating instruction trains. The transmitter modulates the trains and sends both data and energy to the implant. The implanted receiver recovers the data and energy from the wireless signals, decodes the stimulating instructions and accordingly directs the stimulator to generate electrical stimuli. Finally, the stimuli are applied to an electrode array to excite the auditory nerve. The implementation details for this kind of system can be found in Ref. [2].

However, the carrier frequency in the wireless link is kept below 20MHz (usually 5～15MHz) as the incremental electromagnetic absorption in the tissue at higher frequency may do harm to the human body[3]. As a result, the wireless data rate is limited. For example, a data rate of 500kbit/s in a 10MHz carrier is used for a 16-channel implant system with stimulating precision of 10bit and a stimulating rate of only about 900 pulses/channel[2]. This data rate should proportionally increase with channel number, pulse rate, and stimulating precision. Although there are demands for more channels, more precise stimulation, and higher pulse-rate[1], little space is left for increasing the data rate. Moreover, for any modulating method there is always a maximum data rate with a certain carrier frequency.

Fully implanted prostheses are considered to be next generation cochlear prosthetic devices. They will not suffer from the data-rate bottleneck. Because of very tight power requirements, low power analog processing methods are introduced in fully implanted prostheses[4,5]. Nevertheless, there are obvious disadvantages for analog processors: they are dedicated to a certain processing algorithm, can be imprecise, and are vulnerable to noise. Although A/D-then-DSP sys-

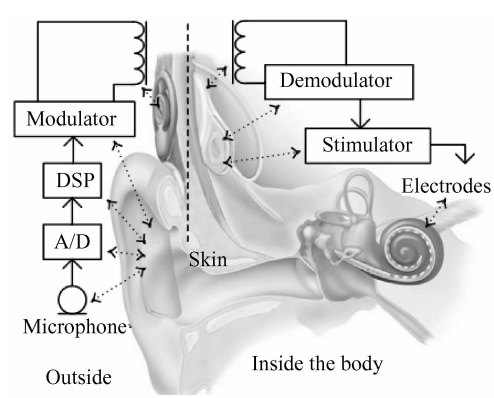

Fig. 1 Classic structure for cochlear prostheses

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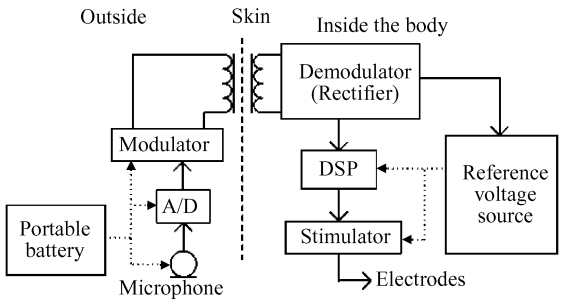

Fig. 2 Structure of the proposed prosthetic system

tems can provide a flexible and robust solution, they seem to consume too much power and can not be sustained by an implanted battery even with state-of-art technology.

Based on these considerations, this paper proposes a new system with an implanted DSP that can remove the data-rate bottleneck from classic prostheses and alleviate the tight power requirements of fully implanted systems. This system is powered by an external battery and only voice-band signals with a data rate of 100kbit/s are required to be transmitted via the wireless link. Optimizations of the speech processing algorithm and hardware implementation are carried out to ensure the low power dissipation of the system.

2 System overview

Like the classic system, the proposed system also consists of an external part and an implant, which is shown in Fig. 2. The external part combines microphone, A/D converter, and modulator while the implant is composed of demodulator, DSP, and stimulating circuit. These two parts are connected by an inductive link, via which power and data are transferred from the external circuit to the implant using a PWM scheme. This system works in a similar way to the classic system, except that the DSP is moved into the implanted part. The implanted DSP can be programmed wirelessly to update the processing algorithm. A watch-dog circuit should also be integrated in the DSP to prevent the software-based operation from failing.

The most essential advantage of this system is that only voice-band signals with low and fixed data rate, instead of a large amount of processed stimulating instructions, should be transmitted via the wireless link. The wireless data rate is independent of channel number, pulse rate, and stimulating precision. But the cost is that the implant may occupy more area and the system may consume much more power than the classic system. Comparatively speaking, the power consumption is much more of a concern in this specific application. Reducing the power consumption of the proposed system is the primary goal of this paper.

The implanted DSP is a key component as it consumes the most power in the system. Careful consideration of the signal-processing algorithm optimization, and DSP hardware design should be carried out to reduce its power consumption.

The wireless link is another key component, of which the power-transmission efficiency is critical to the power consumption of the whole system. If the wireless link is power efficient, most of the energy will be delivered to the implanted circuit; otherwise, huge amounts of power will be wasted during the transmission. Design efforts should be exerted to raise the power-transmission efficiency.

3 Low power signal-processing algorithm and hardware design

3.1 Signal-processing strategy

3.1.1 CIS algorithm

Among various signal-processing strategies developed for multi-channel cochlear prostheses, the continuous interleaved sampling (CIS) approach[6] achieves outstanding performance and has been widely used. The structure of the CIS strategy is shown in Fig. 3.

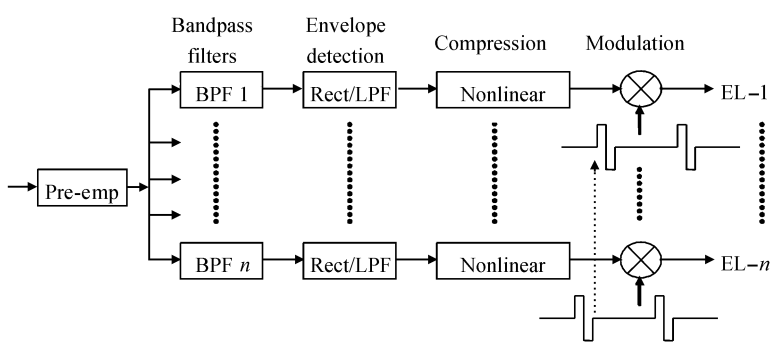

Fig. 3 Structure of CIS algorithm

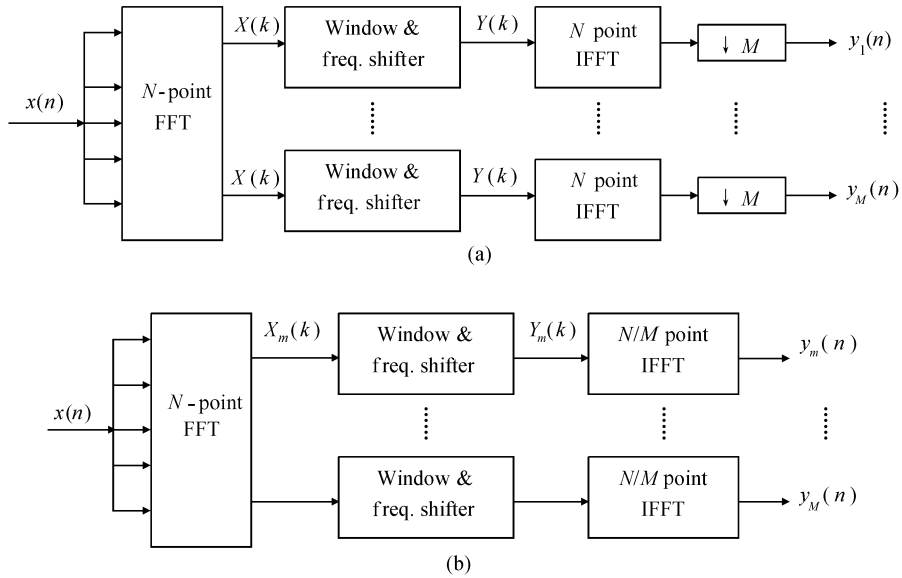

Fig. 4　(a) Prototype structure of an FFT-based filter bank ; (b) Structure of the simplified filter bank

The sound signals are first pre-emphasized and pass through a bank of band-pass filters. The envelopes of the filtered waveforms are extracted by full-wave rectification and low-pass filtering. Their outputs are then compressed and used to modulate biphasic pulses. A nonlinear compression function (e. g., logarithmic) is used to ensure that the envelope outputs fit the patient's dynamic range of electrically-evoked hearing. Trains of balanced biphasic pulses, with amplitudes proportional to the envelopes, are delivered to the electrodes at a constant rate in a non-overlapping fashion.

3.1.2　Optimization of the filter bank

In the CIS algorithm, the filter bank is the most complex component and usually takes more than 60% of the execution time. It is worthy of top-priority optimization. Figure 4 (a) shows the prototype structure of a frequency-domain band-pass filter bank. At first, an N-point FFT transforms the time-domain signals into the frequency domain. The window function is applied to extract the desired sub-band signals and frequency shifters are used to deliver each sub-band signal to the base band. These base-band signals are then transformed back to the time domain by N-point IFFT. Finally, the time-domain signals are down-sampled with a decimation factor of M since the bandwidth of each sub-band signal has been extended in the previous process of frequency division. This FFT-based filter bank can achieve any shape of frequency response with less computational complexity than IIR and FIR filters.

Theoretical analysis shows that this filter bank can be optimized to further decrease the computational complexity. As shown in Ref. [7], the IFFT and its sequential decimation filter in each channel can be merged into an N/M-point IFFT. The simplified structure of the filter bank is shown in Fig. 4(b). As we will discuss later, the simplified filter has very low computational complexity.

3.2　DSP hardware design

3.2.1　DSP with enhanced Harvard architecture

Considering the need for algorithmic diversity and application headroom, a 24bit fixed-point general-purpose DSP with enhanced Harvard architecture is adopted in our system. The proposed DSP is of typical core-memory structure, which is shown in Fig. 5. The core is composed of four main components (ALU, AGU, PCU, and IDBS) with a 3-stage integer pipeline, and the memory space is made up of three independent on-chip static RAMs——an instruction RAM (PRAM) and two data RAMs (XRAM and YRAM). Four internal data buses (PDB, XDB, YDB, and GDB) facilitate data exchange inside the DSP. To ease the processor design, the instruction set of the proposed DSP is modeled after the Motorola DSP56000[8], a widely used commercial DSP targeting audio/sound applications. Therefore, the existing commercial compiler and program library can be used.

3.2.2　Low power design methods

To reduce the power consumption of the DSP, several effective methods were introduced.

(1) The instruction set is reduced and the peripheral interface is simplified.

As the application is specified, some obscure instructions of the Motorola DSP56000 that are seldom or never used in this application are discarded. Only

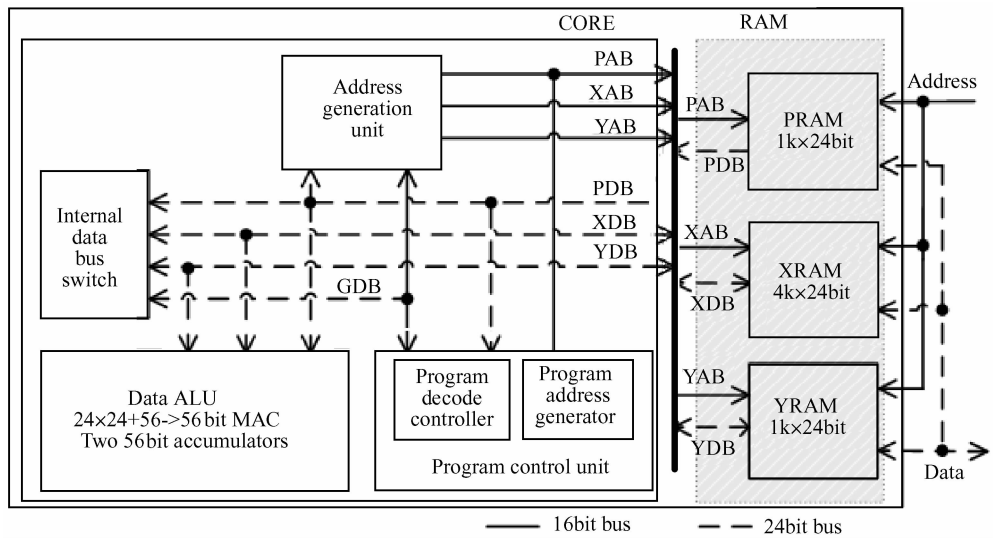

Fig. 5 Architecture of the proposed DSP

central components and the input/output interface (see Fig. 5) are reserved. The extended peripheral interface in the Motorola DSP56000 is not adopted.

(2) Clock-gating[9] is applied to reduce the power consumption of the clock network.

The global clock net of the DSP consumes a large fraction of power owing to its heavy load. Clock gating is thus applied to reduce the clock load. By gating the clock input of the register banks, the local fan-out of the clock can be cut down from a bank of registers to only a clock gating cell when the registers are not active. This approach is quite effective for the proposed DSP, as there are many register banks that have 24 or more registers and usually maintain the same value through multiple cycles.

(3) Operand isolation[10] is used to eliminate redundant activities in the DSP.

In a traditional ALU (arithmetic logic unit), input operands are directly delivered to all arithmetic operators and any change at the input will cause all parallel operators to run simultaneously. For example, in an addition instruction cycle, input changes will activate unnecessary multiplication and logic operations. Although the unnecessary arithmetic results will be discarded and not impact the operation correctness, these redundant operations still result in unnecessary power waste.

In the proposed DSP, ALU operators are isolated by placing latches at their portals, guaranteeing that only the necessary operator is activated in an ALU instruction. The enable signals of the latches are determined when the instruction is decoded. By 'freezing' the inputs to these big combined components when their outputs are not needed, unnecessary power consumption is thus avoided.

(4) Memory partitioning[11] is introduced to reduce the power consumption of the memory system.

Three static RAMs consume more than half of the total power in the proposed DSP. The main idea of the memory partitioning is to divide a monolithic large-volume memory into several small-volume sub-banks that can be independently accessed. For each access to the partitioned memory, only the addressed sub-bank is activated and the others keep inactive. The overall switching capacitance per access is thus decreased and therefore the power can be reduced. The major cost of this method is the silicon area overhead caused by duplication of the addressing and control logic of the sub-banks, and the area overhead will increase with the number of sub-banks.

To achieve both low power and small area, an optimal partitioning method is developed for the proposed DSP. The partitioning method consists of the following steps:

(a) Profile the memory access patterns to identify the most frequently accessed addresses;

(b) Divide the memory into sub-banks of different volume;

(c) Map those frequently accessed addresses into small-volume sub-banks and map the other infrequently accessed addresses into large-volume sub-banks.

This method can minimize the number of memory sub-banks and strike a balance between power reduction and area growth.

3.3 Implementation results

3.3.1 Software implementation

Three types of filter banks and the CIS algorithm are implemented on the proposed DSP. With a sampling rate f_s = 10kHz, FFT length N_{point} = 1024, and sub-band number M_{ch} = 16, the implementation result

Table 2　Comparison result of the proposed DSP

Designs	Power①	Memory size	Total area②	Sampling rate	Other features
The proposed DSP	1910μW	6K×24bit	6.44mm^2	24bit@10kHz	General-purpose
DSP in Ref.[12]	4210μW	32K×8bit	9.18mm^2	16bit@24kHz	Dedicated to CIS

① Supply voltage is 1.8V; Clock frequency is 3MHz
② Both are fabricated in 0.18μm CMOS process

is shown in Table 1. The CIS algorithm is executed with only 2.8 MIPS (million instructions per second), which can be mainly attributed to the simplified filter bank (SFFT-FB). It reduces the computational complexity by more than 80% when compared with traditional IIR (IIR-FB) and FIR (FIR-FB) filter banks.

3.3.2　Hardware implementation

With all the aforementioned low power techniques, the proposed DSP is fabricated in 0.18μm CMOS technology and the chip photograph is shown in Fig. 6. The chip has 69 I/O pins, including a 16bit address bus, a 24bit data bus (see Fig. 5), 5 control & test signal pins, and 24 power & ground pins. The DSP chip is tested by running various speech processing programs on it. At first, the test code and data are loaded into the PRAM, XRAM, and YRAM, respectively; then the DSP core is reset and begins to execute the given test program. The average power consumption is measured as the DSP performs the speech processing task. To showcase the low power merit, the proposed DSP is compared with a very low power DSP for cochlear prosthetic devices reported in Ref. [12], and the detailed result is listed in Table 2. The proposed DSP not only has low power consumption, but also has more flexibility and higher precision, which are desirable for cochlear prosthetic devices.

Table 1　Implementation result of filter banks and CIS

Type	Parameter	Complexity
IIR-FB	$N_{\text{order}} = 8$	6.7 MIPS
FIR-FB	$N_{\text{order}} = 128$	10.5 MIPS
SFFT-FB	$N_{\text{point}} = 1024$	1.3 MIPS
CIS	With SFFT-FB	2.8 MIPS

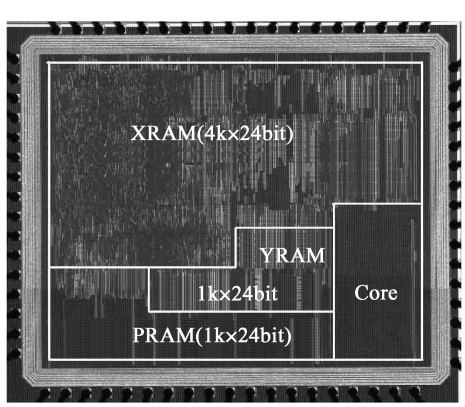

Fig. 6　Die photo of the proposed DSP

4　Power-transmission efficiency

The power-transmission efficiency of the wireless inductive link is another issue which should be addressed. Achieving high power-transmission efficiency, large data-transmission bandwidth, and coupling insensitivity are three major challenges in the design of an inductive link, which have been fully discussed in Refs. [13 ~ 15]. In practice, these three aspects trade off with each other, making the design a multi-dimensional optimization problem. When compared with the classic cochlear prosthesis, the proposed system with an implanted DSP has enormously cut down the requirement of data-transmission bandwidth, making the design of the transmission link less difficult.

Figure 7(a) shows the equivalent circuit of an inductive transmission link, in which L_1 and L_2 are two inductors with coupling factor k. In the circuit, R_{L1} and R_{L2} are the serial resistors of L_1 and L_2, respectively, i.e., $R_{L1} = \omega L_1 / Q_1$, $R_{L2} = \omega L_2 / Q_2$, where Q_1 and Q_2 are the corresponding quality factors of L_1 and L_2. For convenience, some variables are defined as follows:

$$Z = R_{L2} + \frac{1}{j\omega C_2 + \frac{1}{R_L}} = R_{L2} + \frac{R_L}{1 + j\omega R_L C_2}$$

$$Z_{L1} = j\omega L_1, Z_{L2} = j\omega L_2, Z_M = j\omega k\sqrt{L_1 L_2} \quad (1)$$

Hence, the equations of the circuit in Fig. 7(a) can be expressed as

$$\begin{cases} Z_{L1} I_1 + Z_M I_2 = V_1 \\ Z_M I_1 + (Z_{L2} + Z) I_2 = 0 \end{cases} \quad (2)$$

The result of Eq. (2) is

$$\begin{cases} Z_{in} = Z_{L1} - \dfrac{Z_M^2}{Z_{L2} + Z} \\ V_2 = \dfrac{Z_M (Z_{L2} + Z)}{(Z_{L2} + Z) Z_{L1} - Z_M^2} V_1 \end{cases} \quad (3)$$

The expression of the power-transmission efficiency η can be deduced from Eq. (3) along with

$$\begin{cases} V_L = \dfrac{Z - R_{L2}}{Z} V_2 \\ V_1 = \dfrac{I_0}{\dfrac{1}{Z_{in} + R_{L1}} + j\omega C_1 + \dfrac{1}{R_s}} \times \dfrac{1}{Z_{in} + R_{L1}} \\ \eta = \dfrac{|V_L|^2 / R_L}{\text{Real}(I_s V_1)} \end{cases} \quad (4)$$

Finally, the analytical result of η is

$$\eta = \frac{\left|\dfrac{Z_M(Z_{L2}+Z)}{(Z_{L2}+Z)Z_{L1}-Z_M^2}\times\dfrac{Z-R_{L2}}{Z}\right|^2\left|\left(j\omega C_1+\dfrac{1}{R_s}\right)(Z_{in}+R_{L1})+1\right|^2}{\mathrm{Real}\left(\left(j\omega C_1+\dfrac{1}{R_s}\right)(Z_{in}+R_{L1})R_L\right)+R_L} \tag{5}$$

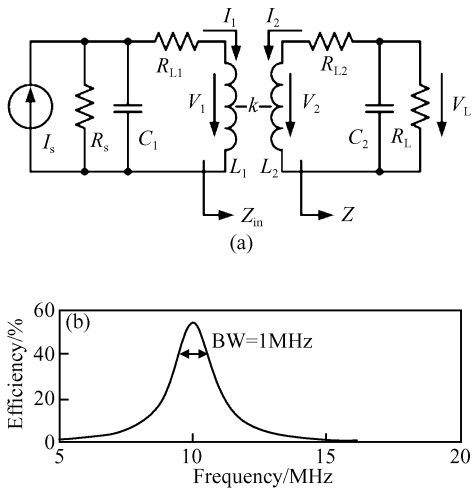

Fig. 7 (a) Equivalent circuit for frequency analysis; (b) Frequency response of transmission efficiency

Optimization towards a higher η based on Eq. (5) has been carried out by altering parameters of the circuit components in Fig. 7(a), and the optimal result is shown in Fig. 7(b). As illustrated in the figure, bandwidth more than 1MHz can be provided for data transmission while guaranteeing the power-transmission efficiency is above 40%. The choice of 10MHz as the carrier frequency is coincident with existing commercial cochlear prosthetic devices, which have been proven safe for the human body.

5 Comparison of the proposed system with the classic system

5.1 Power and area overhead

The biggest concern with the proposed system is its power consumption. Simplified block diagrams in Fig. 8 depict the different power distribution between the classic prosthetic system and the proposed system. To facilitate the analysis, it is assumed that identical components in the two systems consume the same power, and the power-transmission efficiency η also remains the same for the two systems.

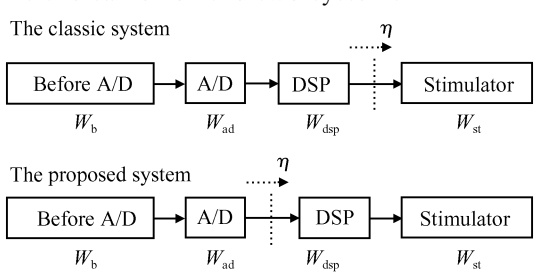

Fig. 8 Power comparison of two systems

The power consumption of the classic system (W_{cla}) and the proposed system (W_{pro}) can be respectively expressed as:

$$W_{cla} = W_b + W_{ad} + W_{dsp} + \frac{1}{\eta}W_{st} \tag{6}$$

$$W_{pro} = W_b + W_{ad} + \frac{1}{\eta}(W_{dsp} + W_{st}) \tag{7}$$

Thus, a difference can be derived as follows:

$$W_{dif} = W_{pro} - W_{cla} = \frac{1-\eta}{\eta}W_{dsp} \tag{8}$$

The power consumption of the proposed DSP W_{dsp} is 1.91mW (see Table 2). The power-transmission efficiency η is obtained as 40% from Section 4. So, compared with the classic system, the increased power dissipation of the proposed system is $W_{dif} = (1-40\%)\times 1.91/40\% = 2.87\mathrm{mW}$.

This power overhead is almost negligible when taking the total power consumption of the whole system (tens of milliwatts) into account. Moreover, the power consumption of the proposed DSP can be further reduced by properly lowering the supply voltage and power-gating. Using advanced small-size fabrication technology (0.18μm or below), the total power of the proposed system is actually lower than existing commercial systems.

Another problem of the proposed system is the area increase of the implant caused by the implanted DSP. However, this is not really a problem. First, the cochlear implant is an assembly package consisting of not only a processing circuit, but also an inductive coil and electrodes. The circuit takes up only a small portion of room and the adoption of the implanted DSP does not necessarily increase the implant size. Second, the total area of the implanted circuit with the DSP can be reduced to smaller than that of existing commercial systems using smaller fabrication technology, just as the power consumption can.

5.2 Performance benefits

There are at least two benefits from the proposed system.

(1) Only voice-band signals with low and fixed data rate (100kbit/s, 10bit@10kHz), which are independent of channel number, pulse rate, and data precision, need to be transmitted via the wireless link. This removes the wireless data-rate bottleneck found in existing systems, promoting the further development of cochlear prostheses. Furthermore, it eases the design of the inductive link and improves the power-transmission efficiency. The speech processing is also

free of the data-rate limitation, which increases the versatility of the processing strategy and the precision of the stimuli.

(2) The proposed system can be easily developed into a fully implanted prosthesis. Fully implanted digital prostheses depend heavily on low power consumption of the implanted DSP and high power usage of the rechargeable implanted battery. The design practice on the implanted DSP will boost the development of fully implanted systems. After the DSP is implanted, the integration of the microphone and A/D converter in the implant will not be difficult.

6 Conclusion

A cochlear prosthetic system with an implanted DSP is presented in this paper. Only voice-band signals with very low and fixed data rate (100kbit/s) are required to be transmitted via the wireless link, regardless of channel number, pulse rate, and stimulating precision. With the data-rate bottleneck removed and the DSP implanted, this system is very suitable for future development.

Power consumption is the main concern of the proposed system. Measures are thus adopted to reduce the power:

(1) Optimization on the realization of the filter bank is carried out, which reduces the computational complexity of the CIS algorithm to only 2.8MIPS.

(2) Low power strategies are introduced in the design of the implanted DSP. As a result, the DSP manages to only consume 1.91mW of power when executing the CIS algorithm at a clock frequency of 3MHz.

(3) Through accurate analysis and optimal parameter selection, the power-transmission efficiency of the wireless inductive link is increased to above 40%.

By combining the above factors, the additional power consumption of the proposed system caused by the implanted DSP can be reduced to 2.87mW. This power overhead is almost negligible when taking the total power consumption of the whole system (tens of milliwatts) into account.

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一种带植入式数字信号处理器的新型人工耳蜗系统*

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摘要：提出了一种带植入式数字信号处理器的人工耳蜗系统.该系统只需在无线通道中传输低码率的语音信号,不存在数据码率受限的问题,有利于人工耳蜗未来的发展.通过优化语音处理算法和数字信号处理器硬件设计,植入式的处理器可以在 3MHz 的时钟频率下执行连续相间采样(CIS)算法,功耗仅为 1.91mW.根据理论分析得到的无线能量传输效率(40%),可以推算出由于处理器植入所增加的功耗是 2.87mW,与现有的商用人工耳蜗系统整机功耗(几十毫瓦)相比微乎其微.由于处理器的植入,新系统可以很容易扩展成全植入式人工耳蜗系统.

关键词：人工耳蜗；低功耗；算法优化；数字信号处理器；能量传输效率
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