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Back-Gate Effect of SOI LDMOSFETs*

Bi Jinshun†, Song Limei, Hai Chaohe, and Han Zhengsheng

(*Institute of Microelectronics, Chinese Academy of Sciences, Beijing* 100029, *China*)

Abstract: 0.5μm-gate-length lateral double-diffused metal-oxide-semiconductor field-effect transistors (LDMOSFETs) with low barrier body contact (LBBC) and body tied to the source (BTS) were fabricated on silicon-on-insulator (SOI) substrates. The back-gate effects on front-channel subthreshold characteristics, on-resistance, and off-state breakdown characteristics of these devices are studied in detail. The LDMOSFETs with the LBBC structure show less back-gate effect than those with the BTS structure due to better control of the floating body effect and suppression of the parasitic back-channel leakage current. A model for the SOI LDMOSFETs has been given, including the front- and back-channel conductions as well as the bias-dependent series resistance.

Key words: SOI; LDMOSFET; back-gate effect
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1 Introduction

Power lateral double-diffused transistors (LDMOSFETs) on silicon-on-insulator (SOI) substrates have attracted considerable interest for applications in high performance RF power amplifiers[1~3]. The advantages of SOI technology include the superior isolation, reduced parasitic capacitances, less leakage current, and better high temperature performance compared to the traditional junction isolation in bulk technology[4,5]. Moreover, SOI technology uses a high resistivity silicon substrate to reduce substrate RF power loss and noise crosstalk[6,7].

Breakdown voltage and on-resistance are key parameters of SOI LDMOSFETs, as discussed in Refs.[8~10]. However, the impact of the back-gate, an additional terminal introduced by the buried oxide to the LDMOSFETs, on breakdown voltage and on-resistance is seldom studied. In practice, if two SOI LDMOSFETs are used in series, the potential of the source and body of the top device in the stack is raised with respect to the back-gate. Thus, this device is biased by the back-gate although the back-gate is not biased intentionally. So it is necessary for the designers to understand the back-gate effect of SOI LDMOSFETs.

This paper discusses the back-gate effect of SOI LDMOSFETs and presents a model of SOI LDMOSFETs.

2 Device fabrication

The 40μm/0.5μm LDMOSFETs were fabricated on 100mm SIMOX (separated by implanted oxygen) wafers from Simgui Corp, with material parameters as follows: p(100), 15~25Ω·cm, 198nm-thick top silicon film, and a 382nm-thick buried oxide layer. Device A is a BTS (body tied to the source) structure LDMOSFET with a 0.5μm drift region length, and device B is a LBBC (low barrier body contact) structure LDMOSFET with a 0.3μm drift region length.

LOCOS (local oxidation of silicon) isolation was used. The gate oxide thickness is 6nm. The p^+ implantation for devices A and B was to implant boron with a dose of $1\times10^{14}cm^{-2}$ and an energy of 25keV. The n-drift region was created by a phosphorous implant of dose $8\times10^{12}cm^{-2}$ and energy 30keV. The n-LDD region (body contact region and drift region were masked) was implanted by arsenic with a $3\times10^{14}cm^{-2}$ dose and 25keV of energy. The n^+ source and drain regions were formed by a masked implant of $5\times10^{15}cm^{-2}$ and 25keV of energy. The n^+ implant mask defines the length of the drift region. The dopants were activated by a 6s, 1030℃ RTA process. In order to reduce the sheet resistance of the source, gate, and drain of the RF LDMOSFETs and improve the RF performance, a salicidation technique[11] based on SiO_2/Si_3N_4 dual sidewalls was developed and applied to thin-film SOI LDMOSFETs with thin gate oxide. The

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† Corresponding author. Email: bravehawk@126.com

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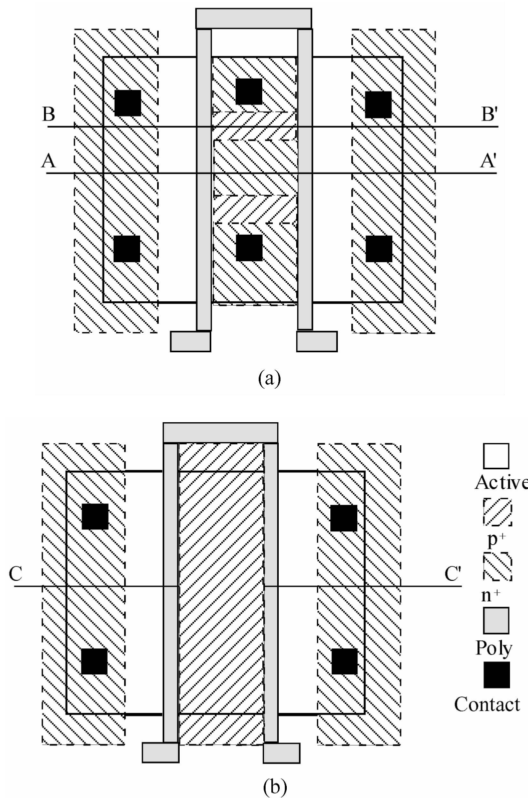

Fig. 1 (a) Layout of the BTS structure LDMOSFET for device A; (b) Layout of the LBBC structure LDMOSFET for device B

layouts of devices A and B are shown in Fig. 1, and their cross-sections along lines A-A′, B-B′ and C-C′ are illustrated in Fig. 2.

The LBBC structure LDMOSFET is close to that of a BTS structure LDMOSFET with two main exceptions: (1) The source does not extend completely through the top silicon film and the region below the source is heavily p^+ doped; (2) Next to the source is a heavily doped p-type region that acts as the body contact.

3 Experimental results and discussion

After the formation of the SOI LDMOSFETs, their front-channel and back-channel properties have been characterized by a Keithley 4200SCS semiconductor characteristics system. Subscripts 1 and 2 indicate the front- and back-channels.

The front-channel subthreshold characteristics of devices A and B are shown in Fig. 3. The front-gate (V_{GS1}) and back-gate (V_{GS2}) voltages varied while maintaining a low drain bias ($V_{DS}=0.1V$). The drain current versus front-gate voltage curves are functions of back-gate voltage both in devices A and B. When $V_{GS2}<0V$, the front-channel subthreshold characteristics almost remain the same as when the back-channel is off. When $V_{GS2}>0V$, the front-channel current increases with the back-gate voltage. In Fig. 3, the off-

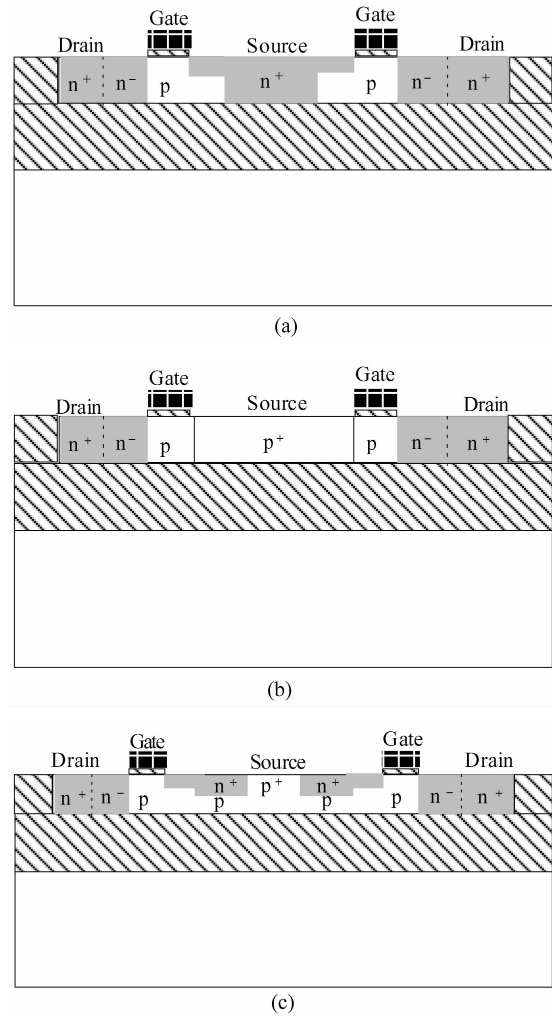

Fig. 2 Cross-sections of devices A and B along lines A-A′ (a), B-B′ (b), and C-C′ (c)

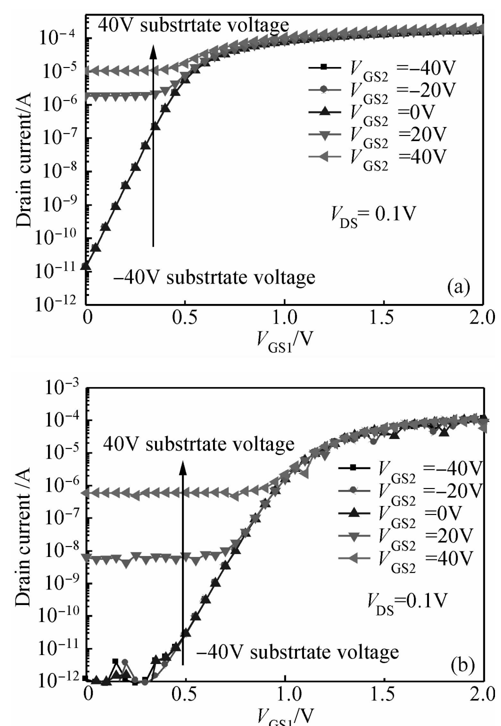

Fig. 3 Front-channel subthreshold characteristics of device A (a) and device B (b)

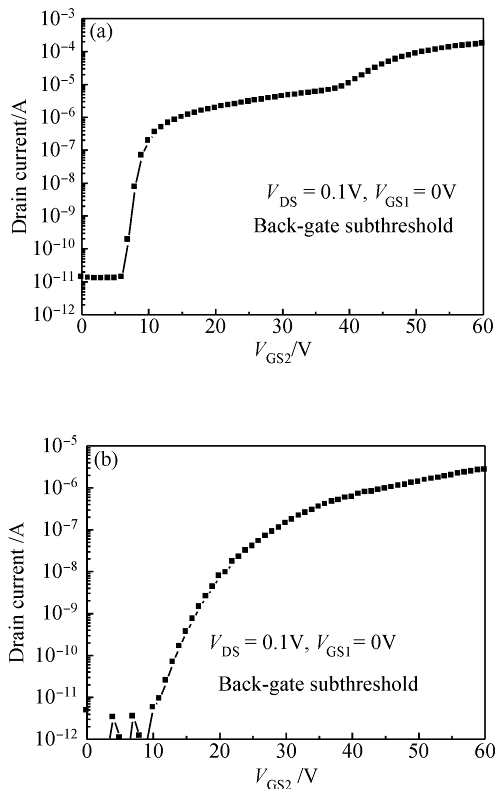

Fig. 4 Back-channel subthreshold characteristics of device A (a) and device B (b)

state current of device A is greater than that of device B. When $V_{GS2} = 20V$, the off-state current of device A is 1.86×10^{-6} A, but that of device B is only 7.35×10^{-9} A. When $V_{GS2} = 40V$, the off-state current of device A is 1.04×10^{-5} A, but that of device B is only 5.89×10^{-7} A.

Figure 4 shows the back-channel subthreshold characteristics of devices A and B. The drain current $1 \times 10^{-9} A/\mu m$ is defined as the back-channel threshold voltage point. The back-channel threshold voltages of devices A and B are 9 and 25V, respectively.

Device B has front-channel and back-channel subthreshold characteristics superior to device A because the LBBC structure keeps the floating body effects under better control and suppresses the back-channel from turning on effectively. Because the source region does not go completely through the top silicon film to the back-channel Si/SiO_2 interface, a parasitic conducting path between the source and drain does not exist, even if the back-channel interface is inverted by the back-gate bias. The body contact barrier height and body resistance play key roles in suppressing floating body effects. The body contact barrier height of devices A and B is considered identical for the same p^+ implantation. For a one-sided BTS body contact structure device, the body resistance is given by

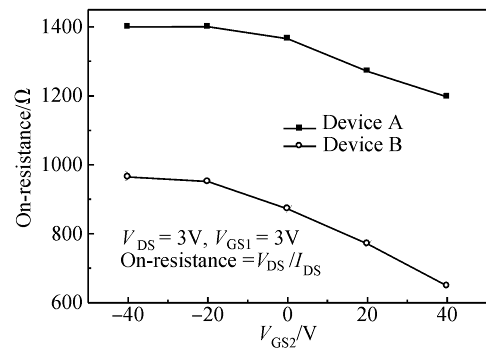

Fig. 5 On-resistance of devices A and B as they vary with back-gate voltage

$$R_{body} = \frac{W_{eff}}{N_A q \mu_p L_{eff}\left(t_{Si} - \sqrt{\frac{4\varepsilon_0 \varepsilon_{Si} \phi_F}{q N_A}}\right)} \quad (1)$$

where N_A is the p-type doping concentration, μ_p is the hole mobility, t_{Si} is the top silicon film thickness, W_{eff} and L_{eff} are the effective channel width and length, and ϕ_F is the Fermi potential. The body resistance greatly increases as device width increases and as gate length shrinks. The body resistance along the width direction is different. This conclusion is applicable to two-sided BTS body contact structure devices in this paper.

For the LBBC body contact structure device, the body resistance is given by

$$R_{body} = \frac{L_S}{N_A q \mu_p W_{eff}(t_{Si} - x_{js} - x_{ds})} \quad (2)$$

$$x_{ds} = \sqrt{\frac{2\varepsilon_0 \varepsilon_{Si}(2\phi_F + V_{sb})}{q N'_A}} \quad (3)$$

where L_s is the source length, x_{js} is the source junction depth, x_{ds} is the source depletion width, and V_{sb} is the source/body voltage. The body resistance along the width direction is the same and proportional to the inverse of the device width.

Figure 5 shows that the back-gate voltage modifies the on-resistance of devices A and B, which is a critical parameter for LDMOSFETs. When $V_{GS2} < -20V$, the on-resistance of devices A and B remains unchanged. In this region, the back-channel is accumulated and the bottom of the drift region is inverted, as shown in Fig. 6. The depletion width in the drift region reaches the maximum. When $V_{GS2} > -20V$, the on-resistance of devices A and B decreases when the back-gate voltage increases. In this region, the back-channel leaks more current and the drift region becomes less resistive.

Figure 7 gives the breakdown characteristics of devices A and B. The back-channel turns on and becomes leakier when $V_{GS2} > 20V$ in device A and $V_{GS2} = 40V$ in device B. It is common in both devices A and B that $BV_{(V_{GS2}=0V)} > BV_{(V_{GS2}=-20V)} >$

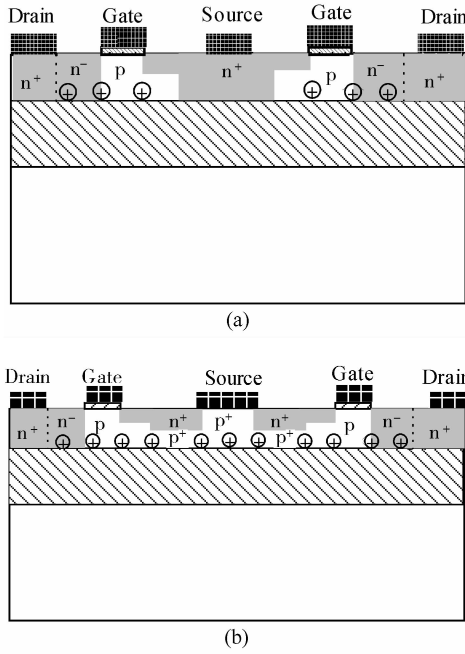

Fig. 6　Back Si/SiO$_2$ interface situation of device A (a) and device B (b)　$V_{GS2} < -20V$

$BV_{(V_{GS2}=-40V)}$. When $V_{GS2} = 20V$ in device B, the back-channel is in the off-state because the threshold voltage of the back-channel is 25V. But the bottom of the drift region is in accumulation, so the resistance of the drift region is lowered. The total on-resistance R_{ON} is the combined series resistance of source resistance R_S, channel resistance R_{CH}, drift region resistance R_{DF}, and drain resistance R_D. Thus, $R_{ON} = R_S + R_{CH} + R_{DF} + R_D$. The drain voltage is divided among these resistors. Because $R_{DF}(V_{GS2} = 20V) < R_{DF}(V_{GS2} = 0V)$, the breakdown voltage at $V_{GS2} = 20V$ is a bit less than that at $V_{GS2} = 0V$ in device B.

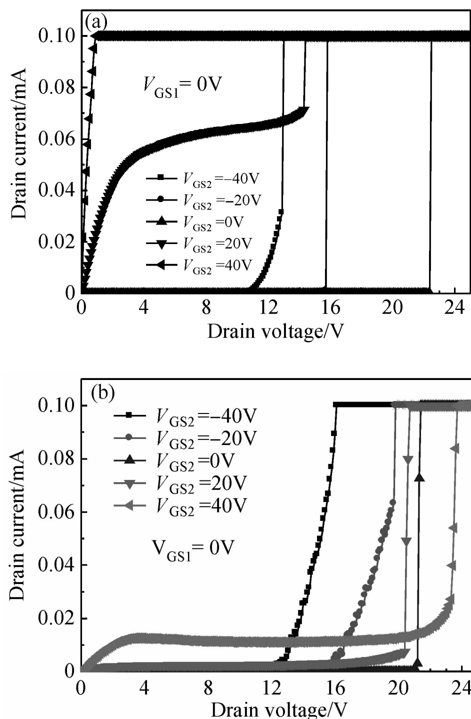

Fig. 7　Breakdown characteristics of device A (a) and device B (b)

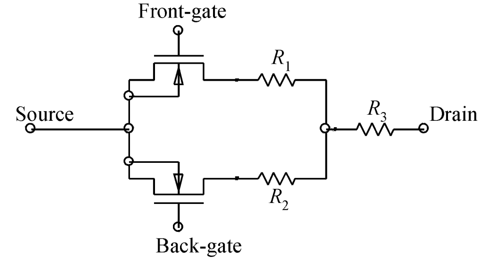

Fig. 8　SOI LDMOSFET circuit model

An equivalent SPICE circuit is used to model the SOI LDMOSFETs, including the front-channel, back-channel, and all associated resistances in Fig. 8. The SPICE model for the LDMOSFETs is achieved by characterization of the front-channel for both bulk and SOI. Only the SOI LDMOSFET requires the characterization of a parasitic back-channel device. R_1 and R_2 are the unavoidable series resistance associated with front-channel and back-channel, while R_3 is their common resistance, dominated by the drift region. R_3 can be modulated by the back-gate voltage. The model is applicable to both the LBBC structure LDMOSFET and the BTS structure LDMOSFET. Because the source of device B does not extend completely through the top silicon film, the G_{D2} of the LBBC structure LDMOSFET is smaller than that of the BTS structure LDMOSFET, which can be derived from Fig. 4.

These transistors are represented by their conductances $G_{D1,2}$:

$$G_{D1,2} = \frac{\mu_{1,2}^0 C_{ox1,2} W/L}{1 + \theta_{1,2}^0 (V_{G1,2} - V_{T1,2})} (V_{G1,2} - V_{T1,2}) \quad (4)$$

where W is the gate width, C_{ox1} and C_{ox2} are the gate oxide and BOX capacitances per unit area, $V_{T1,2}$ are the threshold voltage, $\mu_{1,2}^0$ are the pure mobilities, and $\theta_{1,2}^0$ are the mobility degradation factors at high vertical field.

Without series resistance effects, the intrinsic transconductance of the front- and back-channel is given by

$$g_{m1,2}^0 = \frac{\mu_{1,2}^0 C_{ox1,2} W/L V_D}{[1 + \theta_{1,2}^0 (V_{G1,2} - V_{T1,2})]^2} \quad (5)$$

For single-channel operation mode, the influence of series resistances can be taken into account by replacing the coefficient $\theta_{1,2}^0$ in Eqs. (4) and (5) with $\theta_{1,2}$[12]:

$$\theta_{1,2} = \theta_{1,2}^0 + \mu_{1,2}^0 C_{ox1,2} W/L (R_{1,2} + R_3) \quad (6)$$

For double-channel operation mode, the total drain current is given by[13]

$$I_D = \frac{G_{D1} + G_{D2} + G_{D1}G_{D2}(R_1 + R_2)}{1 + G_{D1}G_{D2}(R_1R_2 + R_1R_3 + R_2R_3) + G_{D1}(R_1 + R_3) + G_{D2}(R_2 + R_3)}V_D \quad (7)$$

So the front gate transconductance is obtained as:

$$g_{m1} = \frac{(1 + R_2G_{D2})^2\dfrac{\partial G_{D1}}{\partial V_{G1}}}{[1 + G_{D1}G_{D2}(R_1R_2 + R_1R_3 + R_2R_3) + G_{D1}(R_1 + R_3) + G_{D2}(R_2 + R_3)]^2}V_D \quad (8)$$

4 Conclusion

In summary, we presented the impact of the back-gate bias of SOI LDMOSFETs with LBBC and BTS structure on the front-channel subthreshold characteristics, on-resistance, and breakdown characteristics. LBBC structure LDMOSFETs have front-channel and back-channel characteristics superior to BTS structure LDMOSFETs for better control of floating body effects and suppression of back-channel leakage. A model for SOI LDMOSFETs has been conceived, including front- and back-channel conduction and bias-dependent series resistance.

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SOI LDMOSFET 的背栅特性*

毕津顺† 宋李梅 海潮和 韩郑生

(中国科学院微电子研究所，北京 100029)

摘要： 在绝缘体上硅衬底上，制备了栅长为 0.5μm 的低势垒体接触结构和源体紧密接触结构的横向双扩散功率晶体管.详细研究了器件的背栅特性.背栅偏置电压对横向双扩散功率晶体管的前栅亚阈值特性、导通电阻和关态击穿特性均有明显影响.相比于源体紧密接触结构，低势垒体接触结构横向双扩散功率晶体管的背栅效应更小，这是因为低势垒体接触结构更好地抑制了浮体效应和背栅沟道开启.还介绍了一种绝缘体上硅横向双扩散功率晶体管的电路模型，其包含前栅沟道，背栅沟道和背栅偏置决定的串联电阻.

关键词： 绝缘体上硅；横向双扩散功率晶体管；背栅效应

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† 通信作者. Email：bravehawk@126.com

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