Impact of 〈100〉 Channel Direction for High Mobility p-MOSFETs on Biaxial Strained Silicon*

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Abstract: Biaxial strain technology is a promising way to improve the mobility of both electrons and holes, while 〈100〉 channel direction appears as to be an effective booster of hole mobility in particular. In this work, the impact of biaxial strain together with 〈100〉 channel orientation on hole mobility is explored. The biaxial strain was incorporated by the growth of a relaxed SiGe buffer layer, serving as the template for depositing a Si layer in a state of biaxial tensile strain. The channel orientation was implemented with a 45° rotated design in the device layout, which changed the channel direction from 〈110〉 to 〈100〉 on Si (001) surface. The maximum hole mobility is enhanced by 30% due to the change of channel direction from 〈110〉 to 〈100〉 on the same strained Si (s-Si) p-MOSFETs, in addition to the mobility enhancement of 130% when comparing s-Si pMOS to bulk Si pMOS both along 〈110〉 channels. Discussion and analysis are presented about the origin of the mobility enhancement by channel orientation along with biaxial strain in this work.

Key words: p-MOSFET; strained Si; channel direction; hole mobility enhancement
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1 Introduction

For decades, CMOS scaling down has been the key to improving device performance until processes under 65nm node were confronted with both fundamental limits and technical challenges. Mobility boosting technologies are therefore becoming indispensable to improve the current drivability independent of geometric scaling. For channel engineering, strained silicon technology is a promising candidate that can notably enhance both electron and hole mobility by band structure altering. The biaxial strain is typically introduced by the incorporation of a relaxed $Si_{1-x}Ge_x$ buffer layer, which is used as an epitaxial template for depositing a Si layer in a state of biaxial tensile strain. The strain induces splitting in the conduction band and valence band relatively, which is the cause of reduced scattering and lower effective mass, thus resulting in the mobility enhancement of both electron and hole[1,2].

However, the rate of strain-induced band splitting in the valence band is considerably lower than in the conduction band[3]; in addition, electron mobility is several times greater than hole mobility in conventional Si CMOS devices[4]. For instance, mobility enhancement of 70% and drive current increase of 35% were observed for strained-Si nMOS on a $Si_{0.8}Ge_{0.2}$ buffer layer[5]. Accordingly, the further boosting of hole mobility is essential and yet a challenge, since high performance CMOS circuits expect equally high current drivability of nMOS and pMOS. Among various techniques of hole mobility boosting, the use of the 〈100〉 channel direction is the most cost effective because it only requires 45° rotated layouts on (001)-oriented wafers[6]. Meanwhile, both theoretical calculations and experimental results report that this technique makes little difference on n-MOSFETs[7,8]. Furthermore, the mechanism of the channel-direction induced mobility enhancement is still not completely understood and remains controversial[7~13].

In order to investigate the impact of 〈100〉 channel combined with biaxial strain on p-MOSFET performance, such 45° rotated devices were designed in the layouts of this work and the samples were fabricated using biaxial strained silicon technology. The electric characteristics of the devices are studied and the mechanism is discussed.

2 Experiment

A graded $Si_{1-x}Ge_x$ buffer, a relaxed $Si_{0.7}Ge_{0.3}$ lay-

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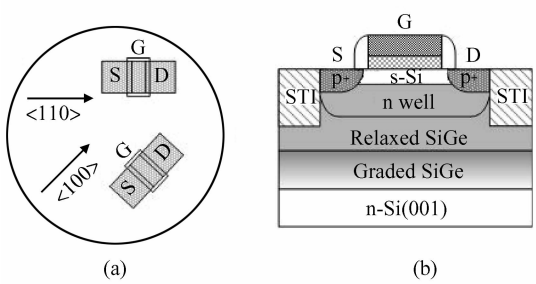

Fig. 1 Schematic diagram of the channel orientation and the device structure (a) Si (001) substrate; (b) Cross section of p-MOSFET device

er, and a strained Si cap layer were epitaxied in turn on a Si (001) nominal substrate in a reduced pressure chemical vapor deposition (RPCVD) reactor. The material growth was first performed at the temperature of 900℃ and the pressure of 100Torr. The Ge content x was gradually increased from 0 to 30% in the graded $Si_{1-x}Ge_x$ buffer due to the grading growth rate, in order to reduce surface roughness and threading dislocation density. The temperature and the pressure remained high during the growth of the relaxed $Si_{0.7}Ge_{0.3}$ layer to ensure the complete relaxation of the SiGe layers. Then the growing temperature dropped to 650℃, followed by the deposition of the strained Si cap layer. The thickness of the strained Si cap layer was optimized to be 10nm to avoid relaxation and to minimize the misfit dislocations.

The strained p-MOSFETs were fabricated along both 〈110〉 and 〈100〉 channels on the same wafer using a modified bulk Si CMOS process, where the active area is defined by shallow trench isolation (STI) technology and the gate oxide thickness is 10nm. Bulk Si p-MOSFETs using the same process were also fabricated as counterparts.

The 45° rotated layout design and the device structure is illustrated in Fig. 1.

3 Results and discussion

Figure 2 is the high-resolution transmission electron microscopy (HRTEM) image of the strained silicon layer on $Si_{0.7}Ge_{0.3}$ virtual substrate. It shows that the strained silicon layer is of an expected thickness and high crystalline quality with no observed defects, providing the high performance of the strained Si (s-Si) devices as presented below.

The study of the device characteristics was based on the data derived by a Keithley 4200 I-V measuring instrument and auxiliary temperature control equipment.

The drive current comparison between 〈100〉 s-Si nMOS and 〈110〉 s-Si nMOS is depicted in Fig. 3. The

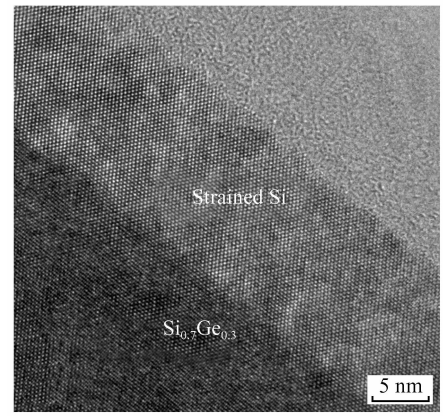

Fig. 2 HRTEM image of the strained silicon layer on $Si_{0.7}Ge_{0.3}$ virtual substrate

minute difference between the curves suggests that the channel orientation from 〈110〉 to 〈100〉 preserves the high performance of s-Si nMOS. This result is also in accordance with Refs. [7,8], in which the electron mobility has little dependence on channel orientation due to the isotropy of the electron effective mass.

The I_D-V_{DS} characteristic of 〈100〉 s-Si pMOS and 〈110〉 s-Si pMOS is depicted in fig. 4. The drive current at the saturation region of 〈100〉 s-Si pMOS has acquired an improvement of 13% compared to 〈110〉 s-Si pMOS when the overdrive voltage (V_{GS} − V_T) is −2V. The derived transconductance (g_m) increases by 14% as a result of the channel orientation change from 〈110〉 to 〈100〉. The drive current of 〈110〉 bulk Si pMOS is also depicted in Fig. 4. Compared to that of 〈110〉 s-Si pMOS, it exhibits a drive current improvement of 75% due to the biaxial strain.

The hole mobility was extracted in the non-saturation region by the equation $\mu_{eff} = (\partial I_D/\partial V_D) \times (L/W)/Q_{INV}$, where Q_{INV} (the charge of the inverse layer) was determined as $Q_{INV} = C_{OX}(V_G - V_T)$. The average vertical effective field in the inverse layer (E_{eff}) was determined as $E_{eff} = Q_{INV}/2\varepsilon_0\varepsilon_{Si} = \varepsilon_{SiO_2}(V_G$

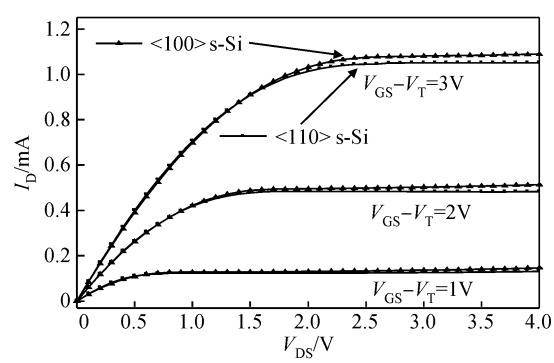

Fig. 3 I_D-V_{DS} characteristic comparison of 〈100〉 s-Si and 〈110〉 s-Si n-MOSFETs

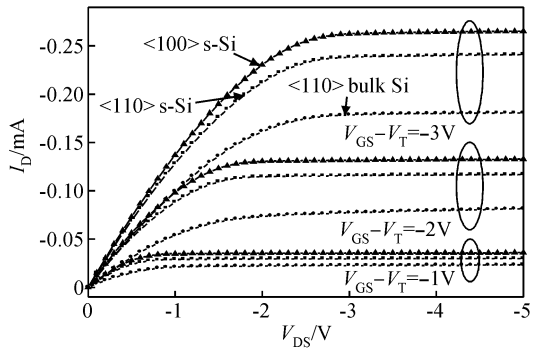

Fig. 4　I_D-V_{DS} characteristic comparison of 〈100〉 s-Si, 〈110〉 s-Si and 〈110〉 bulk Si p-MOSFETs

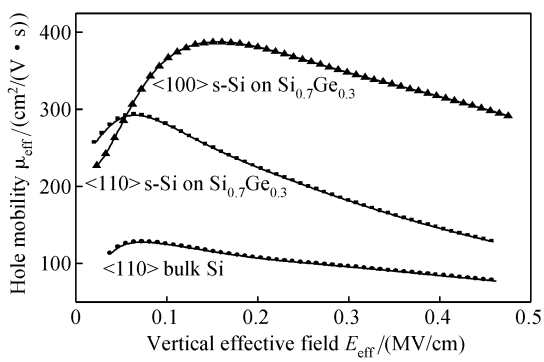

Fig. 5　Hole mobility of 〈100〉 s-Si, 〈110〉 s-Si and 〈110〉 bulk Si p-MOSFETs versus E_{eff}

$-V_T)/2\varepsilon_{Si}t_{ox}$. The hole mobility of 〈100〉 s-Si and 〈110〉 s-Si pMOS versus E_{eff} is plotted in Fig. 5. The maximum hole mobility has obtained an enhancement of 30% due to the change of channel direction from 〈110〉 to 〈100〉 on the s-Si p-MOSFETs. The hole mobility of 〈110〉 bulk Si is also plotted for comparison. The mobility enhancement of 130% is attained by comparing s-Si pMOS to bulk Si pMOS both along 〈110〉 channels. The drop of the mobility caused by the enhanced surface scattering occurs in all three curves as E_{eff} increases. But the mobility along the 〈100〉 channel does not drop as fast as that along 〈110〉 on the same strained Si p-MOSFETs.

The results above exhibit advantages that are attributed to the combination of biaxial strain technology and channel orientation as follows:

(1) The biaxial strain has increased the hole mobility by 130% compared to bulk Si, which is a measurable success in the improvement of pMOS performance.

(2) The increase of Ge content x in the SiGe relaxed layer can raise the mobility enhancement, but will saturate when the Ge content is high enough ($x \sim 0.4$) to trigger deterioration of surface quality[9]. The channel orientation from 〈110〉 to 〈100〉 might be a good option for further enhancement of the hole mobility. Moreover, it does not result in any deterioration for nMOS performance, but even a slight improvement instead.

(3) Device performance at high E_{eff} is critical since the gate oxide thickness shrinks with the scaling trend, while the applied voltage might not change for a period of time. From this aspect, the channel orientation from 〈110〉 to 〈100〉 contributes to the preservation of the high mobility enhancement at high E_{eff}, which is promising for future development.

(4) The modified CMOS fabrication using biaxial strain and channel orientation in this work is completely compatible with the conventional bulk Si CMOS process. Thereby the improvement of the device performance can be achieved with little extra cost.

Some previous results related with channel orientation on (001) surface are listed in Table 1, where the mobility gain and I_D improvement both concern the enhancement due to channel orientation only.

According to Sayama's[7] and Saito's[10] experiments, when the channel orientation change from 〈110〉 to 〈100〉 is applied to bulk silicon, the results differ for different device dimensions. For short channel devices, the mobility gain of 8% and the I_D improvement of 15% are obtained along the 〈100〉 channel, whereas for long channel devices the difference is negligible. This phenomenon is due to the different patterns of carrier transport in short channel and long channel devices[10].

Nevertheless, mobility gain and I_D improvement reaches 30% and 13% relatively on biaxial strained long channel 〈100〉 pMOS in this work, which is direct evidence that biaxial strain enhances the impact of 〈100〉 channel orientation on long channel devices. To study the origin of this enhancement, mechanisms of mobility and of the band altering induced by biaxial strain are reviewed.

Table 1　mobility gain and performance improvement for various strain techniques with channel orientation from 〈110〉 to 〈100〉

Author/year	Strain type	Strain sigh	Channel	Mobility gain/%	I_D improvement/%
Sayama/1999[7]	Bulk Si	Zero	Short	8	15
Saito/2006[10]	Bulk Si	Zero	Short	—	19
			Long	negligible	5
Shima/2002[11]	Biaxial-strained-SiGe	Compressive	Short	25	10
Komoda/2004[12]	Uniaxial-strained-Si	Both	Short	—	20
This work	Biaxial-strained-Si	Tensile	Long	30	13

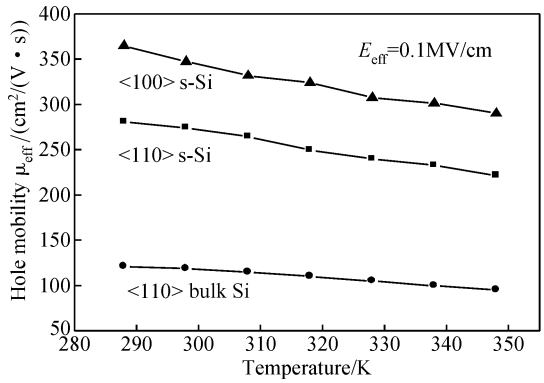

Fig. 6 Hole mobility dependence on temperature at E_{eff} = 0.1MV/cm

Effective mobility is determined as $e\tau/m_c^*$, where τ is the relaxation time due to scatterings and m_c^* is the conductivity effective mass. The major scatterings are Coulomb scattering and lattice scattering. Coulomb scattering is not changed, since the channel doping is unchanged and independent of strain. Lattice scattering is correlated to temperature. Figure 6 shows the hole mobility dependence on temperature of 〈100〉 s-Si, 〈110〉 s-Si, and 〈110〉 bulk Si pMOS. The curves of 〈100〉 s-Si and 〈110〉 s-Si have almost the same slope, which means that lattice scattering is not relevant to the mobility gain. Other scatterings like surface, inter-band, and intra-band scatterings should also be considered, but their anisotropy, especially under the impact of biaxial strain, is too complicated to be determined, even with the assistance of state-of-the-art calculations. Therefore, it is difficult to explain the mobility gain solely from τ.

Then to find out the origin, m_c^* should be taken into account. Because of the difficulty in evaluating the exact m_c^* under all circumstances, qualitative analysis is stated as follows:

m_c^* is determined by the conductivity effective mass of the heavy hole band m_c^* (HH) and that of the light hole band m_c^* (LH), as well as the hole occupation of the HH (heavy hole) band and LH (light hole) band relatively.

The biaxial strain intensifies the anisotropy of m_c^* (HH)[8], and thus reduces the m_c^* (HH) along the 〈100〉 channel on s-Si compared to that on bulk Si. This is a plausible origin for biaxial strain enhancing the impact of 〈100〉 channel orientation on long channel devices. Along with the mechanism of hole occupation of HH and LH bands, the shift of the summit toward high E_{eff}, as well as the gentle slope at high E_{eff}, of the 〈100〉 s-Si mobility curve in Fig. 5 can also be explained relatively.

Figure 7 illustrates the impact of the biaxial strain and the change of E_{eff} on hole occupation of the

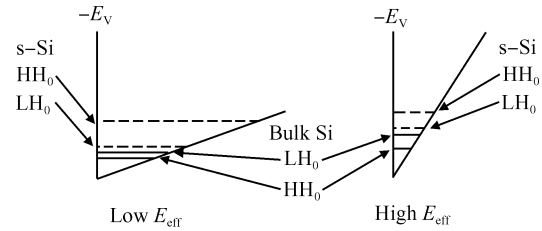

Fig. 7 Schematic valence band of bulk Si (solid lines) and s-Si (dashed lines) at low/high E_{eff}[9]

HH band and LH band. In bulk Si, the HH band is lower and the splitting between the LH and HH bands grows with the increase of E_{eff}, and hence the HH band becomes preferentially occupied at high E_{eff}. In contrast, the LH band is the lower state in s-Si, and it is separated from the HH band by a larger gap with virtue of biaxial strain at low E_{eff}. However, the energetic separation of LH and HH bands is diminished by the increase of E_{eff} due to quantum confinement. Therefore, it can be concluded that biaxial strain favors the occupation of the LH band, while the increase of E_{eff} favors occupation of the HH band[9].

In bulk silicon, LH and HH bands degenerate at the Γ-point. The biaxial tensile strain splits the degeneracy and favors the hole occupation of the LH band, which is the lower state than the HH band, thus leading to the reduction of m_c^*[9]. Meanwhile, the rise of E_{eff} favors the occupation of the HH band, thus leading to the increase of m_c^*. At low E_{eff} where Coulomb scattering is dominant, the diminished Coulomb scattering due to the increasing E_{eff} counteracts the increase of m_c^* and gives rise to the hole mobility. Meanwhile, at high E_{eff} where surface scattering is dominant, the enhanced surface scattering due to the increasing E_{eff}, along with the increase of m_c^*, causes the drop of the hole mobility. When the channel is changed from 〈110〉 to 〈100〉 on biaxial strained silicon, the m_c^* is reduced because of the anisotropy of the HH effective mass, which slows down the increasing rate of m_c^* resulting from the favored occupation of the HH band as E_{eff} increases. Thus, the summit of the mobility shifts toward high E_{eff} and the mobility drop is more gentle for 〈100〉 s-Si pMOS compared to 〈110〉 s-Si pMOS.

In summary, the result of this work is consistent with the presented origin, and is quite satisfactory according to the reports listed in Table 1.

4 Conclusion

Biaxial strained p-MOSFETs along the 〈100〉 channel with high performance were demonstrated in this work. The maximum hole mobility enhancement

has achieved 30% due to the change of channel direction from 〈110〉 to 〈100〉 on the same strained Si p-MOSFETs, in addition to the mobility enhancement of 130% brought in by the biaxial strain only. The drive current has obtained an improvement of 13% at the overdrive voltage of −2V merely due to channel orientation change. The origin of the mobility enhancement due to the combination of biaxial tensile strain and 〈100〉 channel is presented.

The results indicate that changing the channel orientation from 〈110〉 to 〈100〉 on a (001) surface can significantly improve pMOS performance, with the contribution of biaxial tensile strain. The combination of these two techniques is promising for future CMOS circuit development.

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〈100〉沟道方向对高迁移率双轴应变硅 p-MOSFET 的作用*

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摘要： 双轴应变技术被证实是一种能同时提高电子和空穴迁移率的颇有前景的方法；〈100〉沟道方向能有效地提升空穴迁移率. 研究了在双轴应变和〈100〉沟道方向的共同作用下的空穴迁移率. 双轴应变通过外延生长弛豫 SiGe 缓冲层来引入，其中，弛豫 SiGe 缓冲层作为外延底板，对淀积在其上的硅帽层形成拉伸应力. 沟道方向的改变通过在版图上 45°旋转器件来实现，这种旋转使得沟道方向在(001)表面硅片上从〈110〉晶向变成了〈100〉晶向. 对比同是〈110〉沟道的应变硅 pMOS 和体硅 pMOS，迁移率增益达到了 130%；此外，在相同的应变硅 pMOS 中，沟道方向从〈110〉到〈100〉的改变使空穴迁移率最大值提升了 30%. 讨论和分析了这种双轴应变和沟道方向改变的共同作用下迁移率增强的机理.

关键词： p-MOSFET；应变硅；沟道方向；空穴迁移率增强

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