A New High Voltage SOI Device with a Nonuniform Thickness Drift Region and Its Optimization*

Luo Xiaorong†, Zhang Wei, Zhang Bo, Li Zhaoji, Yan Bin, and Yang Shouguo

(*State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu 610054, China*)

Abstract: A new SOI high-voltage device structure with nonuniform thickness drift region (n-uni SOI) and its optimization design method are proposed. Owing to the nonuniform thickness drift region, the electric field in the SOI layer is modulated and the electric field in the buried layer is enhanced, resulting in an enhancement of breakdown voltage. An analytical model taking the modulation effect into account is presented to optimize the device structure. Based on the analytical model, the dependencies of the electric field distribution and breakdown voltage on the device parameters are investigated. Numerical simulations support the analytical model. The breakdown voltage of the n-uni SOI LDMOS with $n = 3$ is twice as high as that of a conventional SOI while its on-resistance maintains low.

Key words: SOI; nonuniform thickness drift region; electric field; modulation; high voltage
EEACC: 2560B; 2560P
CLC number: TN386 **Document code**: A **Article ID**: 0253-4177(2008)10-1902-05

1 Introduction

Silicon on insulator (SOI) technology offers tremendous advantages over junction isolation, such as low leakage current, near ideal isolation, and high switching speed, but suffers from low breakdown voltage (BV) and the self-heating effect (SHE). To address these issues, several structures have been proposed[1~10], in which a linear drift doping profile technology on the ultra-thin SOI has been applied to realize a high BV (>700V)[2], while the local self-heating near the source is presented[11,12]. Therefore, the step doping profile in the SOI layer (SD SOI) has been proposed to obtain a trade-off between BV and SHE[12,13]. An analytical model can shorten the design cycle by the first-order design scheme and provide physical insight into the breakdown mechanism. Chung *et al*. have given a general expression of the surface electric field accounting for the effects of the gate and drain field plates[14]. The breakdown voltage models for SD SOI devices and surface implanted SOI LDMOSs have been given[13,15]. But these device structures and analytical models are presented only for SOI devices with a uniform thickness in the drift region.

In this work, a new SOI high-voltage device structure with a nonuniform thickness in the drift region and its analytical model for the electric field distribution are proposed. The electric field of the drift region is modulated by the nonuniform thickness SOI layer, improving the electric field distribution in the buried layer and thus enhancing breakdown voltage. We analyze and optimize the electric field distribution and breakdown voltage for the n-uni SOI. The results show that the proposed device structure enhances BV and reduces on-resistance (R_{on}).

2 Structure and model

The cross section of an n-uni SOI LDMOS is shown in Fig. 1, where the SOI layer is divided into n regions with different SOI thicknesses t_{Si} ($i = 1, 2, \cdots, n$, $t_{Sn} = t_S$). The length of ith region is L_i. N-uni SOI

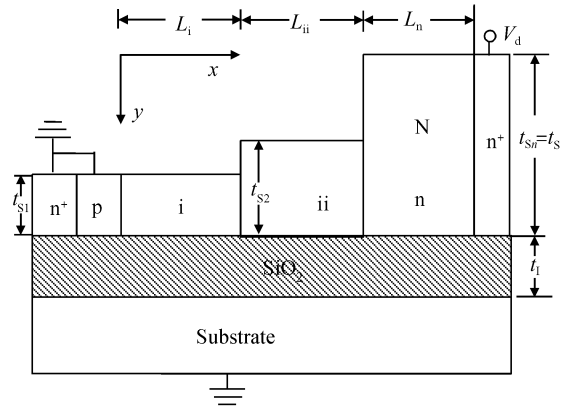

Fig. 1 Schematic cross section of an n-uni SOI LDMOS

* Project supported by the National Natural Science Foundation of China (Nos. 60436030, 6080625) and the Youth Teacher Foundation of University of Electronic Science and Technology of China (No. jx0721)
† Corresponding author. Email: xrluo@uestc.edu.cn
Received 4 April 2008, revised manuscript received 5 June 2008

with $n = 1$ is the conventional SOI. x measures the horizontal position relative to the edge of the p region while y measures the vertical positions relative to nth region surface, respectively. N_d and L_d are the doping concentration and length of the drift region with the permittivity of ε_S, satisfying $L_d = \sum_{i=1}^{n} L_i$. t_I is the thickness of the buried layer with permittivity of ε_I.

The new surface field peaks are generated at steps, which modulates the electric field of the SOI layer and increases the electric field of the buried layer, resulting in an enhancement of breakdown voltage.

When a high positive voltage V_d is applied to the drain while the source, gate, and substrate are grounded, the drift region is fully depleted. The potential function $\varphi_i(x, y)$ of ith ($i = 1, 2, \cdots, n$) region follows the 2D Poisson's equation:

$$\frac{\partial^2 \varphi_i(x,y)}{\partial x^2} + \frac{\partial^2 \varphi_i(x,y)}{\partial y^2} = -\frac{qN_d}{\varepsilon_S}, \quad t_S - t_{Si} \leqslant y \leqslant t_S, i = 1,2,\cdots,n \tag{1}$$

$\varphi_i(x, y)$ can be approximated by a simple parabolic function. The boundary conditions for Eq. (1) are given by

$$\left.\frac{\partial \varphi_i(x,y)}{\partial y}\right|_{y=t_S-t_{Si}} = 0, \left.\frac{\partial \varphi_i(x,y)}{\partial y}\right|_{y=t_S} = -\frac{\varepsilon_I \varphi_i(x,t_S)}{\varepsilon_S t_I}, \quad t_S - t_{Si} \leqslant y \leqslant t_S, i = 1,2,\cdots,n \tag{2}$$

For the optimal device structure, the following expression is satisfied to obtain a maximal BV:

$$E\left(\frac{i}{n}L_d, t_S - t_{Si}\right) = E_C, \quad i = 1,2,\cdots,n \tag{3}$$

where E_C is the critical electric field of Si. Solving Eq. (1) with the boundary conditions (2) and (3), the surface potential and surface electric field distributions are given by

$$\varphi_i(x, t_S - t_{Si}) = \frac{E_c t_i}{\mathrm{sh}(L_d/nt_i)}\left[\mathrm{ch}\left(\frac{x - \frac{i-1}{n}L_d}{t_i}\right) - \mathrm{ch}\left(\frac{\frac{i}{n}L_d - x}{t_i}\right)\right] + \frac{qN_d t_i^2}{\varepsilon_S}, \quad i = 1,2,\cdots,n \tag{4}$$

$$E_i(x, t_S - t_{Si}) = \frac{E_c}{\mathrm{sh}(L_d/nt_i)}\left[\mathrm{sh}\left(\frac{x - \frac{i-1}{n}L_d}{t_i}\right) + \mathrm{sh}\left(\frac{\frac{i}{n}L_d - x}{t_i}\right)\right], \quad i = 1,2,\cdots,n \tag{5}$$

where $t_i = t_{Si}\sqrt{0.5 + (t_I/\varepsilon_I)(\varepsilon_S/t_{Si})}$. Equations (4) and (5) can also be applied to an SD SOI LDMOS by substituting $t = t_S\sqrt{0.5 + (t_I/\varepsilon_I)(\varepsilon_S/t_S)}$ and N_{di} for t_i and N_d, respectively, where t_S and N_{di} are the thickness of the SOI layer and the concentration of ith region for an SD SOI LDMOS, respectively. For the SD SOI LDMOS, substituting $\varphi_1(0, 0) = 0$ and $\varphi_n(L_d, 0) = \mathrm{BV} = \sum_{i=1}^{n}\int_{\frac{i-1}{n}L_d}^{\frac{i}{n}L_d} E_i(x, 0)\mathrm{d}x = 2ntE_C\,\mathrm{th}\frac{L_d}{2nt}$ into Eq. (4) yields $N_{d1} \leqslant \frac{\varepsilon_S E_{S,C}}{qt}\,\mathrm{th}\,\frac{L_d}{2nt}$ and $N_{dn} \leqslant \frac{(2n-1)\varepsilon_S E_{S,C}}{qt}\,\mathrm{th}\,\frac{L_d}{2nt}$, based on which, the RESURF condition of $N_{di} \leqslant \frac{(2i-1)\varepsilon_S E_{S,C}}{qt} \propto (2i-1)$ and $N_{di}t_S = (2i-1)N_{d1}t_S$ can be inferred. This result agrees with that of Refs. [13, 16]. According to the above analysis, a high-voltage SOI device can be obtained by varying the thickness of the SOI layer and maintaining a fixed N_d, which is expressed by

$$N_d t_{Si} = (2i-1)N_d t_{S1} \tag{6}$$

This is the design conception of an n-uni SOI high-voltage device.

3　Results and discussion

Figure 2 gives the surface field and surface potential distributions for the conventional SOI and n-uni SOI LDMOS with $n = 3$, in which the structural parameters are $t_I = 3\mu$m, $t_S = 0.5\mu$m and $L_d = 36\mu$m for two devices, $t_{Si} = 0.1 \times (2i-1)\mu$m, $L_i = L_d/3$ for the n-uni SOI LDMOS. Compared with the conventional SOI, the new surface field peaks P1 and P2 are generated at steps, lowering the electric field peaks at the ends of the drift region for n-uni SOI. So a high average electric field in the drift region is obtained for the n-uni SOI due to the modulation effect, resulting in an increase of BV from 198V of the conventional SOI to 405V. The analytical results of the surface field in the middle of each region for the n-uni SOI LDMOS are lower than the numerical simulations in Fig. 2 (a). The discrepancies result from the assumption of $\left.\frac{\partial \varphi_i(x,y)}{\partial y}\right|_{y=t_S-t_{Si}} = 0$ in Eq. (2), which ignores the 2D effect of the surface field though it is important for the n-uni SOI LDMOS with small t_{Si} and L_i. The analytical results for the conventional SOI agree well with the simulations due to the large t_{Si} (0.5μm) and L_i (36μm) in Fig. 2 (a). The surface potential distributions are given in Fig. 2 (b). The voltage drop is almost uniform in the x-direction for the n-uni SOI. However, the voltage is mainly sustained by pn and nn^+ junctions and the drift region hardly supports voltage for the conventional SOI, thus BV is low.

The surface field distributions for the n-uni SOI and SD SOI (represented by line) LDMOSFETs are also compared in Fig. 2 (a). The parameters are used in simulation as follows: for n-uni SOI, $t_{S1} = 0.1\mu$m, $t_{S2} = 0.3\mu$m, $t_{S3} = 0.5\mu$m and $N_d = 4.5 \times 10^{16}\,\mathrm{cm}^{-3}$; for

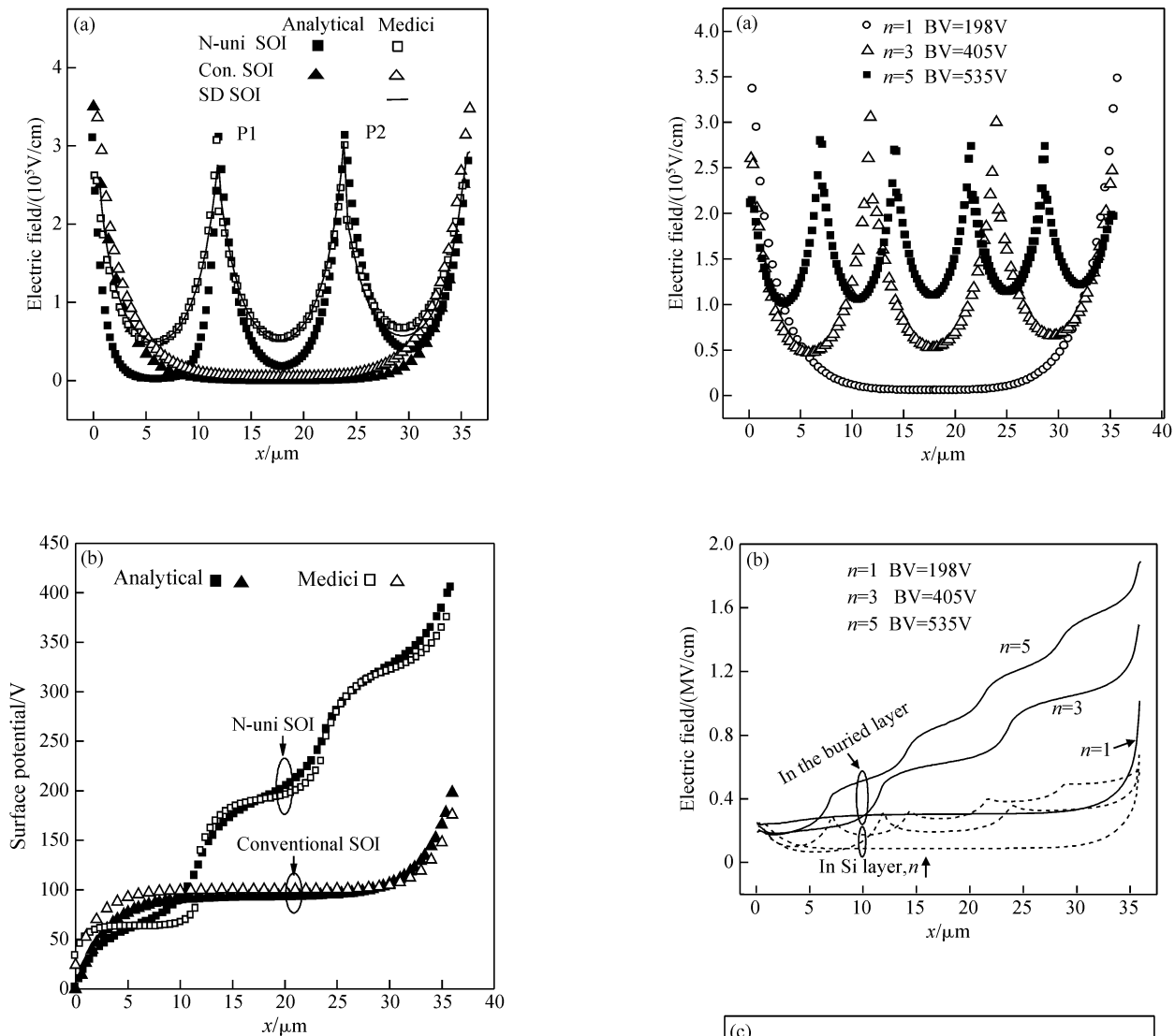

Fig. 2 Surface electric field and potential distributions (a) Surface electric field distributions; (b) Surface potential distributions ($t_1 = 3\mu m$, $t_S = 0.5\mu m$, $L_d = 36\mu m$ for all, $t_{S1} = 0.1\mu m$, $t_{S2} = 0.3\mu m$, $t_{S2} = 0.5\mu m$, $L_i = L_d/3$ for n-uni SOI)

SD SOI, $N_{d1} = 1.5\times10^{16}$ cm^{-3}, $N_{d2} = 4.5\times10^{16}$ cm^{-3}, $N_{d3} = 7.5\times10^{16}$cm^{-3} and $t_S = 0.3\mu m$. The charge densities in ith region for the n-uni SOI and SD SOI LDMOSFETs are equal and satisfy the ratio $2i-1$. Their electric field distributions and BV (n-uni SOI, BV = 405V, SD SOI BV = 399V) are almost identical.

BV increases as n increases because of the enhanced modulation effect of multiple steps on the electric field. Figure 3 gives the electric field distributions in the x- and y-directions at $n = 1, 3, 5$. Both the number of the surface field peaks and the average electric field increase with n. The new electric field peaks on the interface between the SOI layer and buried layer appear on account of the coupling effects of the surface field, leading to an enhancement of the interface electric fields as illustrated in Fig. 3 (b). Therefore, the electric field of the buried layer E_I is

Fig. 3 Influence of n on the electric field distributions in the x- and y-directions (a) Surface electric field distributions versus n; (b) Interface electric field distributions versus n; (c) Electric field distributions in y-direction versus n ($t_1 = 3\mu m$, $L_d = 36\mu m$, $L_i = L_d/n$ for n-uni SOI, $N_d = 1.3\times10^{16}$, 4.5×10^{16} and 7.5×10^{16}cm^{-3} for $n = 1, 3$ and 5, respectively)

enhanced from about 65V/μm of the conventional SOI ($n = 1$) to 170V/μm for the n-uni SOI LDMOS with $n = 5$ in Fig. 3(c), and BV increases from 198V

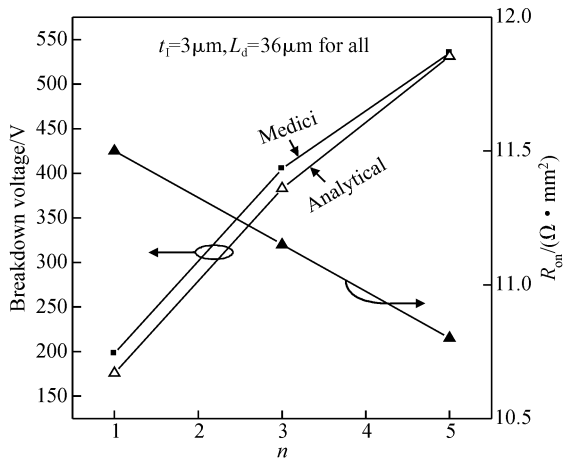

Fig. 4　BV and R_{on} as a function of n (the same structure parameters as given in Fig. 3)

to 535V. BV for the n-uni SOI LDMOS with $n = 3$ is twice as high as that of the conventional SOI.

Figure 4 shows the dependences of BV and R_{on} on n. We conclude that BV increases and R_{on} decreases as n increases. $n = 3$ can be used to realize a high BV and low R_{on} taking the fabrication difficulty into account. The step SOI layer can be realized either by selective dry etching twice or by selective oxidation followed by oxide removal twice. The analytical results of BV are lower than the simulation in Fig. 4 as a result of the low electric field values used in the analytical model (in Fig. 2(a)).

Figure 5 gives the impact of N_d on BV with the different step heights. The optimal N_d decreases as t_{S3} increases for given t_{S1} and t_{S2}. The step heights of $t_{S2} - t_{S1}$ and $t_{S3} - t_{S2}$ are not permitted to be too high or too low in order to get a high BV. $t_{Si} = (2i - 1)\ t_{S1}$ is an optimal SOI thickness profile. Figure 5 gives the optimal analytical results of BV. The design results agree with the numerical simulations.

Figure 6 compares the surface temperature distributions for the n-uni SOI ($n = 3$) and the conventional SOI LDMOSFETs with their own optimal N_d. V_d = 12V, the gate voltage V_g = 10V, and the substrate temperature 300K are used in simulation. For an n-uni SOI LDMOS, the enhancement of E_I makes t_I decrease for a fixed BV or BV increase for a constant t_I, resulting in a low self-heating effect or a high BV as indicated in Fig. 6. Thus, we conclude that the n-uni SOI structure can not only enhance BV, but reduce R_{on} and SHE. So, it has the potential for application in high voltage and power fields.

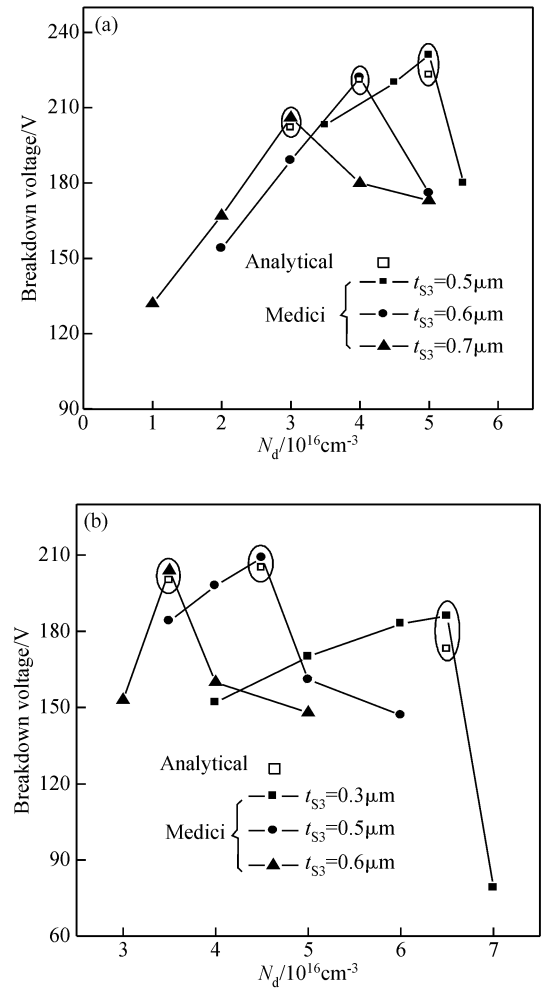

Fig. 5　BV as a function of N_d with the different step heights for n-uni SOI　(a) $t_{S2} = 0.3\mu$m; (b) $t_{S2} = 0.2\mu$m　$t_I = 1.5\mu$m, $t_{S1} = 0.1\mu$m, $L_d = 15\mu$m, $L_i = L_d/3$

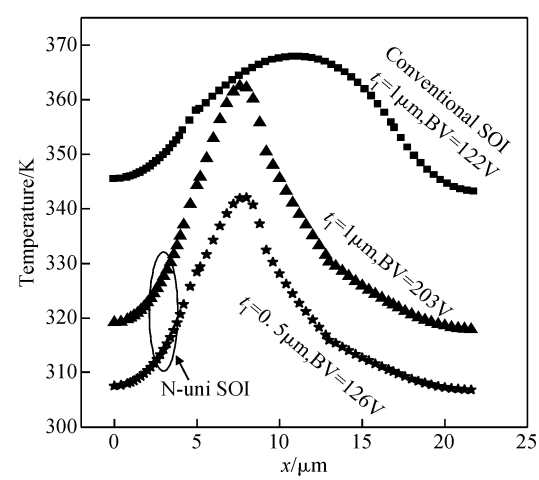

Fig. 6　Surface temperature distributions ($L_d = 12\mu$m, $t_S = 0.5\mu$m, $V_g = 10$V, $V_d = 12$V for all, $t_{S1} = 0.1\mu$m, $t_{S2} = 0.3\mu$m, $t_{S2} = 0.5\mu$m for n-uni SOI)

4　Conclusion

A new SOI high-voltage device with nonuniform thickness in the drift region is proposed. The electric field in the SOI layer is modulated and the electric field in the buried layer is enhanced, realizing a high breakdown voltage. An analytical model is presented to guide the design for the proposed structure. It

shows the breakdown voltage of n-uni SOI LDMOS is twice as high as that of conventional SOI, and R_{on} and SHE remain low.

References

[1] Luo Xiaorong, Zhang Bo, Li Zhaoji. A novel 700V SOI LDMOS with double-side trench. IEEE Electron Device Lett, 2007, 28(5): 422

[2] Merchant S, Arnold E, Baumgart H, et al. Realization of high breakdown voltage (>700V) in thin SOI device. Proc Int Symp Power Semicond Devices ICs, 1991: 31

[3] Luo Xiaorong, Zhang Bo, Li Zhaoji. A new structure and its analytical model for the electric field and breakdown voltage of SOI high voltage device with variable-k dielectric buried layer. Solid-State Electron, 2007, 51: 493

[4] Duan Baoxing, Zhang Bo, Li Zhaoji. New thin-film power MOSFETS with a buried oxide double step structure. IEEE Electron Device Lett, 2006, 27(5): 377

[5] Nakagawa A, Yasuhara N, Baba Y. Breakdown voltage enhancement for devices on thin silicon layer/silicon dioxide film. IEEE Trans Electron Devices, 1991, 38(7): 1650

[6] Luo Xiaorong, Zhang Bo, Li Zhaoji. New high-voltage (>1200V) MOSFET with the charge trenches on partial SOI. IEEE Trans Electron Devices, 2008, 55(7): 1756

[7] Funaki H, Yamaguchi Y, Hirayama K, et al. New 1200V MOSFETstructure on SOI with SIPOS shielding layer. Proc IEEE ISPSD, 1998: 25

[8] Kim I J, MatSumoto S, Sakai T, et al. Breakdown voltage improvement for thin-film SOI power MOSFET's by a buried oxide step structure. IEEE Electron Device Lett, 1994, 15(5): 148

[9] Udrea F, Trajkovic T, Amaratunga G A J. Membrane high voltage devices-a milestone concept in power ICs. IEEE IEDM, 2004: 451

[10] Luo Xiaorong, Zhang Bo, Li Zhaoji, et al. A new SOI high voltage device with step thickness sustained voltage layer. Electron Lett, 2008, 44(1): 55

[11] Chang F L, Lin M J, Lee G Y, et al. Modeling and design of the high performance step SOI-LIGBT power devices by partition mid-point method. Solid-State Electron, 2003, 47: 1693

[12] Sunkavalli R, Tamba A, Baliga B J. Step drift doping profile for high voltage DI lateral power devices. Proc Int SOI Conf, 1995: 139

[13] Guo Y F, Li Z J, Zhang B. A new analytical model for optimizing SOI LDMOS with step doped drift region. Microelectronics Journal, 2006, 37: 861

[14] Chung S K, Han S Y. Analytical model for the surface field distribution of SOI RESURF devices. IEEE Trans Electron Devices, 1998, 45(5): 1374

[15] Chung S K. An analytical model for breakdown voltage of surface implanted SOI RESURF LDMOS. IEEE Trans Electron Devices, 2000, 47(5): 1006

[16] Guo Y F, Fang J, Zhang B, et al. A 2D analytical model of SOI double RESURF effect. Chinese Journal of Semiconductors, 2005, 26(4): 33

非均匀厚度漂移区 SOI 高压器件及其优化设计*

罗小蓉† 张 伟 张 波 李肇基 阎 斌 杨寿国

(电子科技大学电子薄膜与集成器件国家重点实验室, 成都 610054)

摘要: 提出非均匀厚度漂移区 SOI 高压器件新结构及其优化设计方法. 非均匀厚度漂移区调制 SOI 层的电场并增强埋层电场, 从而提高器件击穿电压. 考虑到这种调制效应, 提出解析模型用以优化设计该新器件的结构参数. 借助解析模型, 研究了电场分布和器件击穿电压与结构参数的关系. 数值仿真证实了解析模型的正确性. 具有 3 阶梯的非均匀厚度漂移区 SOI 器件耐压为常规结构 SOI 器件的 2 倍, 且保持较低的导通电阻.

关键词: SOI; 非均匀厚度漂移区; 电场; 调制; 高压

EEACC: 2560B; 2560P

中图分类号: TN386 **文献标识码**: A **文章编号**: 0253-4177(2008)10-1902-05

* 国家自然科学基金(批准号: 60436030, 60806025)和电子科技大学青年教师基金(批准号: jx0721)资助项目

† 通信作者. Email: xrluo@uestc.edu.cn

2008-04-04 收到, 2008-06-05 定稿