Design Analysis of a Novel Low Triggering Voltage Dual Direction SCR ESD Device in 0.18μm Mixed Mode RFCMOS Technology*

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Abstract: A novel SCR on-chip ESD device is proposed to protect IC chips against ESD stressing in two opposite directions. The triggering voltages of four types of dual direction SCRs (DDSCR) are compared and analyzed. pMOS or nMOS are embedded into the structures to adjust their triggering voltages. Both MOSFETs embedded DDSCRs have tunable triggering voltage, low DC leakage (~pA), and fast turn on speed snapback *I-V* characteristics without latch-up problem. It achieves high ESD performance of ~94V/μm. The new ESD protection devices are area efficient and can reduce the parasitic effects significantly.

Key words: electrostatic discharge; dual direction SCR; snapback
PACC: 4110D; 4400; 7340L **EEACC**: 5110; 2560; 1280
CLC number: TN402 **Document code**: A **Article ID**: 0253-4177(2008)11-2164-05

1 Introduction

Electrostatic discharge (ESD) causes a significant percentage of the failures in electronics industry. The shrinking size of semiconductor circuits, thinner gate oxides, complex chips with multiple power supplies and mixed-signal blocks, larger chip capacitance and faster circuit operation, all contribute to increased ESD sensitivity of advanced semiconductor devices[1]. On-chip ESD protection design becomes a big challenge in mixed mode RFCMOS ICs. SCR ESD device is reported as the most efficient on-chip ESD protection device, but it does not possess the snapback function to conduct current in both directions. In order to against ESD pulses in positive and negative stressing modes, an alternative is to use two devices to form active discharging paths in two opposite directions[2]. But its double size would consume large silicon area and induce substantial parasitic effects. Such a problem is more severe in mixed mode RF and high pin-count designs. Wang[3,4] devised a dual direction SCR (DDSCR) ESD protection structure implemented in BiCMOS technology with a deep n^+ isolation layer. And he used a trigger assist circuit to reduce the triggering voltage of the DDSCR which comprises two pairs of Zener diodes with back-to-back connection. Its best ESD performance is ~80V/μm. Ker[5] mentioned that to realize the DDSCR device structure proposed by Wang in the CMOS process, an extra deep n-well mask must be added into the process flow. The deep n-well mask prevents the initial leakage path in the npnpn structure. Of course, the extra mask and associated process steps increase the costs. What's more, Zener diodes trigger assist circuit is not only an area consuming method but also incompatible in certain CMOS processes.

In this paper, a successful design of a novel low triggering voltage compact dual direction SCR ESD devices which are based on both pnpnp and npnpn structures are reported, originally targeting mixed mode RF chips. All of the DDSCR structures are realized in 0.18μm mixed mode RFCMOS process. The basic operation mechanism of novel pnpnp based DDSCR without additional masks is described.

2 pnpnp based DDSCR devices

2.1 pnpnp DDSCR device design

The symmetrical pnpnp DDSCR structure in CMOS process illustrated in Fig. 1 comprises one lateral npn (T2) structure and two vertical pnp structures (T1 and T3). The ESD device is off in normal condition, therefore it does not interfere with IC chip operation. Consider the case when a positive ESD

* Project supported by the Natural Science Foundation of Jiangsu Province (No. BK2007026) and the Natural Science Foundation of Zhejiang Province (No. Y107055)

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Received 5 April 2008, revised manuscript received 24 July 2008

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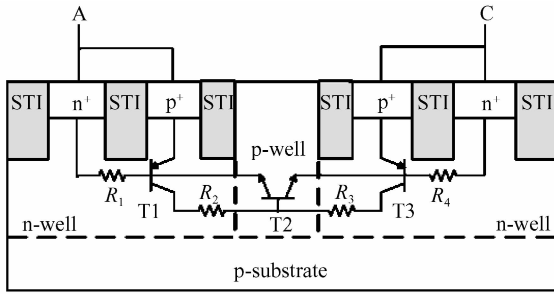

Fig. 1　Device structure of pnpnp DDSCR

pulse is applied to the terminal A of the device with respect to the terminal C, the BC junction (p-well/n-well) of T2 is reverse biased. As the reverse voltage monotonically increases, the BC junction will reach its avalanche breakdown voltage eventually. A large amount of electron-hole pairs are therefore generated. Those excess electrons and holes will be collected by the n^+ and p^+ connected to the terminal A and C, respectively. A potential drop builds up along the electron flowing path due to parasitic n-well resistance R1 simultaneously. So the BE (p^+/n-well) junction of T1 is forward biased and eventually turns on T1, and so does T2. The T2 and T3 BJT pair forms a regenerative thyristor. Continuous stressing will drive the thyristor into deep snapback region with low on-resistance (R_{on}). And vise versa, when a negative ESD pulse is applied to the terminal A of the device, it is the same effect as a positive ESD pulse is applied to the terminal C of the device with respect to the terminal A. T2 and T3 BJT pair will perform the same thyristor function due to its symmetrical device design.

2.2　n^+ modified pnpnp DDSCR device design

The triggering voltage of the DDSCR device mentioned in 2.1 is dominated by the avalanche breakdown of n-well/p-well junction, which could be more than 14V in this 0.18μm CMOS process. In order to reduce the avalanche breakdown voltage between the n-well and p-well to provide more effective ESD protection for internal circuit, a heavily doped n^+ diffusion is added across the two wells. The triggering voltage is determined by the avalanche breakdown voltage (V_{av}) between the p/n junction.

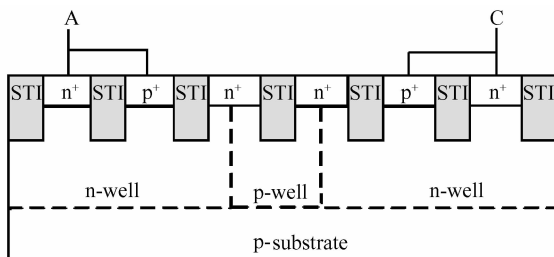

Fig. 2　Cross section of n^+ modified pnpnp DDSCR

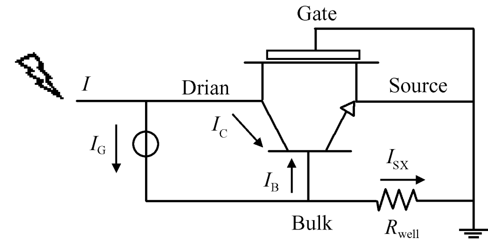

Fig. 3　A high current operation model of GGnMOS

$$V_{av} = \frac{\varepsilon E_{br}^2}{2eN_d} \tag{1}$$

where ε is the permittivity of the material, N_d is the donor concentrations, e is the unit electron charge which is typically -1.602×10^{-19} coulomb (C), and E_{br} is the breakdown field in the depletion region of the junction[6]. The concentrations of n^+ diffusion across the wells is larger than the concentrations of n-well, so the V_{av} value of n^+ modified DDSCR is smaller. However, because of the deeper STI isolation, the triggering voltage (~11V) of the n^+ modified DDSCR could be still somewhat too high to effectively protect the thin gate oxide of input stages in the same process. Therefore, this kind of DDSCR has to be cooperated with a secondary protection device to perform the overall ESD protection function for input stages.

3　MOSFET embedded DDSCR devices

In this specific 0.18μm CMOS process, the depth of STI is about ~0.53μm, but the junction depth of p^+/n^+ diffusion is only about ~0.2/0.18μm. The deeper STI region in the device creates a longer current path from the anode to the cathode, which not only makes higher breakdown voltage but also leads to a slower turn-on speed of the DDSCR. To more effectively protect the input stages and even output stages, the MOSFET embedded DDSCRs with reduced STI isolation regions are invented. A pMOS embedded DDSCR called PLVT_DDSCR is based on pnpnp structure without additional process. An nMOS embedded DDSCR called NLVT_DDSCR is based on npnpn structure by using an extra T-well mask in mixed mode RFCMOS process. However, the extra T-well mask will increase costs.

A GGnMOS model is shows in Fig. 3. In parallel with the drain and source diffusion, a parasitic lateral BJT is formed. The total drain current can be expressed as a function of the parasitic bipolar current and the thermal generation current:

$$I = I_C + I_G \tag{2}$$

where the generation current can be expressed as

$$I_G = (M-1)I_C \tag{3}$$

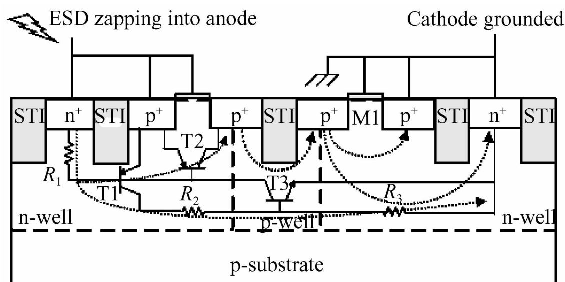

Fig 4 Device structure of PLVT_DDSCR

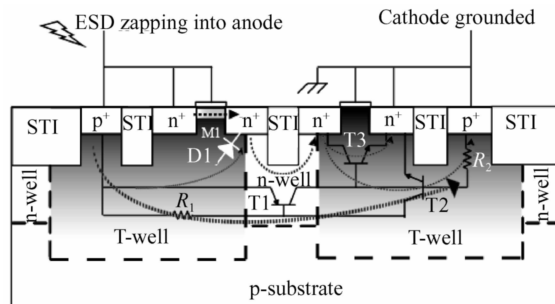

Fig. 5 Device structure of NLVT_DDSCR

M is the avalanche multiplication factor that should satisfy the form:

$$M = \frac{1}{1 - \left(\frac{V_D}{V_{av}}\right)^n} \tag{4}$$

The power factor n of this relationship is a function of the doping profile at the metallurgical junction. The substrate current can be estimated as

$$I_{SX} = I_G - I_B \tag{5}$$

We can express the voltage drop in the substrate as

$$V_{SX} = I_{SX} R_{well} \tag{6}$$

The triggering voltage of GGnMOS is the value of V_D when V_{SX} reaches ~0.7V[6]. So in this situation, the GGnMOS is triggered off before the original avalanche breakdown voltage V_{av}. A similar working mechanism applies to GDpMOS except that its poly gate, source region and bulk are tied to the same high potential terminal, and its parallel parasitic lateral BJT is a pnp transistor.

3.1 PLVT_DDSCR device design

The compact device structure of PLVT_DDSCR is shown in Fig. 4. As a positive ESD pulse is applied to the anode terminal of the device with respect to the grounded cathode terminal, the gate of the pMOSFET at the pulsed side is connected to high potential that prevents the formation of inversion region in the channel. The BC (n-well/p^+) junction of its parasitic BJT (T2) of the pMOSFET is reverse biased and eventually reaches its avalanche breakdown voltage, and the device is triggered off due to GDpMOS (gate to VDD pMOS) mechanism. A large amount of electron-hole pairs are therefore generated. As the excess electrons flowing through forwarded p-well/n-well junction path, they are collected by the n^+ at the cathode terminal, a potential is built through the parasitic n-well resistor R_3 to turn on T3, and the T1 and T3 pair forms a regenerative thyristor to conduct the current. The inherent thyristor leads to a second triggering of the device. Although the bulk gate, poly gate and drain of M1 are tied together to low potential, still a sub-inversion channel is unavoidable. A portion of current will flow through the channel of pMOS M1 simultaneously. And vise versa, the same operation mechanism applied as the relative negative ESD pulse arrives.

3.2 NLVT_DDSCR device design

In HJTK advanced mixed mode RFCMOS process, besides n-well and p-well, there is a triple-well (T-well) mask, which allows circuits to be independent of the substrate bias condition and is often used to isolate the n-channel MOSFET from substrate noise. This is an advantage for noise isolation, mixed mode and dynamic threshold MOSFET applications[7]. NLVT_DDSCR is an npnpn based structure. As Figure 5 shows, the operation mechanism is almost the same as PLVT_DDSCR except the first triggering is due to the parasitic lateral BJT of GGnMOS (gate grounded nMOS) at the opposite side of ESD pulse, and the inversion channel of nMOSFET (M1) at the ESD pulse side of the device. Once the GGnMOS is triggered off, the channel of nMOS (M1) in the T-well is conducting some current due to its gate tied to anode terminal and the T-well isolation effect. The second triggering is due to the inherent thyristor (in this case T1&T2 pair).

4 Measurements and discussion

By using Barth 4002 transmission line pulse (TLP) testing system, a series of pulses with 100ns pulse width and a 10ns rise time by 0.5V increment are applied to the tested devices. The measurement window is set to 70% to 90% of the pulses. The failure point is defined as the leakage suddenly increased to ~μA under 2V of DC bias.

The TLP measured I-V plots of four types of the DDSCRs are shown in Fig. 6 to compare their triggering voltages (V_{t1}). The V_{t1} of original pnpnp based DDSCR (Fig. 1) and n^+ modified DDSCR (Fig. 2) are 14.4 and 11V, respectively. The n^+ diffusion across the wells cannot bring the triggering voltage under the safe margin of the breakdown voltage of the gate oxide of input stages. MOSFET embedded

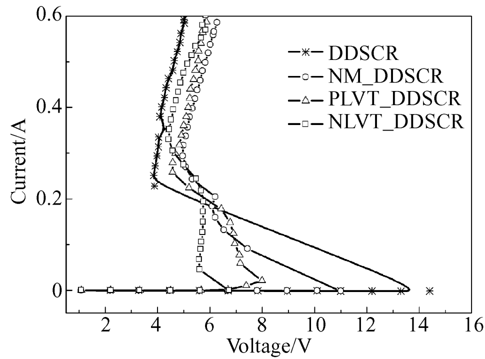

Fig.6　V_{t1} comparison of four types of DDSCRs

DDSCRs can reduce V_{t1} to 8～6.5V. As shown in the insert of Fig.7, the first triggering mechanism is by parasitic lateral BJT of the GDpMOS or GGnMOS, and the second snapback is due to the inherent thyristor of the device structures. There is a good symmetrical

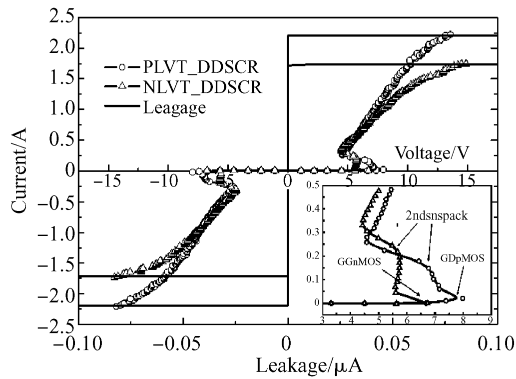

Fig.7　Positive and negative TLP *I-V* plots and leakage of LVT_DDSCR

Table 1　TLP results of four types of DDSCRs

DUT	V_{t1}/V	V_h/V	I_{t2}/A	ESDV/（V/μm)
DDSCR	14.40	3.85	2.29	98.28
NM_DDSCR	11.00	5.06	2.30	98.63
PLVT_DDSCR	7.90	4.12	2.19	93.94
NLVT_DDSCR	6.74	4.43	1.74	74.63

TLP *I-V* characteristic for positive and negative ESD stresses (Fig.6). The relative high holding current (260～330mA) and holding voltage (more than 2V) can help to the latch-up immunity.

5　Conclusion

In HJTK 0.18μm mixed mode RFCMOS technology, the pnpnp based dual direction SCR without an extra T-well is successfully realized. n^+ modified DDSCR reduces triggering voltage to some extent. pMOS embedded low triggering DDSCR can bring triggering voltage below 8V. What's more, by using an extra T-well mask, nMOS embedded low triggering DDSCR can bring triggering voltage below 7V or even lower. The low voltage triggering DDSCR ESD device features a second snapback symmetric *I-V* characteristic without latch-up problem. Its relative I_{t2} value equals more than 3.5kV HBM ESD failure voltage, and translates into a very high ESD performance of 94V/μm. And the comparison of various DDSCRs is summarized in Table 2. This compact ESD design reduces silicon area and ESD induced parasitic effects significantly. It can be used for VDSM and RF on-chip ESD protection applications.

Table 2　Comparison of various DDSCRs

Process (Designer)	DDSCR type	Triggering mechanism	Triggering voltage/V	Turn-on speed	Latch-up issue	Design complexity	Overall performance
0.6μm BiCMOS (A. Wang)	DDSCR	Avalanche breakdown	23	Slow	Yes	Middle	Middle
	LVT_DDSCR	External Zener breakdown	7.8	Middle	Yes	High	Good
0.18μm Logic CMOS (Author)	DDSCR	Avalanche breakdown	14.4	Slow	No	Low	Middle
	NM_DDSCR	Avalanche breakdown	11	Slow	No	Low	Middle
	PLVT_DDSCR	GDpMOS	7.9 (Tunable)	Fast	No	Middle	Good
0.18μm MM_RFCMOS (Author)	NLVT_DDSCR	GGnMOS	6.7 (Tunable)	Fast	No	Middle	Good

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0.18μm 混合信号 RFCMOS 工艺中新型低触发电压双向 SCR 静电防护器件的设计*

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摘要： 提出了一类新型片上 SCR 静电放电防护器件，此类器件用于保护芯片双向抗击静电应力.比较和分析了四种双向 SCR 器件的触发电压.其中采用嵌入 pMOS 管或 nMOS 管的双向 SCR 器件结构具有可调触发电压，低漏电流(～pA)和开启速度快的骤回 *I-V* 特性，并且没有闩锁问题.该器件的抗 ESD 能力可达～94V/μm.此类新型 ESD 防护器件具有面积小、寄生效应小的特点.

关键词： 静电放电；双向 SCR；骤回
PACC： 4110D；4400；7340L **EEACC：** 5110；2560；1280
中图分类号： TN402 **文献标识码：** A **文章编号：** 0253-4177(2008)11-2164-05

* 江苏省自然科学基金(批准号:BK2007026)及浙江省自然科学基金(批准号:Y107055)
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2008-04-05 收到,2008-07-24 定稿
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