High-Consistency Behavior Modeling of a Switched-Capacitor Sigma-Delta Modulator in SIMULINK*

Ou Wei and Wu Xiaobo†

(*Institute of VLSI Design, Zhejiang University, Hangzhou* 310027, *China*)

Abstract: To improve the simulation accuracy of SIMULINK, a novel inclusive behavior model of an integrator is proposed that introduces the effects of different circuit nonidealities of a switched-capacitor sigma-delta modulator into SIMULIK simulation. The nonlinear DC gain and nonlinear settling process are introduced into the op-amp module. The signal-dependent charge injection and nonlinear resistance are introduced into the switch module. In addition, the noise source including flicker and thermal noise is introduced into system as an independent module. The novel model is verified by SIMULINK behavioral simulations. The results are compared with results from circuit level simulation in Cadence SPICE using TSMC 0.35μm mixed signal technology. It shows that the novel model succeeds in introducing the influences of the nonidealities into behavior simulation to more realistically describe the circuit performances and increase the accuracy of SIMULINK simulation.

Key words: sigma-delta modulator; nonlinear DC gain; feed-through; slewing distortion; phase margin; charge injection

EEACC: 2570D

CLC number: TN432 **Document code**: A **Article ID**: 0253-4177(2008)11-2209-09

1 Introduction

An A/D converter is the only channel through which signals can be transferred from natural environment to digital processors. Recently, it has been widely applied to modern electronic equipment, including portable products powered by batteries, which are required to work in low voltage, low power conditions. Since Σ-Δ data converters can meet this requirement inherently, they have attracted a lot of interest.

A Σ-Δ data converter is comprised of an analog modulator and a digital filter. As the development of modern integrated circuit (IC) technology, its feature size and the supply voltage are continuously scaling down. The modulator design becomes a great challenge when high performance is demanded.

The Σ-Δ modulator is usually implemented in two different configurations——switch capacitor (SC) and continuous time (CT). The CT modulator may consume lower power in some cases; however, it is inherently too sensitive to some non-idealities like clock jitter and mismatching. Moreover, it has poor compatibility with standard CMOS technology. In contrary, the SC modulator is robust and insensitive to these non-idealities. Furthermore, it has good compatibility with standard CMOS technology. So the SC modulator is being applied more recently. This paper is focused on the SC modulator.

Although the SC Σ-Δ modulator is relatively stable and robust, there are still a lot of issues in its design when high performance is required, especially in low voltage, low power cases. For example, when supply voltage is reduced, the DC gain of op-amp and its linearity will become poor, and so does the transient response. This causes a nonlinear issue to the system and results in the performance degradation. Thus, it is worthwhile for circuit designers to analyze it.

In IC design, the circuit level simulation using SPICE is usually regarded as the most accurate way to predict the circuit performance. However, while the system is very large, it will occupy too many computer resources and take too long in practice. Alternatively, simulation based on the macro-model in SIMULINK can achieve both high accuracy and time efficiency as long as accurate enough models are available. This is the target of the research on behavior modeling in this paper.

There are many previous works on behavior modeling. However, not all the main nonidealities existing in real circuits[1,2], such as feedthrough, phase margin, and flicker noise, were embraced. All these factors as well as nonlinear DC gain, slew distortion, and charge injection will be analyzed in this paper. Based on the

* Project supported by the National Natural Science Foundation of China (No. 90707002)

† Corresponding author. Email: wuxb@vlsi.zju.edu.cn

Received 7 April 2008, revised manuscript received 18 July 2008

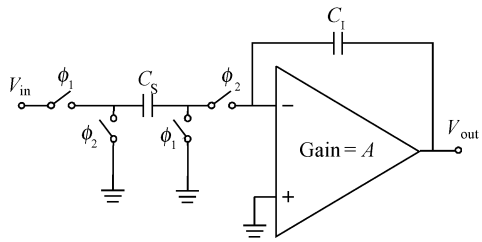


Fig. 1 Single-ended SC integrators

analysis, the behavior model is proposed and added to SIMULINK. The model is applied to simulate a three order single bit Σ-Δ modulator. The results are compared with that simulated in Cadence SPICE using TSMC 0.35μm mixed signal technology to verify the developed model.

2 Integrator nonidealities analysis

Figure 1 shows a single-ended integrator that is comprised of an S/H circuit and an op-amp with capacitor feedback. Suppose the integrator is ideal, then the switch resistance and parasitic capacitor of the S/H circuit can be omitted; and the op-amp has no transfer delay and an infinite gain. Equation (1) is the ideal transfer function. Of course, these assumptions are not valid in actual circuits. Thus, the ideal transfer function should be modified according to practical situations to improve the simulation accuracy. In this chapter, the performance of a real op-amp and its effect on the transfer function of integrator will be discussed.

$$H(z) = \frac{C_S}{C_I} \times \frac{z^{-1}}{1 - z^{-1}} \tag{1}$$

2.1 Finite gain

Because of the finite gain of real op-amps, it is impossible to transfer charges from the sampling capacitor to the integrating capacitor fully at each period. Therefore, the output voltage can not reach the expected value, causing a gain error and pole location error in the transfer function of the integrator.

Equation (2) is the charge transfer function for a given period. Equation (3) is the z-domain voltage transfer function. They both differ from the ideal transfer function in gain and pole error. These errors will result in the noise floor rising and leakage in the cascade structure. Figure 2 (b) is their realization in SIMULINK. The structure of the integrator is different from the popular, one shown in Fig. 2 (a).

$$q_I(n) = q_I(n-1) + C_I\left(V_{in}(n) - \frac{Q_I(n)}{C_I(A+1)}\right) \tag{2}$$

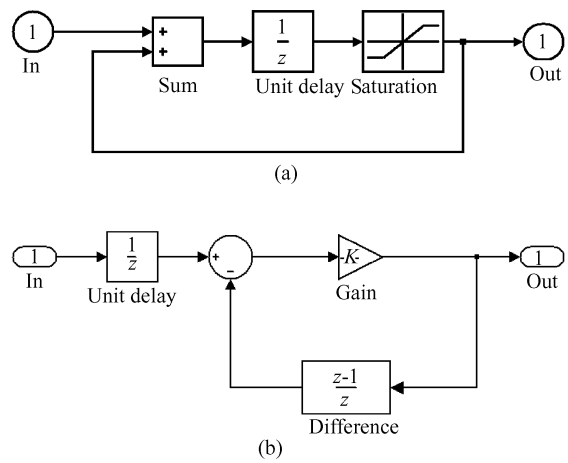


Fig. 2 (a) Conventional integrator in SIMULINK; (b) Improved integrator in SIMULINK

$$H(z) = p\frac{C_S}{C_I} \times \frac{z^{-1}}{1 - pz^{-1}}, \quad p \approx 1 - \frac{1}{A} \tag{3}$$

The improved integrator features a distinct structure that contains a differential block in the feedback path. The differential block behaves as a feedback capacitor in the integrating phase, which senses the output voltage and feedback current through detecting the differential voltages[3].

2.2 Nonlinear DC gain

Analysis of finite gain is based on the assumption of constant gain. However, this is not true in real circuits. Actually, the gain varies with the change of input signals, which is illustrated in Fig. 3.

In Fig. 3, the output resistance of an op-amp is expressed as $r_{o1} // r_{o2}$, where r_{o1} and r_{o2} are the channel resistance of the output transistors M1 and M2 respectively. $r_{o1} \propto 1/\lambda_I I_1$, $r_{o2} \propto 1/\lambda_{II} I_2$, where I_1, I_2 is the output currents and λ_I, λ_{II} are the channel-length modulation coefficients of M1 and M2. In proper design, both M1 and M2 are working in the saturation region and can be described as Eq. (4). Parameter λ is dependent on the overdrive voltage V_{gs} in Eq. (5), where λ_0 and λ_1 are decided by process[4].

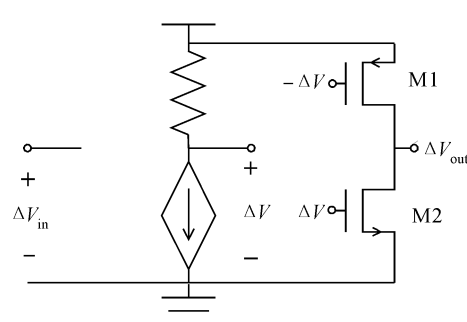


Fig. 3 Simplified structure of a two stage op-amp

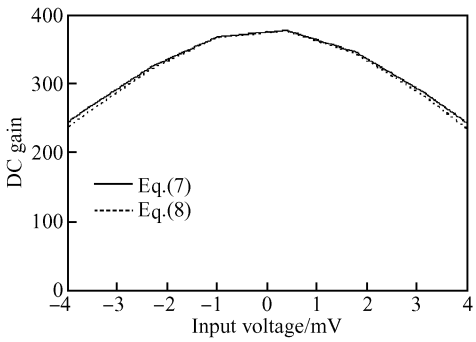


Fig. 4　Nonlinear DC gain versus input

$$I_{out} = \frac{\beta}{2}(V_{gs} - V_{th})^2(1 + \lambda V_{ds}) \tag{4}$$

$$\lambda = \lambda_0[1 + \lambda_1(V_{gs} - V_{th})] \tag{5}$$

Usually, parameters of output transistors are symmetrically designed to keep the quiescent output voltage around the midpoint of the supply voltage. For simplicity, both nMOS and pMOS are assumed to have the same overdrive voltage V_{od}, β, λ_0, and λ_1. Assuming that the currents through both transistors are equal, using square law equation (4), the ΔV_{out} can be expressed as Eq. (6).

$$\Delta V_{out} = \frac{(V_{od} + \Delta V)^2 - (V_{od} - \Delta V)^2 + \lambda_0 V_{vdd}(V_{od} - \Delta V)^2[1 + \lambda_1(V_{od} - \Delta V)]}{\lambda_0[(V_{od} + \Delta V)^2 + (V_{od} - \Delta V)^2 + \lambda_1(V_{od} + \Delta V)^3 + \lambda_1(V_{od} - \Delta V)^3]} \tag{6}$$

$$\frac{d\Delta V_{out}}{d\Delta V} = 2\frac{\alpha}{\lambda_0\beta} - 2\frac{\alpha}{\lambda_0\beta^2}(4\Delta V + 3\lambda_1(V_{od} + \Delta V)^2 - 3\lambda_1(V_{od} - \Delta V)^2) \tag{7}$$

$$\alpha = 2V_{od} - \lambda_0(V_{od} - \Delta V)V_{vdd} - 3\lambda_0\lambda_1 V_{vdd}(V_{od} - \Delta V)^2$$

$$\beta = (V_{od} + \Delta V)^2 + (V_{od} - \Delta V)^2 + \lambda_1(V_{od} + \Delta V)^3 + \lambda_1(V_{od} - \Delta V)^3$$

$$\frac{d\Delta V_{out}}{d\Delta V} = \frac{(2\lambda_0 V_{od} - 2)\Delta V^2 + 2V_{od}^2 - \lambda_0 V_{vdd} V_{od}^2}{\lambda_0[(2V_{od}^2 + 8\lambda_1 V_{od}^2)\Delta V^2 + V_{od}^3 + 2\lambda_1 V_{od}^4]} \tag{8}$$

Equation (7) is the expression of gain. Since the typical value of β, λ_0, and λ_1 are much less than the unit, and ΔV is usually on the order of magnitude of several millivolts, neglecting high order terms, Equation (7) can be reduced to Eq. (8), which shows that the gain is mainly determined by λ_0 and partially by λ_1, and V_{od} derived from the effect of overdrive voltage on channel depth. The curves of Eqs. (7) and (8) are plotted in Fig. 4 by solid and dashed lines, respectively. It can be seen that they are quite consistent with each other. In addition, the gain nonlinearity of the first stage can be neglected due to its small variations.

Figure 5 shows that a nonlinear block is introduced into the forward path of the improved integrator to model the DC gain nonlinearity of the op-amp. The settling accuracy of the integrator depends on the amplitude of the input signal. Compared with the method mentioned in Ref. [2], this model provides a more direct guide in circuit design.

2.3　Settling behavior

Figure 6 (b) is the step response of a unit gain feedback op-amp, and Figure 6 (a) shows the structure of the op-amp. The response can be divided into three distinct parts: feedthrough, slewing, and linear settling. Equation (9) is the expression for the linear settling process when the step input is applied.

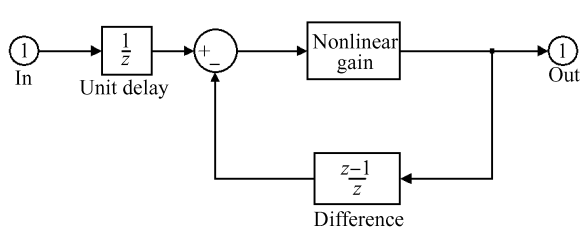
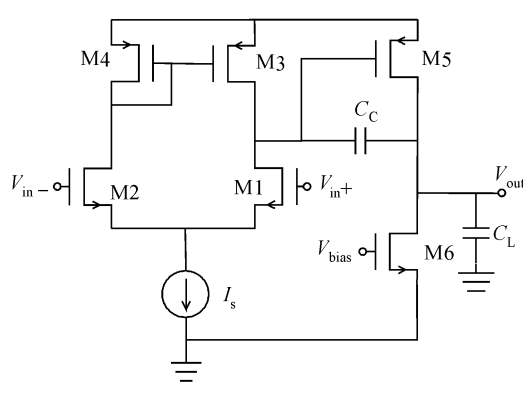
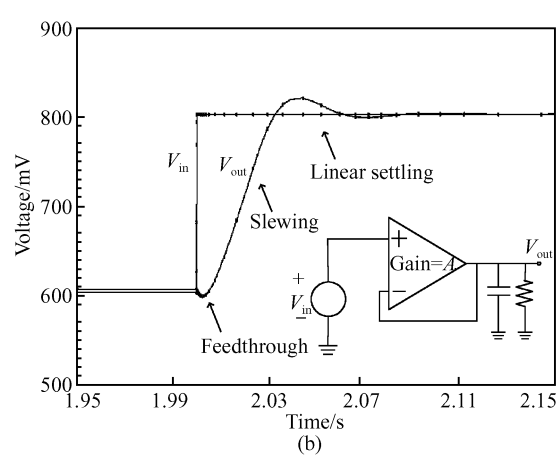


Fig. 5　Nonlinear block in SIMULINK



(a)



(b)

Fig. 6　(a) Two stage op-amp; (b) Step response of op-amp

$$V_{\text{out}} = 1 - \frac{p_2(\text{GBW} + z)}{\alpha} e^{\frac{\text{GBW}}{z}t} e^{-\frac{1}{2}p_2 t} \sinh\left(\frac{1}{2}\alpha t\right) + p_2(\text{GBW} + z) e^{\frac{\text{GBW}}{z}t} e^{-\frac{1}{2}p_2 t} \cosh\left(\frac{1}{2}\alpha t\right)$$

$$\alpha = \sqrt{p_2^2 z^2 - 2p_2^2 z\text{GBW} + p_2^2 \text{GBW}^2 - p_2 z^2 \text{GBW}} \quad (9)$$

where GBW is the unit-gain bandwidth of the op-amp, and z is the RHP zero caused by Miller capacitor, both in rad/s.

Feedthrough is caused by the existing RHP zero, which was often overlooked in previous works. However, it is important because it will result in a signal-dependent settling error. As expressed by Eq. (9), the RHP zero increases the real part of the time constant and makes its product with the sum of hyperbolic sine and hyperbolic cosine terms larger than a unit. Then, the output becomes negative first and slows down the settling process. The effect of feedthrough can be regarded as a reduction of effective settling time. The time reduction is determined by V_{in} and slew rate.

Slewing is another nonlinear phenomenon in step response. The reduced time for linear settling due to slewing is signal-dependent. That makes the settling inaccuracy arise and become input-dependent. It may be serious because in this case the quantizer input is not white as it should be. Theoretically, slewing time can be found by analyzing the behavior of the op-amp from stop of slewing to linear settling. However, slewing time is still affected by the op-amp structure and signal, and thus it is hard to obtain. For example, the slewing time of a two stage op-amp should be found by solving the transcendental equation as Eq. (11), which is proved to have no analytical solution. Numeric simulation seems to be an approach. However, it is still unadoptable in the block description in SIMULINK because it will consume too many computer resources. Fortunately, an alternate approach is available since the slewing duration for a two stage op-amp is very close to that of a one stage op-amp if they have the same GBW. Equation (12) shows that the solution for a one stage op-amp is easy to get. Thus, by solving it, the slewing time of a two stage op-amp can be found.

$$\frac{Ap_1 p_2(e^{-p_1 t} - e^{-p_2 t})}{p_2 - p_1}(V_{\text{in}} - \text{SR} \times t) = \text{SR} \quad (11)$$

$$Ap_1 e^{-p_1 t}(V_{\text{in}} - \text{SR} \times t) = \text{SR} \Rightarrow t \approx \frac{V_{\text{in}}}{\text{SR}} - \frac{1}{Ap_1} \quad (12)$$

where A is the DC gain, p_1 is the dominant pole, and p_2 is the second dominant pole, both in rad/s.

Linear settling is a small signal process and it is easier to predict it than slewing and feedthrough. In common consideration, GBW is the main factor to determine the settling performance. However, it is also influenced by the phase margin in limited slew rate and GBW. Inadequate PM will result in unstable settling according to input and bias conditions, which is another source of harmonic generation.

A proper choice of GBW and PM will improve the system performance[5]. It is recommended to use a moderate phase margin and a large GBW to minimize the overall settling error and alleviate the requirements of slew rate and power consumption.

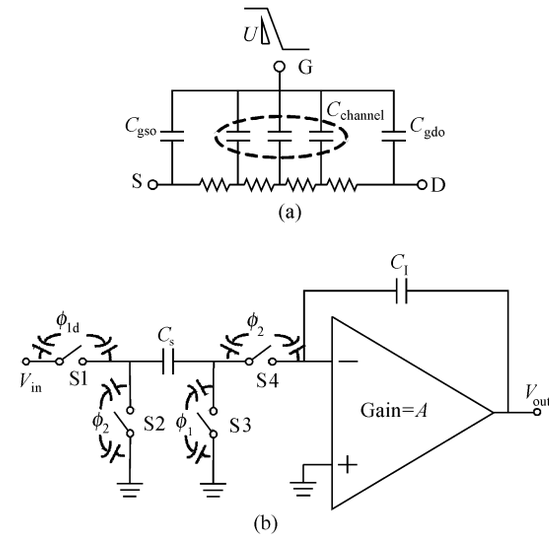


Fig. 7 (a) Nonideal switch model; (b) Charge error contribution

3 Switch nonidealities analysis

Figure 7 (a) is a nonideal model of a switch. When the switch is off, the charges stored in the channel and overlap capacitors of the MOS transistor will be released and injected into the sampling or integrating capacitor. The injection can be divided into two cases: the slow case, as shown in Eq. (13), and the fast case, as shown in Eq. (14). Usually, the fast case is more serious and it will be discussed later.

$$V_{\text{error}} = \frac{2C_{\text{gdo}} + C_{\text{channel}}}{2C_s} \times \sqrt{\frac{\pi UC_s}{2\beta}} + \frac{C_{\text{gdo}}}{C_s}(V_s + V_{\text{th}} - V_l), \quad U > \frac{\beta V_{\text{ht}}^2}{2C_s} \quad (13)$$

$$V_{\text{error}} = \frac{2C_{\text{gdo}} + C_{\text{channel}}}{2C_s} \times \left(V_{\text{ht}} - \frac{\beta V_{\text{ht}}^3}{6UC_s}\right) + \frac{C_{\text{gdo}}}{C_s}(V_s + V_{\text{th}} - V_l), \quad U > \frac{\beta V_{\text{ht}}^2}{2C_s} \quad (14)$$

here $V_{\text{ht}} = V_h - V_s - V_t$, $V_g = V_h - Ut$[3],

$$C_{\text{gdo}} = wl_d C_{\text{ox}}, \quad C_{\text{channel}} = wlC_{ox} \quad (15)$$

where U is the slope of clock falling edge, V_h and V_l are the clock voltage when the switch is on and off, respectively, and V_s is the drain source voltage.

Figure 7 (b) shows the error source distribution of the charge injection in the integrator. Errors will

be introduced both in the sampling phase and the integrating phase. At the last period of the sampling phase, the charges in parasitic capacitors S1 and S3 are injected into C_s. The two parts can not cancel each other completely because V_{in} is not equal to AC ground, and the net gain charge is a polynomial function of V_{in}. In the integrating phase, the case is much better, because the charges in parasitic capacitors S2 and S4 are equal and they can counteract completely. Considering C_I, S4 absorbs charges from C_I during switching on and injects the same amount of charges during switching off, it also can be neglected and S1 can be considered as the most influential error source. Substituting Eq. (15) into Eq. (14), the charge error due to switching off can be expressed as Eq. (16), and the net charge error is Eq. (17).

$$V_e = \frac{\beta(2wl_dC_{ox} + wlC_{ox})}{12UC_s^2}V_{ht}^3 + \frac{wlC_{ox}}{2C_s}V_{ht} + \frac{wl_dC_{ox}}{C_s}(V_H - V_L) \tag{16}$$

$$V_{ne} = -\frac{\beta(2wl_dC_{ox} + wlC_{ox})}{12UC_s^2}V_{in}^3 + \frac{\beta(2wl_dC_{ox} + wlC_{ox})}{4UC_s^2}V_{ht}V_{in}^2 - \left(\frac{\beta(2wl_dC_{ox} + wlC_{ox})}{4UC_s^2}V_{ht}^2 + \frac{wlC_{ox}}{2C_s}\right)V_{in} \tag{17}$$

where l_d is the lateral diffusion length of the drain underneath the gate. In TSMC 0.35μm mixed signal technology, l_d is 1.2×10^{-7} m, C_{ox} is 4.6×10^{-3} F/m^2, and $t_{ox} = 7.5\times10^{-9}$ m.

Charge injection may result in great distortion in a low voltage circuit. To prevent it, the circuit and layout design must be careful. Some measures like dummy switches, CMOS switch, bottom plate sampling, and bootstrap switch are adoptable to improve it[2]. The modeling of signal-dependent charge injection can be realized through a polynomial module that detects the input and add its output to signal again.

The next nonideality of the switch is its nonzero and nonlinear resistance. Because it has nonzero resistance, the settling error inevitably exists. The worst case is that the resistance is determined by input voltage, which results in nonlinearity and signal dependent inaccuracy of settling. To analyze the nonlinear resistance of the switch, the Laplace transformation is used as shown in Eq. (18) and its time domain form is obtained as Eq. (19). The time constant is determined by V_{in} and clock voltage.

$$g_m = \beta(V_{gt} - V_{in}), C = C_s \Rightarrow \frac{V_{in}}{s\left(1 + \frac{sC_s}{\beta(V_{gt} - V_{in})}\right)} \tag{18}$$

$$V_s = V_{in}\left(1 - e^{-\frac{\beta(V_{gt} - V_{in})t}{C_s}}\right) \tag{19}$$

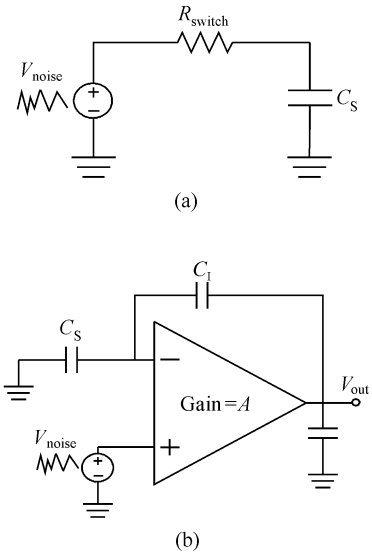


Fig. 8　(a) Switch thermal noise; (b) Op-amp thermal noise

In general, the problem caused by resistance nonlinearity is not as severe as that by charge injection. But in extremely low supply voltage conditions, it becomes the bottleneck of system performance. A bootstrap switch or clock voltage doubler can be used to avoid this problem. In case of less charge injection, the bootstrap switch is preferred[6].

4　Noise analysis

Intrinsic noise includes thermal noise and flicker noise. Thermal noise is caused by the random fluctuation of carriers due to thermal energy. It is white in spectra density and has a wide band[7]. The energy can be accumulated onto sampling or integrating capacitors, but is limited by the time constant of the switch capacitor or gain bandwidth of the op-amp, respectively, as in Fig. 8 (a). The expression of accumulated energy of thermal noise due to switch resistance is shown as Eq. (20).

$$e_n^2 = \int_0^\infty \frac{4kTR_s}{1 + (2\pi fR_sC_s)^2}\mathrm{d}f = \frac{kT}{C_s} \tag{20}$$

$$e_n^2 = \int_0^\infty \frac{16kT}{3g_{m1}}\left|\frac{\beta g_{m1}G_0}{\beta g_{m1} + 2\pi fC_0}\right|^2\mathrm{d}f = \frac{4kT}{3C_0} \tag{21}$$

where k is the Boltzmann's constant and T is the temperature in Kelvin. A Gaussian random block with unit variance and a constant block equal to kT over C_S are used for modeling and the product of their output can be regarded as the switch thermal noise.

Op-amp thermal noise can be regarded as input referred noise, shown in Fig. 8 (b), and the expression of accumulated noise energy on the integrating capacitor is expressed as Eq. (21). The effective output capacitor can be structurally different. In a one stage op-amp, it is determined by C_{load}, C_I and C_S. But in a

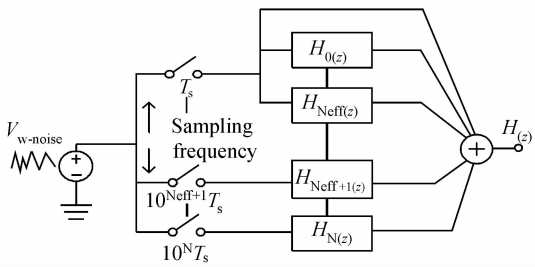


Fig. 9 Realization of flicker noise model

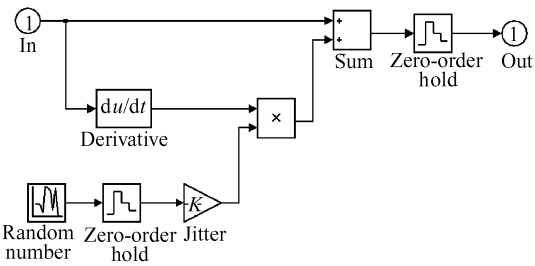


Fig. 11 Clock jitter realization

2nd order op-amp, it equals C_C[8].

Flicker noise is also called $1/f$ noise. It exists in association with a direct current and has a spectral density that is inversely proportional to frequency. Adding an offset to the op-amp input straightforwardly fails to model the influence of flicker noise effectively because their behaviours are quite different in both the time and frequency domains. As shown in Fig. 9 the modeling of flicker noise can be realized by using a combination of subfilters described as Eq. (23) to filter the white noise and get the mock flicker noise[9].

$$S_{1/f}(f) = \frac{k}{wlf} \tag{22}$$

$$H(z) = 1 + \sum_{n=0}^{N} \frac{10^{-0.5n}\sqrt{2}\pi f_c T_s}{1 - z^{-1}\exp(-2\pi 10^{-n} f_c T_s)} \tag{23}$$

where N represents the number of the subfilters, and each subfilter is single order. Figure 10 depicts the transient and frequency response, which are close to the theoretical ones. Thermal noise is usually the main consideration when high resolution or wide signal band is required. Augmenting the sampling capacitor can minimize this problem, but at the cost of increasing the chip area and power consumption. Some measures like correlated double sampling and chopper stabilization can be used to diminish its effect.

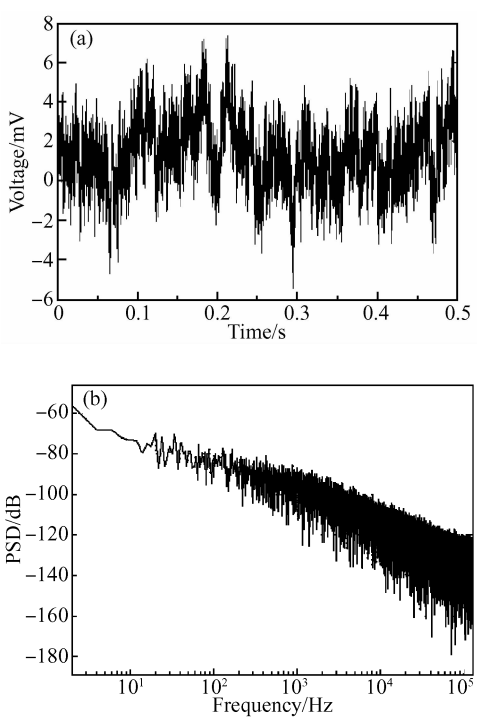


Fig. 10 (a) Transient response of flicker noise; (b) Spectral density of flicker noise

5 Clock jitter

Clock jitter is introduced by the non-uniform sampling of the input signal. This effect increases the total error power at the system output. The magnitude of this error is a function of the statistical properties of the jitter and the input signal to the system[1]. When the input is a sinusoidal, the error can be expressed as

$$x(nt + \delta) - x(t) \approx 2\pi f_{in}\delta A\cos(2\pi f_{in} nt) = \delta\frac{\mathrm{d}}{\mathrm{d}t}x(t) \tag{24}$$

where δ is the sampling uncertainty. This error can be modeled by a combination of Gaussian random block with unit variation and derivation block of the input as shown in Fig. 11.

6 Simulation and validation

Figure 12 shows the entire behavior model in SIMULINK, which takes noise and nonidealities of the integrator into consideration. As mentioned above, these nonidealities can greatly influence the performance of the SC Σ-Δ modulator under certain conditions. A comparison of simulation results between ideal and nonideal modulators is illustrated in Fig. 13. Many nonidealities like charge injection, slew limitation, low phase margin, and gain nonlinearity result in an obvious degradation of the system performance.

Phase margin is usually overlooked because enlarged slew rate and gain bandwidth can alleviate its effect. But as more strict requirements are requested in low voltage low power applications, it can not be neglected. Figure 14 shows the effect of different phase margins on the 3rd harmonic generation when slew rate and gain bandwidth are limited. When the

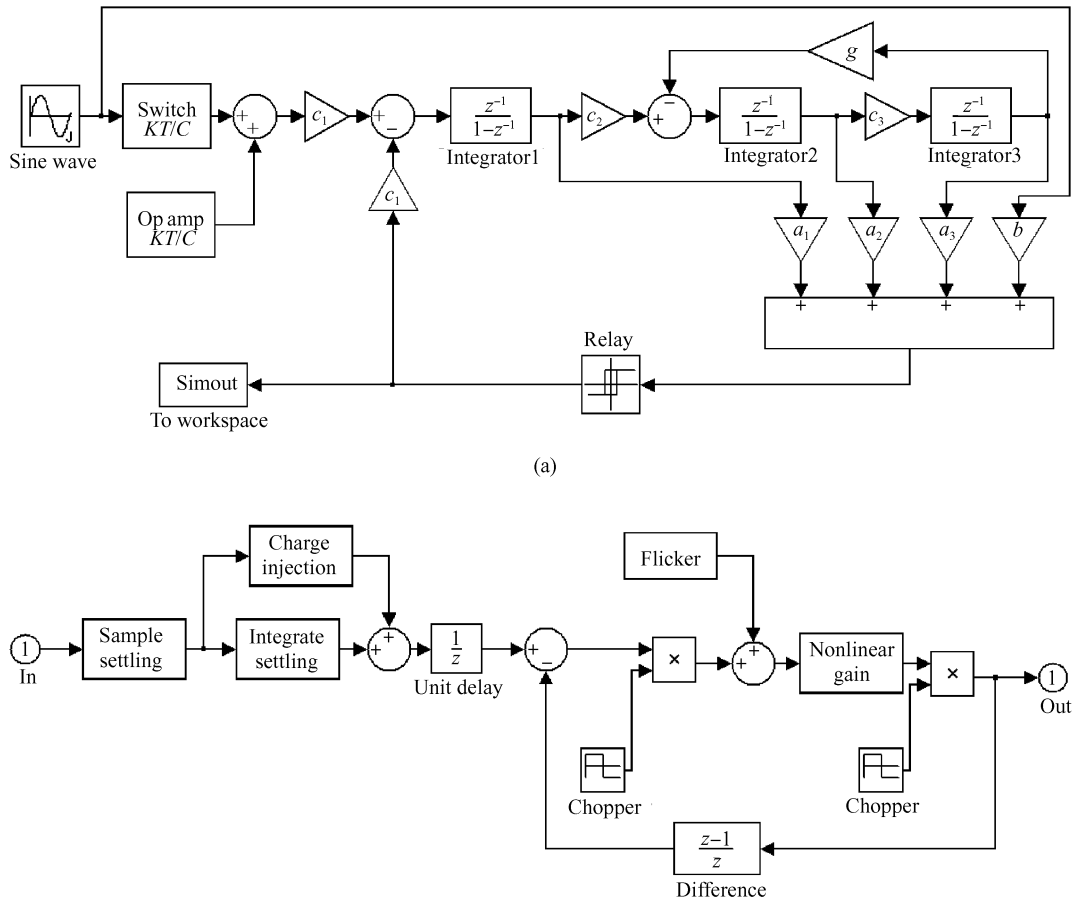


Fig. 12　(a) Nonideal three order single bit modulator; (b) Nonideal model of the first integrator

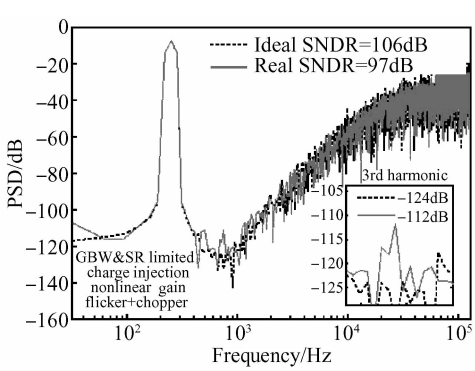


Fig. 13　Output PSD between ideal and nonideal modulator

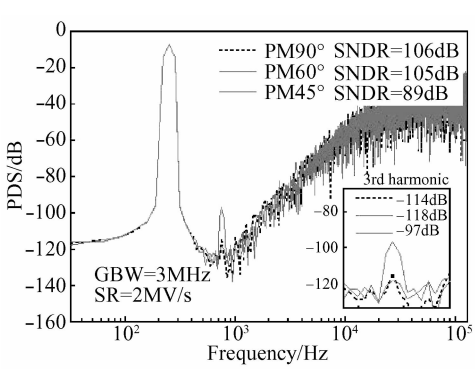


Fig. 14　Output PSD when different phase margins included

phase margin is smaller than 45°, the third harmonic is obviously higher than the noise floor. Under 60° of phase margin, it just behaves like that of 90°. Based on this simulation, it is easy to determine the floor level of the slew rate, gain bandwidth, and phase margin and then get lowest power compensation while not degrading the performance significantly.

A high dynamic range for an SC Σ-Δ modulator is an important target of the design. In ideal conditions, the simulated maximum input is usually on the high side because only the nonlinear gain of the quantizer

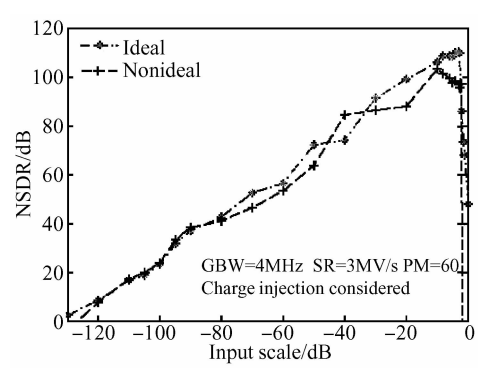


Fig. 15　Comparison of SNDR versus input between ideal and nonideal

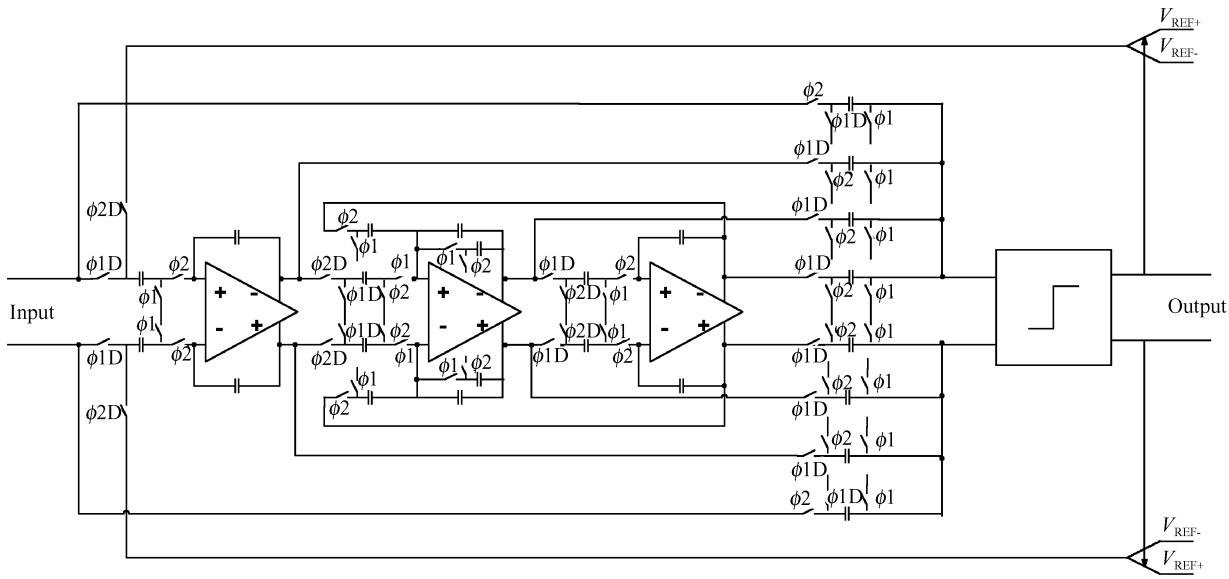


Fig. 16 Circuit implementation of three order modulator

induces the SNR degradation when large input is applied[8]. When circuit nonidealities are considered, the maximum input is greatly reduced because more nonlinear blocks exist in the loop. Figure 15 is a comparison of simulated SNDR for ideal and nonideal modulators.

Figure 16 shows the implemented circuit of the mentioned modulator. The specifications of the building blocks are listed in Table 1. It is simulated by Cadence SPICE in TSMC 0.35μm mixed signal technology.

Figure 17 shows the output PSD curves of the circuit simulated by SIMULINK model and Cadence SPICE, respectively. The parameters listed in Table 1 are adopted for both. The curves show that the simulated output spectra densities of SIMULINK are consistent with that of SPICE.

Table 2 shows the comparison of simulation time, accuracy, and coverage between the SPICE and SIMULINK simulation while nonideal models are introduced. Here, the simulation time is that spent for scanning 8192 FFT points while the accuracy option

Table 1 Parameters of modulator shown in Fig. 16

Parameter	Value
Oversampling ratio, OSR	128
Clock frequency/kHz	256
Input sinusoidal frequency/Hz	250
c_1, c_2, c_3	1/5, 1/3, 1/6
a_1, a_2, a_3	3, 4, 4
b	1
g	1/500
DC gain/dB	55
Slew rate/(MV/s)	3
Unit gain bandwidth/MHz	4
Phase margin/(°)	60

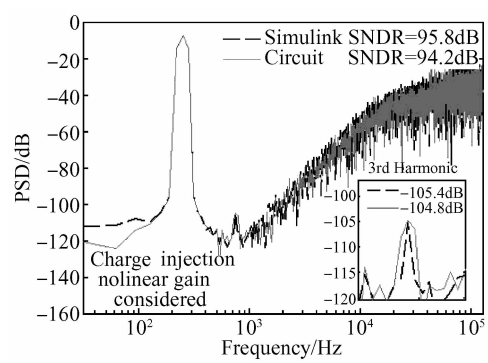


Fig. 17 Comparison of PSD between SPICE and Simulink simulation while nonideal models are introduced

of transient simulation in Cadence SPICE is moderate. Although the accuracy of the SPICE simulation is good, it fails to introduce the models of transient flicker noise and thermal noise to predict the effects of noises. Verilog-AMS is more flexible than SPICE, but it also has no flicker noise source model. SD Toolbox[10] is based on the behavior simulation in a SIMULINK environment, which is similar to this work, so that a very short simulation time is achieved. However, many nonidealities like inadequate phase margin, feed through, and flicker noise are lacking in this

Table 2 Comparison with other simulation methods

	Time	Accuracy	Coverage
SPICE	☹ (12h36min)	☺	☺
Verilog-AMS	😐 (8min43s)	☺	☺
SD toolbox	☺ (23s)	😐	😐
This work	☺ (57s)	☺	☺

tool. Therefore, its accuracy is much lower than that of this work. Table 2 shows that the behavior models presented in this paper have the best cost-effectiveness among these methods.

7 Conclusion

In this paper, an inclusive and precise behavior model of an SC sigma-delta modulator in SIMULINK was proposed. The considerations for the model construction include finite DC gain and its nonlinearity, feedthrough, limited slew rate, limited GBW, inadequate phase margin, nonlinear switch resistance, charge injection, and noises. A real circuit based on TSMC 0.35μm mixed signal technology was accomplished and simulated using Cadence SPICE. The consistency between SIMULINK and Cadence SPICE simulations verified the developed novel model.

Acknowledgments The authors would like to thank Mr. Bill Liu and other engineers of ADI, for their useful discussion and technical support.

References

[1] Malcovati P, Brigati S, Francesconi F, et al. Behavioral modeling of switched-capacitor sigma-delta modulators. IEEE Trans Circuit Syst, 2003, 50(3): 352

[2] Zare-Hoseini H, Kale I, Shoaei O. Modeling of switched-capacitor delta-sigma modulators in SIMULINK. IEEE Trans Instrum Meas, 2005, 54(4): 1646

[3] Allen P E, Hollberg D R. CMOS analog circuit design. Oxford, Tennessee: Oxford University Press, 2002

[4] Category: Product, File: Spectre Circuit Simulator Device Model Equations Ver. 5, Available: Cadence

[5] Roh J. A 0.9-V 60-μW 1-bit fourth-order delta-sigma modulator with 83-dB dynamic range. IEEE J Solid-State Circuits, 2008, 43(2): 361

[6] Yao S. Modifications for reliability of bootstrapped switeches in low voltage switched-capacitor circuit. IEEE EDSSC, Proceedings, 2005

[7] Norsworthy S R, Schreier R, Temes G C. Delta-sigma data converters. Piscataway, NJ: IEEE Press, 1997

[8] Schreier R, Temes G C. Understanding delta-sigma data converters. Piscataway, NJ: IEEE Press, 2005

[9] Terry S C. Time-domain noise analysis of linear time-invariant and linear time-variant systems using MATLAB and HSPICE. IEEE J Solid-State Circuits, 2005, 52(3): 805

[10] Category: Control Systems, File: SD Toolbox [Online] Available: http://www.mathworks.com/matlabcentral/fileexchange

基于 SIMULINK 的开关型 Σ-Δ 调制器行为级建模*

欧　伟　吴晓波†

（浙江大学超大规模集成电路设计研究所，杭州　310027）

摘要：为精确反映多种非理想因素对开关型 Σ-Δ 调制器的影响，提高其在 SIMULINK 仿真器下的仿真精度，针对 SIMULINK 的行为级建模提出一种新的积分器模型. 主要的改进之处包括：在运放模块中引入了有关直流增益非线性及信号建立过程非理想性的考虑，在开关模块中引入了电荷注入效应和导通阻抗的信号相关性影响，并将噪声模型作为独立模块引入系统. 应用该模型进行 SIMULINK 仿真，并与 TSMC 0.35μm 混合信号工艺下 SPICE 仿真结果进行比较验证. 结果表明，所提出的模型成功地反映了上述因素对电路的重要影响，模型的应用提高了 SIMULINK 的仿真精度.

关键词：Σ-Δ 调制器；非线性直流增益；馈通；转换失真；相位余度；电荷注入

EEACC：2570D

中图分类号：TN432　　**文献标识码**：A　　**文章编号**：0253-4177(2008)11-2209-09

* 国家自然科学基金资助项目（批准号：90707002）

† 通信作者. Email: wuxb@vlsi.zju.edu.cn

2008-04-07 收到，2008-07-18 定稿