Design of an Active-RC Low-Pass Filter with Accurate Tuning Architecture

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Abstract: An active-RC low-pass filter of 5MHz cutoff frequency with a tuning architecture is proposed. It is implemented in 0.18μm standard CMOS technology. The accuracy of the tuning system is improved to be within (−1.24%, +2.16%) in measurement. The chip area of the tuning system is only a quarter of that of the main-filter. After tuning is completed, the tuning system will be turned off automatically to save power and to avoid interference. The in-band 3rd order harmonic input intercept point (IIP3) is larger than 16.1dBm, with 50Ω as the source impedance. The input referred noise is about 36μV_{rms}. The measured group delay variation of the filter between 3 and 5MHz is only 24ns, and the filter power consumption is 3.6mW. This filter with the tuning system is realized easily and can be used in many wireless low-IF receiver applications, such as global position systems (GPS), global system for mobile communications (GSM) and code division multiple access (CDMA) chips.

Key words: CMOS circuit design; auto tuning; active RC filter; wireless system
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1 Introduction

Integrated continuous-time active filters with precise cutoff frequency or RC time constant are widely required in many wireless applications such as GPS, GSM and CDMA. In active-RC filters, the frequency characteristics are determined by RC time constants that might change when the fabrication process, operating temperature, supply voltage or aging vary. The accurate on-chip tuning schemes should be incorporated within the filter in order to compensate the above variations and maintain the frequency responses to be within the desired specification. Tuning implies measuring filter performance, comparing it with a standard reference, calculating the error, and applying a correction to the system to reduce the error. Automatic frequency tuning of filters involves locking of the filter's response to an external reference. The reference is usually a stable resistor or a clock signal. A system clock such as crystal frequency has been agreed upon the most reliable reference[1]. There are two possible ways to tune the RC time constant, i.e. active and passive component tuning. However, the active component tuning suffers from nonlinearity. For the passive tuning, passive C or R components are adjusted within a set of discrete values[2]. For the same accuracy setting, the C tuning is preferred in practical circuit design because its frequency performance is much better than the R tuning in spite of the equivalent implementation cost [3].

In this paper, an accurate auto-tuning system is presented and used to tune a low-power 4th Butterworth active-RC leapfrog low-pass filter (LPF) [4], which is shown in Fig. 1. The tuning system in Fig. 2 is based on the discrete capacitor bank, and can be either tuned automatically or tuned through by switching a control signal outside.

2 Discrete capacitor tuning approaches

Figure 2 shows the architecture of the tuning circuit[2] including an integrator to generate the voltage ramp, a comparator, and a digital circuit to decide the control word for the main filter circuit-to-be-tuned of Fig. 1.

Figure 3 shows the concept of the capacitor tuning. A programmable capacitor bank [Fig. 3 (b)] is used to form the capacitor of the integrator in Fig. 3 (a) within both the main filter circuit and the tuning circuit. Each of the parallel capacitors can be connected or disconnected to operational amplifier (opamp) by switching on or off the switches.

As shown in Fig. 2, the integrator to generate the voltage ramp that consists of an opamp, transistors (M1, M2 and M3), a capacitor bank, an active switch,

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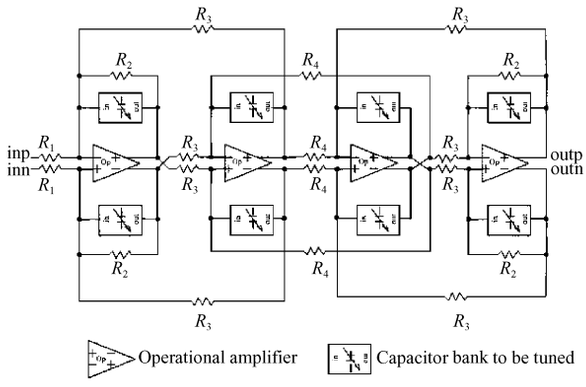


Fig. 1　Low-pass leapfrog filter to be tuned

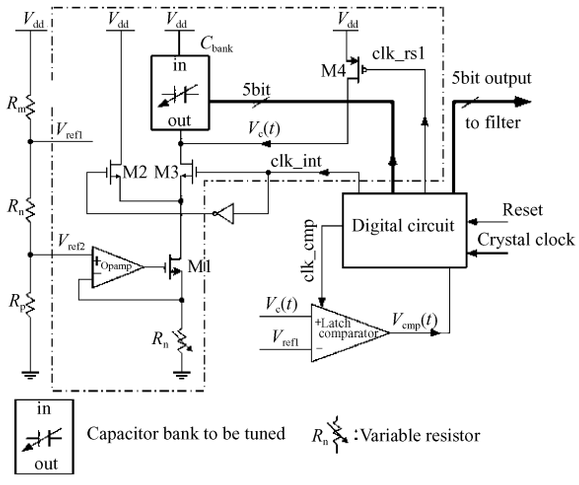
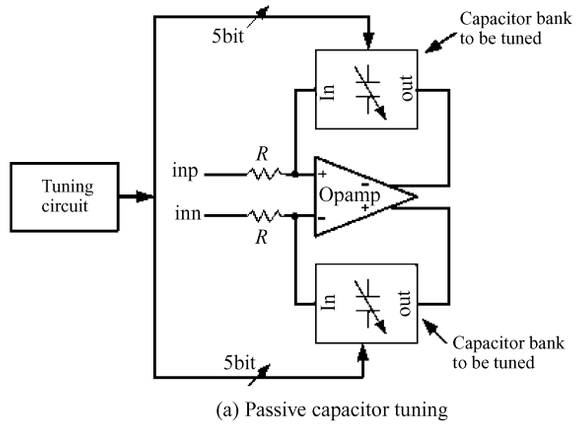
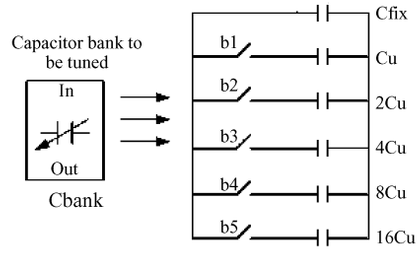


Fig. 2　Architecture of the tuning circuit



(a) Passive capacitor tuning



(b) Schematic of capacitor to be tuned(5bit)

Fig. 3　Integrator in main filter with discrete tuning (capacitor tuning) (a) Passive C tuning in active RC circuits; (b) Schematic of the capacitor bank-to-be-tuned (5bit)

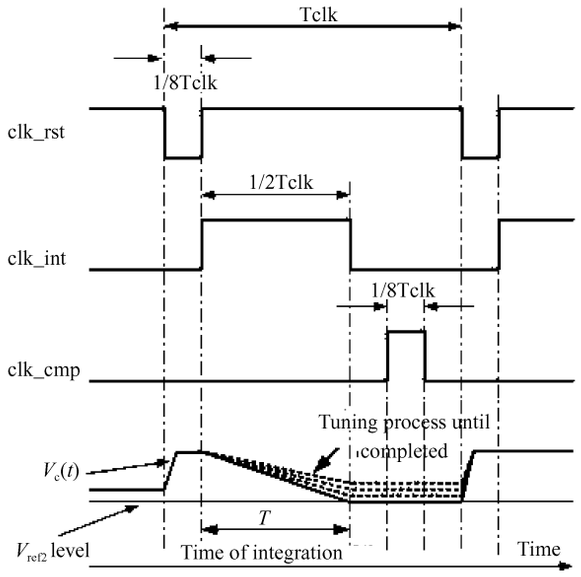


Fig. 4　Timing and waveform of the tuning circuit

an inverter and a variable resistor is presented with dashed lines. Capacitor banks with 5bit control word are developed in both the tuning circuit and the main filter.

The desired ideal output waveform of the tuning circuit with respect to the clock sequence is shown in Fig. 4 and the simulation results are shown in Fig. 8.

The gain of the opamp is high enough (about 77dB) to make the voltage across the variable resistor equal to V_{ref2}, so the current going through variable resistor is fixed. The schematic of the variable resistor is shown in Fig. 5. There are eight active switches in it. Each time only one of them is on while others are off, corresponding to 8 available different crystal frequencies as shown in Table 1. For one crystal

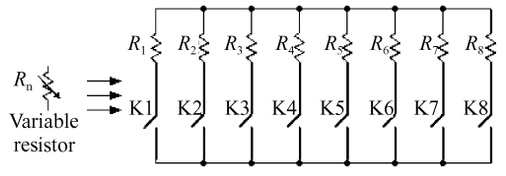


Fig. 5　Schematic of the variable resistor in tuning circuit

Table 1　Eight crystal frequencies for different usages

Usage	Crystal frequency/MHz
GPS	16.368
	18.414
GSM	13
	26
CDMA	14.4
	19.2
	19.68
	19.8

frequency, the nominal resistor value of the resistor bank can be calculated according to Eq. (5). The variable resistor will be discussed in the next section. In the tuning architecture, the resistor value of R_n is controlled by an 8bit signal generating from the SPI (serial and parallel interface) circuit of the digital part out of LPF on the chip.

The current through the variable resistor is integrated over the capacitor bank (C_{bank}) from discharging when clk_int is high. The integrator output during the integration can be expressed as[2]

$$V_c(t) = V_{dd} - \frac{V_{ref2}}{R_n C_{bank}} t \quad (1)$$

The integration period is fixed to be T, where T equals half of the period of the signal clk_int whose duty circle is 50%. The integrator output voltage $V_c(t)$ at the end of each integration period ($V_c(T)$) varies with C_{bank}. Therefore, we can adjust the C_{bank} accordingly and compare $V_c(T)$ with a certain reference voltage V_{ref1}. For convenience, we choose V_{ref1} to be the desired value when the product of $R_n C_{bank}$ in the integrator equals the designed time constant which is corresponding to the crystal frequency values. Through the digital circuit in the tuning circuit, "11111" word is set as an initial value to the capacitor bank. And the 11111 control word makes the switches in the capacitor bank all be the on state. Then the counter in the digital circuit reduces the control word by 1 bit each step, until $V_c(T)$ reaches the reference voltage V_{ref1}. From 11111 to 00000, we always can find the proper control word for the capacitor bank which can make $V_c(T)$ furthest close to V_{ref1}. The worst case will happen when the counter counts for 32 times which is the longest time to tune[5]. If we set the initial value 00000 to the capacitor bank which makes the switch all be off state, then the case is vice versa. When clk_int is low, the integration over the capacitor bank is stopped. This turns on transistor M2 and turns off M3 to stop the current going through the capacitor bank. When clk_cmp is high, the comparison between $V_c(T)$ and V_{ref1} is activated. Once clk_rst becomes low, the voltage $V_c(t)$ at one end of the capacitor bank is reset to V_{dd} before next integration phase starts as shown in Fig. 4.

When the capacitance in the tuning integrator is tuned to the desired control word (desired capacitor value), the tuning circuit is disabled to avoid any interference on filter signal path and to reduce power consumption[5]. The control word is stored and applied to the capacitor banks in the main filter circuits. The tuning circuit can be turned on again when a recalibration signal is received. The same capacitor bank and the same kind of unit resistors applied in both the tuning circuits and the main filter circuits can make a perfect matching between the master and slave circuits[4]. So, a good RC time constant agreement between the tuning circuits and the main filter can be reached.

3 Design of tuning circuits

Then we discuss the circuit design of sub blocks in the tuning circuits.

3.1 Capacitor bank[5]

As shown in Fig. 3, the capacitance of the capacitor bank is determined by a digital control word and can be tuned to a set of discrete values.

$$C_{bank} = C_{fix} + nC_u, \quad n = 0, 1, \cdots, 2^N - 1 \quad (2)$$

where C_{fix}, C_u is a fixed capacitor and a unit capacitor respectively. Each capacitance bank must be capable of representing every value of capacitance in a specified range given by $C_{nom} \pm x\%$. C_{nom} is the nominal design value and x is the required percentage range of capacitance. We have[5]:

$$C_{fix} = C_{nom}\left[1 + \frac{x}{100}\left(\frac{1}{2^N} - 1\right)\right] \quad (3)$$

Here, we choose the tuning range of $(-50\%, +50\%)$ around C_{nom}, that is to say $x = 50$, and we choose $N = 5$, $C_u = 0.2$pF and $C_{fix} = 3.3$pF. The quantization error ε is given by

$$\varepsilon = \pm \frac{1}{\frac{2C_{fix}}{C_u} + 2n \mp 1} \quad (4)$$

The quantization error ε will be maximum when n equals to zero. The calculation shows that the maximum ε_{max} is $\pm 3.125\%$ ($\varepsilon_{max} = 1/2^N$, $N = 5$). It means the maximum quantization error ε_{max} is directly relative to N. In some applications, N is set to 4, so that the accuracy is within $\pm 6.25\%$ ($= 1/2^N$, $N = 4$). The accuracy in the latter case ($N = 4$) comparing to the former case ($N = 5$) is lower to save the capacitor bank area. The tuning accuracy within $\pm 4\%$, that is to say ± 200kHz variation for 5MHz cutoff frequency, can be tolerated for our application. So a capacitor with a 5bit control word has been chosen for chip area and accuracy trade-off[6].

3.2 Digital circuit

The digital circuit in the tuning circuit consists of two parts: a wave generator and a counter. The wave generator generates four clock signals: output clock for the counter, clk_rst, clk_int and clk_cmp. The desired and conceptual timing and waveforms of signals clk_rst, clk_int and clk_cmp are shown in Fig. 4. The frequencies of the above four clock signal have the

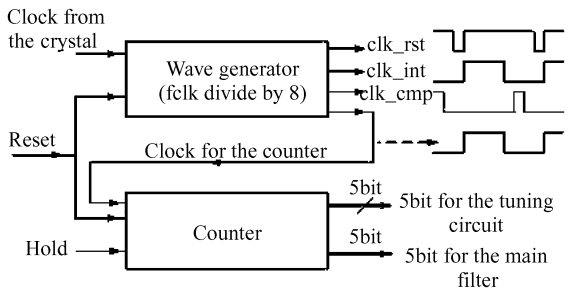


Fig. 6　Building blocks of the digital circuit in tuning circuits

same frequency and are 1/8 of frequency of crystal (f_{crystal}). The signal reset is used to re-active the digital circuits. The signal hold is linked to the comparator so that once $V_c(T)$ is furthest close to V_{ref1}, the comparator and the counter are latched up. The properly tuned control word is then sent to the main filter and saved in registers in digital circuits. And then the tuning circuit is disabled.

3.3　Variable resistor

As shown in Fig. 5 and $f_{\text{clk\_int}} = \frac{1}{8} f_{\text{crystal}}$, according to Eq. (1), we have:

$$R_n = \frac{4V_{\text{ref2}}}{(V_{\text{dd}} - V_{\text{ref1}})C_{\text{nom}} f_{\text{crystal}}} \tag{5}$$

where C_{nom} is the nominal value of capacitor bank and f_{crystal} is the crystal frequency for reference.

3.4　Comparator [6]

The comparator is used to compare $V_c(T)$ with V_{ref1} and provide a 1bit flag signal to the digital tuning logic to lock the control word of the capacitor bank. Then the digital circuit feeds back a latch signal to latch the D flip-flop (DFF) in the comparator as shown in Fig. 7.

4　Simulation results

Simulation results are listed in Table 2. There are

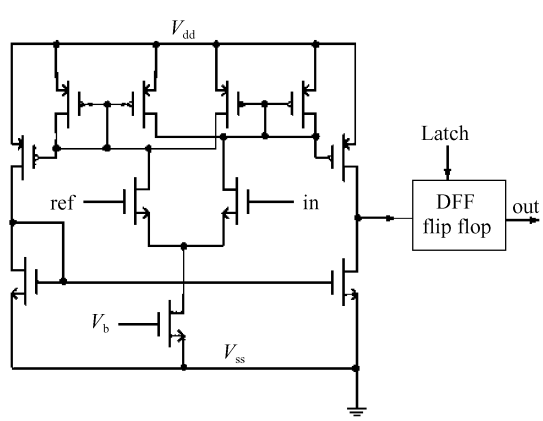


Fig. 7　Comparator used in the auto-tuning circuit

Table 2　simulation results of the tuning circuits and main filter circuits

Group No. (condition)	Corner type	Locked code of tuning circuits (pre/post sim)	Cutoff frequency of the main filter circuits (pre/post sim) /MHz
A ($T = -40$℃ $V_{\text{dd}} = 1.6$V)	Fast	00111/01000	4.993/5.051
	Slow	11011/11011	5.025 /5.010
B ($T = -40$℃ $V_{\text{dd}} = 2$V)	Fast	00111/00111	4.974 /4.974
	Slow	11011/11011	5.015 /4.998
C ($T = 95$℃ $V_{\text{dd}} = 1.6$V)	Fast	01000/01000	5.053 /5.050
	Slow	11010/11010	5.113 /5.103
D ($T = 95$℃ $V_{\text{dd}} = 2$V)	Fast	01000/01000	5.031 /5.029
	Slow	11010/11010	5.129 /5.119
E ($T = 27$℃ $V_{\text{dd}} = 1.6$V)	Fast	01000/01000	5.103/5.100
	Slow	11011/11010	5.107/4.949
F ($T = 27$℃ $V_{\text{dd}} = 2$V)	Fast	00111/01000	5.083 /5.080
	Slow	11010/11010	4.979 /4.967
G ($T = 27$℃ $V_{\text{dd}} = 1.8$V)	Fast	01000/01000	5.105 /5.103
	Slow	11011/11010	5.125 /5.111
T ($T = 27$℃ $V_{\text{dd}} = 1.8$V)	Typical	10001/10001	5.021 /5.011

8 groups of results: A, B, C, D, E, F, G and T. The 8 combinations are corresponding to different environment temperatures (−40, 27, 95℃), different source voltages (1.6, 1.8, 2V) and different process corners (Fast corner, Slow corner). Group T is the typical case without process corner consideration. Besides, we also list the pre-simulation and post-simulation results in the table. In Table 2, the data on the left of the denotation "/" is the pre-simulation data and on the right is the post-simulation data.

In all cases that considering the process, temperature and voltage source variations, the tuning circuits can tune the cutoff frequency to the range of (4.974 ~ 5.129MHz) around 5.021MHz in pre-simulation. So the tuning accuracy of tuning circuits is (−0.94% ~ +2.15%). And in post-simulation, the tuning circuits tune the cutoff frequency to (4.949 ~ 5.119MHz) around 5.011MHz, which corresponds to tuning accuracy of (−1.24% ~ +2.16%). It corresponds to (−62, 108kHz) variation which is well below the maximum tolerance of the application. In layout design, we use matching techniques described above to improve the accuracy of the tuning. Besides, we use many dummy transistors for perfect matching. Thanks to the good matching technique, the accuracy of tuning is improved comparing to pre-simulation. The waveforms of clk_rst, clk_int, clk_cmp, $V_c(t)$ and $V_{\text{cmp}}(t)$ corresponding to post-simulation are shown

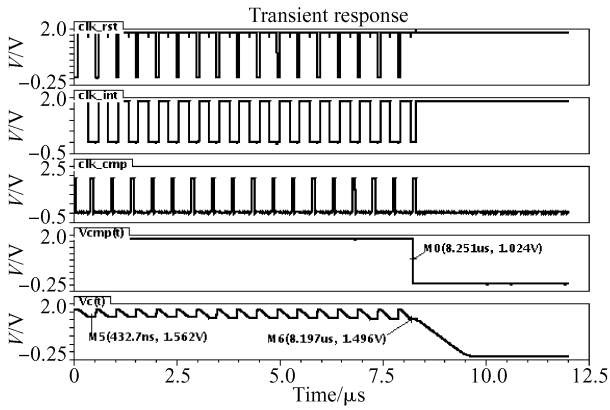


Fig. 8 Waveforms of clk_rst, clk_int, clk_cmp, $V_c(t)$ and $V_{cmp}(t)$ in tuning circuits corresponding to post simulation

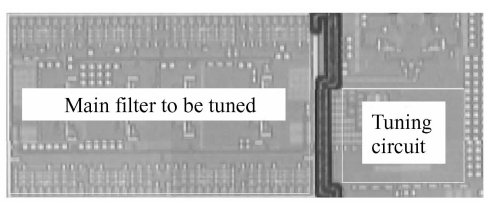


Fig. 9 Main filter and tuning circuit in chip die photo

in Fig. 8. And the in-band IIP3 of the low-pass filter in pre-simulation and post-simulation is better than 16.1dBm. The input referred noise of the filter is about $36\mu V_{rms}$.

5 Measurement results

The LPF with auto-tuning has been fabricated in 0.18μm standard CMOS technology which adopts metal insulator metal (MIM) capacitors and poly-resistors for fabricating capacitors and resistors. The filter within a GPS system has been taped out. The die photo of the filter system is shown in Fig. 9. The area of this tuning architecture is $0.047827mm^2$, only about a quarter of that of the main filter circuits. Operating with a 1.8V power supply, the total power consumption of the LPF system is 3.6mW.

The frequency response of the filter in typical case after tuning is shown in Fig. 10. The marker "2"

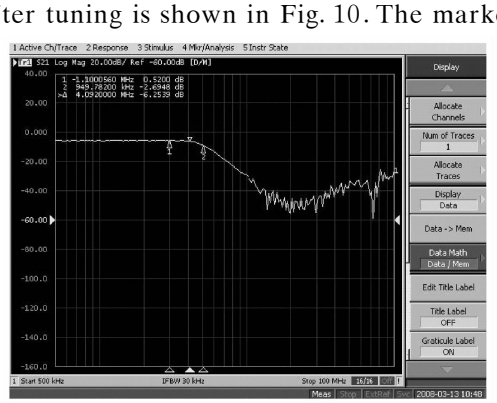


Fig. 10 Tuned frequency response of the low pass filter

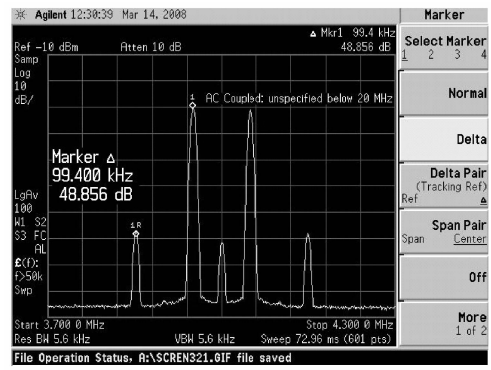


Fig. 11 Linearity of the filter and test-buffer combination

in the figure corresponding to 5.04MHz (4.09MHz + 0.95MHz) is attenuated −3.21 (0.52dB + 2.69dB) comparing with the pass-band gain, so the cutoff frequency of the low pass filter is very close to the simulation case. The attenuation at 20MHz (4fc) is about −45dB and it attenuates the interferers in the stop band well. Note that in Fig. 10 and Fig. 12 markers "1" and "2" are all relative to marker "Δ". When the temperature changes from −40 to 100℃, we choose three temperature points which is −40, 27, 100℃. The cutoff frequency corresponding to these three temperature points after tuning are 5.112, 5.012 and 4.920MHz respectively, corresponding to tuning error of (−1.84% ~ +2.00%) around 5.012MHz. And it meets the requirement well and is in good accordance with the simulation case. The crystal frequency variation is very small with variation only about tens of ppm (1/1000000), so the effect of crystal frequency variation can be ignored. The variations of unit resistors in both tuning circuits and main filter circuits are calibrated automatically through adjusting the discrete capacitor banks to keep the RC product constant. So the tuning accuracy is only limited by the discrete quantization errors of the capacitor bank when it jumps from one control word to the other. The transient response of the tuning circuit is shown in Fig. 8. The response of $V_c(T)$ shown in Fig. 8 indicates that the tuning is completed after about 10μs.

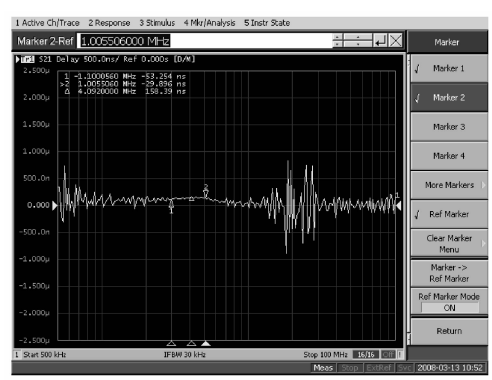


Fig. 12 Measured group delay of the main filter

Table 3　Measured performance summary of LPF

Supply voltage	1.8V
Power consumption	3.6mW
Cutoff frequency fc	5.04MHz
In-band IIP3	16.1dBm
Input referred noise	$36\mu V_{rms}$
Group delay variation from 3 to 5MHz	24ns
Attenuation@20MHz	≈ -45dB
Tuning accuracy	(−1.24%, +2.16%)
Tuning time	less than 10μs

The signal of $V_c(t)$ is the power down signal for the voltage supply in tuning circuit after $V_c(t)$ turns out to be low voltage level in which time the tuned control words are already saved in registers.

The filter is tested through a test-buffer circuit. And the linearity of the filter and test-buffer combination is measured as shown in Fig. 11. The two tones with input power of −15dBm for the IIP3 measurement are set to be 3.95 and 4.05MHz. So from Fig. 11, the IIP3 of the combination can be calculated to be 9.458dBm according to Eq. (6) [7].

$$\mathrm{IIP}_3|_{\mathrm{dBm}} = \frac{\Delta P|_{\mathrm{dBm}}}{2} + P_{\mathrm{in}}|_{\mathrm{dBm}} \tag{6}$$

The linearity of the test-buffer is 9.2dBm through simulation. So linearity of the combination is limited by the test-buffer. It is expected that the linearity of the filter alone is as good as the simulation case. After the tuning is shut down, the filter consumes only 2mA from 1.8V voltage supply.

The group delay variation is measured to be less than 24ns [(158.39 ~ 53.254ns), (158.39 ~ 29.896ns)] between 3MHz and 5MHz as shown in Fig. 12 which is much smaller than the 100ns specification. So the phase distortion is proved to be very small. The bandwidth of (3MHz, 5MHz) is of great concern because the passive poly-phase filter in front of the filter along the down conversion chain of the whole chip attenuates the out of band interferers well. The performance summary of the LPF is shown in Table 3.

6 Conclusion

This article mainly presents an LPF with accurate auto-tuning structure. The tuning structure exhibits good accuracy and matching properties. Besides, the tuning scheme is very easy to realize, in which the digital circuit needs only a wave generator and a counter. It can work automatically or by outside setting from the SPI circuit. The area of this tuning architecture is $0.047827\mathrm{mm}^2$, only about 1/4 of that of the main filter circuits, as shown in Fig. 9. And the tuning circuit will be turned off after the tuning is completed (when $V_c(T)$ turns out to be low) so its power consumption is considered near zero. After tuning is completed, the power consumption is only 2mA in measurement. So the filter with this tuning architecture is efficient both in area and power consumption.

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一种带有精准调谐结构的有源 RC 低通滤波器的设计

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摘要：提出了一种带有精准调谐结构的有源 RC 低通滤波器的设计方案，其截止频率为 5MHz，并在 0.18μm 标准 CMOS 工艺线上流片得到验证.调谐精度达到(－1.24%，+2.16%)，测试中得到验证.调谐系统所占芯片面积仅为主滤波器面积的 1/4.调谐系统完成调谐功能后会自动关闭，降低了功耗以及对主滤波器的串扰.以 50Ω 作为源阻抗，滤波器带内 3 阶交调量(IIP3)好于 16.1dBm.滤波器输入参考噪声为 36μV_{rms}.滤波器群延迟时间波动测试结果为 24ns.滤波器功耗为 3.6mW.带有这种调谐结构的滤波器容易被实现，可以用于很多无线低中频应用中，例如全球定位系统、全球通和码分多址等芯片系统中.

关键词：CMOS 电路设计；自动调谐；有源 RC 滤波器；无线系统
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