Post-Gate Process Annealing Effects of Recessed AlGaN/GaN HEMTs*

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Abstract: This paper focuses on how to reduce the gate leakage current caused by plasma dry etching. X-ray photoelectron spectroscopy (XPS) is employed to measure the AlGaN surface before and after etching. N vacancies are introduced, which cause that gate currents are not dominated by the thermal electron emission mechanism. N vacancies enhance the tunneling effect and reduce the Schottky barrier height as n-type doped in the etched AlGaN surface. A post-gate process for AlGaN/GaN HEMTs, annealing at 400°C in a nitrogen ambient for 10min is introduced. After annealing, Ni atoms of gate metal reacted with Ga atoms of AlGaN, and N vacancies were reduced. The reverse leakage decreased by three orders of magnitude, the forward turn-on voltage increased and the ideality factor reduced from 3.07 to 2.08.

Key words: GaN; dry etching; gate leakage; annealing; N vacancy

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1 Introduction

The development of AlGaN/GaN high-electron mobility transistors (HEMTs) has been largely advanced in recent years. AlGaN/GaN HEMTs have demonstrated high current levels, high breakdown voltages, and high frequency power performance due to their unique material properties. More than 250W of peak output power is achieved with newly developed X-band solid-state power amplifier^[1].

However, there are still two problems to be solved: DC-RF dispersion and high leakage current. In order to restrain DC-RF dispersion, a GaN cap layer is introduced. The GaN cap layer results in surface far away from the 2D electron gas (2DEG) channel, minimizes the impact of surface charging on device operation^[2,3]. But the recessed HEMTs will cause larger leakage current through the Schottky gates, which may cause extra noise and reliability problems^[4]. It is reported that the significant increase of the gate leakage current is due to the increasing of the roughness and appearance of N vacancies in AlGaN surface^[5].

In this paper, we introduce a post-gate process for AlGaN/GaN HEMTs, annealing at 400° C in the nitrogen ambient for 10min. The post-gate process annealing reduces the reverse leakage current, and the mechanism of reducing the damages induced by inductively coupled plasma (ICP) etching is explained. The changes of the I-V characteristics, the transfer char-

acteristics and the small signal performance are also given to display the other annealing effects.

2 Experiment

Figure 1 shows a schematic illustration of Al-GaN/GaN HEMT device structure. The AlGaN/GaN HEMT layer was grown by metal organic chemical vapour deposition (MOCVD) on SiC substrate. The heterostructure consisted of a $3\mu\text{m}$ -thick GaN buffer layer, a 110nm-thick high mobility GaN layer, a 1nm AlN layer, a 25nm undoped AlGaN layer in which the Al composition is 20%, and an undoped 1nm-thick GaN cap layer.

Source and drain ohmic electrodes were formed by evaporating Ti/Al/Ti/Au, which was then alloyed using rapid thermal annealing at 850°C for 30s. The

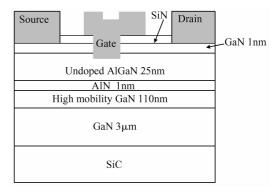


Fig. 1 Schematic illustration of the AlGaN/GaN HEMTs

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contact resistivity evaluated by transmission-line matrix measurements was $10^{-6}~\Omega~ \cdot \text{cm}^2$. Device isolation was accomplished by ICP etching. A 120nm-thick SiN was then deposited using plasma-enhanced CVD. After a gate footprint was opened through the SiN film using CHF $_3$ and SF $_6$ plasma dry etching, gate recess etching was performed using Cl $_2$ and BCl $_3$ plasma dry etching by ICP. The length of gate footprint is $1\mu\text{m}$. Then a Γ -shape gate was formed by another gate lithography. Ni/Au was used as a gate metal. The Γ -shape gate metal overlapping the SiN film played the role of field-plate.

After completing gate metallization, in order to make the metal be able to endure big current and reduce the metal resistance, the device was provided with a Ti/Au metallization and a 2.5 μ m Au-plated airbridge process to complete the AlGaN/GaN HEMTs.

Finally, these device samples were annealed at 400°C in a nitrogen ambient with time range of 10 to 20min.

3 Results and discussion

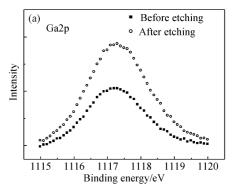
The ICP dry etching has a low etch selectivity between materials and causes subsurface damages. Figure 2 shows the X-ray photoelectron spectroscopy (XPS) Ga2p, Ga3d and N1s spectra of AlGaN surfaces before and after dry etching by Cl₂ and BCl₃.

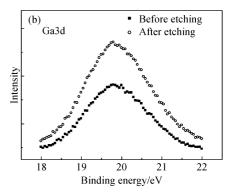
Comparing Fig. 2 (b) with Fig. 2 (c), it can be seen that before etching, the ratio of N1s/Ga3d is 1.20, but after etching, the ratio decreases to 1.03. The drop of the ratio shows that the dry etching by ICP can reduce N content in AlGaN surface and introduce N vacancies which enhance the tunneling effect as n-type dopant in the etched AlGaN surface [6].

The ICP induced damages and the associated defects lead to an increase in gate leakage current. The reverse leakage currents increase with the density of the N-vacancy defect donor, due to the enhancement of the tunneling transport process by the barrier thinning with ionization of the N-vacancy defect donor [7].

Figures 3 (a),3 (b) and 3 (c) show the typical drain current-voltage characteristics of AlGaN/GaN HEMTs devices with $120\mu m$ gate-width before and after annealing at $400\,^{\circ}\!\!\mathrm{C}$ for 10 and 20min in N_2 , respectively.

After annealing, drain saturation currents reduced compared to those before annealing. The gate bias is in the range of -5 to 2V with a step of 1V. After $10\min$ annealing, the maximum drain current at





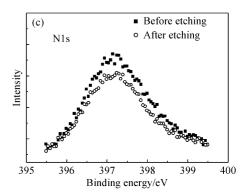
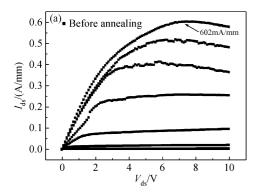


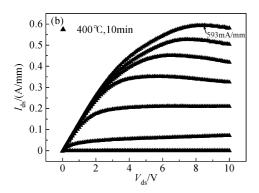
Fig. 2 XPS spectra of AlGaN before and after etching (a) Ga2p; (b) Ga3d; (c) N1s

a gate bias of 2V dropped from 602 to 593mA/mm. After 20min annealing, the maximum drain current at a gate bias of 2V decreased to 574mA/mm, due to the decrease of 2DEG concentration at the AlGaN and GaN interface. It was suggested that the diffusion of Ni atoms in the GaN layer affects the strain and surface states of the AlGaN which causes the decrease of polarization induced-charges^[8].

Figure 4 shows the typical transfer characteristics of AlGaN/GaN HEMTs devices with $120\mu m$ gatewidth before and after annealing at 400°C for 10 and 20min in N₂.

Before annealing, a maximum extrinsic transconductance (g_m) was measured 156mS/mm. It decreased to 148mS/mm at the same drain bias voltage after 10min annealing at 400°C in N_2 and decreased to 135 mS/mm after 20min annealing, because of the drain current degradation. The threshold voltage of the





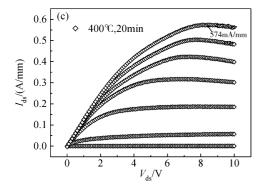


Fig. 3 I-V characteristics of HEMTs (a) Before annealing; (b) After annealing for $10\min_{i}$ (c) After annealing for $20\min_{i}$

same devices shifted from -4 to -3.9V after annealing, indicating a little change of gate modulation efficiency.

Figure 5 shows the gate current characteristics of

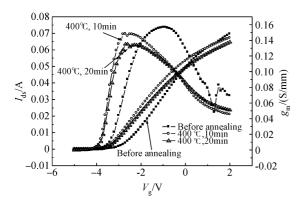


Fig. 4 Transfer characteristics of HEMTs before and after annealing

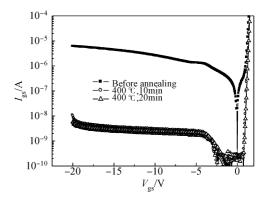


Fig. 5 Gate current characteristics of HEMTs before and after annealing

AlGaN/GaN HEMTs devices with $120\mu m$ gate-width before and after annealing at 400°C for 10 and 20min in N_2 .

Table 1 shows the reverse leakage, forward turnon voltage and ideality factor of AlGaN/GaN HEMTs devices before and after annealing at 400° C for 10 and 20min in N₂.

After annealing, the reverse leakage of the Schottky contacts both decreased by three orders of magnitude, the forward turn-on voltage increased by $0.5 \sim$ 1V and the ideality factor decreased from 3.07 to 2. 08 and 2. 17. Very large ideality factors (>3) before annealing indicates that the gate currents of fabricated AlGaN/GaN HEMTs are not dominated by the thermal electron emission mechanism but other mechanisms, such as vertical tunneling, surface barrier thinning, and trap-assisted tunneling. It is considered that the main leakage mechanism here is trap-assisted tunneling and the N vacancies induced by ICP dry etching are the main traps. After annealing, the ideality factor decreased because of the formation of Ga_4Ni_3 , Ni_3N and Ni_4N at the Ni/GaN interface during annealing. The reduction of the N vacancies is responsible for the reduction of the leakage current [9]. Ni atoms affect the strain and surface states of the AlGaN layer, which causes the barrier height increase of Schottky contacts on strained AlGaN/GaN heterostructures.

Figure 6 shows the $V_{\rm gs}$ -ln $I_{\rm gs}$ of the forward gate current. It can be seen from the low voltage that after annealing, the gate-to-source resistance is increased after annealing.

Table 1 Reverse leakage, turn-on voltage and ideality factor before and after annealing

Parameter	Before annealing	Annealing for 10min	Annealing for 20min
Reverse leakage	$-6.03 \mu A$	- 10. 76nA	- 5. 76nA
Turn-on voltage	1.4V	1.5V	1.55V
Ideality factor	3.07	2.08	2.17

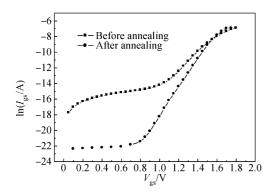


Fig. 6 $V_{\rm gs}$ -ln $I_{\rm gs}$ of the forward gate current

Considering the $I_{\rm d}$ - $V_{\rm d}$, transfer and Schottky characteristics, the optimum annealing condition is 10min annealing at 400°C in N₂. Figure 7 shows the small signal characteristics of AlGaN/GaN HEMTs before and after annealing at 400°C for 10min.

The small signal RF measurements of AlGaN/GaN HEMTs were measured using an Agilent 8510C network analyzer. Figure 7 shows the plots of the current gain $|H_{21}|$, the maximum stable power gain (MSG) and maximum available gain (MAG) versus frequency for the device.

After annealing, f_t and $f_{\rm max}$ both decreased. They can be respectively expressed as

$$\begin{split} f_{\rm t} &= \frac{g_{\rm m}}{2\pi (C_{\rm gs} + C_{\rm gd})} \\ f_{\rm max} &\cong \frac{f_{\rm t}}{2\sqrt{(R_{\rm g} + R_{\rm gs} + R_{\rm s})/R_{\rm ds} + 2\pi f_{\rm t} R_{\rm g} C_{\rm gd}}} \end{split}$$

After annealing, the gate-to-source resistance increased, $g_{\rm m}$ decreased, $C_{\rm gs}$ decreased and $C_{\rm gd}$ increased. So, the $f_{\rm t}$ and $f_{\rm max}$ both decreased.

4 Conclusion

In this paper, we focused to reduce the gate leakage current after dry etching by ICP. XPS is employed to measure the AlGaN surface before and after etching. N vacancies are introduced, so gate currents are not dominated by the thermal electron emission mechanism. N vacancies enhance the tunneling effect and reduce the Schottky barrier height as n-type doped in the etched AlGaN surface. We introduce a post-gate process for AlGaN/GaN HEMTs, annealing at 400°C in a nitrogen ambient. After annealing, Ni atoms of gate metal reacted with Ga atoms of AlGaN, and then N vacancies reduced. The reverse leak-

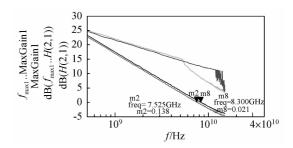


Fig. 7 Small signal characteristics of HEMTs before and after annealing

age decreased by three orders of magnitude, the forward turn-on voltage increased and the ideality factor dropped down from 3. 07 to 2. 08. Considering the $I_{\rm d}$ - $V_{\rm d}$, transfer and Schottky characteristics, the optimum annealing condition is 10min annealing at 400°C in N_2 . The small signal characteristics before and after annealing are also given. This result encourages us to apply post-process annealing technique to AlGaN/GaN HEMTs.

References

- [1] Kanto K.Satomi A.Asahi Y.et al. An X-band 250W solid-state power amplifier using GaN power HEMTs. IEEE Radio and Wireless Symposium, 2008:77
- Wang W K, Lin P C, Lin C H, et al. Performance enhancement by using the n⁺-GaN cap layer and gate recess technology on the Al-GaN-GaN HEMT fabrication. IEEE Electron Device Lett, 2005, 26(1):5
- [3] Coffie R, Buttari D, Heikman S, et al. p-capped GaN-AlGaN-GaN high-electron mobility transistors (HEMTs). IEEE Electron Device Lett, 2002, 23(10):88
- [4] Okamoto Y, Ando Y, Nakayama T, et al. High-power recessedgate AlGaN-GaN HFET with a field-modulating plate. IEEE Trans Electron Devices, 2004, 51(12):2217
- [5] Li Chengzhan, Pang Lei, Liu Xinyu, et al. Effect of plasma dry etching on recessed AlGaN/GaN HEMT gate leakage. Chinese Journal of Semiconductors, 2007, 28(11):1777
- [6] Kotani J, Hashizume T, Hasegawa H. Analysis and control of excess leakage currents in nitride-based Schottky diodes based on thin surface barrier model. J Vac Sci Technol B, 2004, 22(4): 2179
- [7] Kotani J, Kasai S, Hashizume T, et al. Lateral tunneling injection and peripheral dynamic charging in nanometerscale Schottky gates on AlGaN/GaN hetrosturucture transistors. J Vac Sci Technol B,2005;1799
- [8] Lee J. Processing and characterization of advanced AlGaN/GaN heterojunction field effect transistors. PhD Dissertation, Ohio State University, 2006;68
- [9] As D J, Potthast S, Fernandez J, et al. Mechanism of current leakage in Ni Schottky diodes on cubic GaN and Al_xGa_{1-x}N epilayers. Mater Res Soc Symp Proc, Vol. 892,0892-FF13-04.1

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凹栅槽 AlGaN/GaN HEMTs 器件退火处理效应*

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摘要:研究了如何减小等离子体干法刻蚀导致的大肖特基漏电.用 X 射线光电能谱(XPS)分析刻蚀前后的 AlGaN 表面,发现刻蚀后 AlGaN 表面出现了 N 空位,导致肖特基栅电流偏离热电子散射模型,N 空位做为一种缺陷使得肖特基结的隧穿几率增大,反向漏电增大,肖特基势垒降低.介绍了一种 AlGaN/GaN HEMTs 器件退火处理方法,优化退火条件为 $400^{\circ}C$, N_2 氛围退火 10min.退火后,栅金属中的 Ni 与 Ga 原子反应从而减少 N 空穴造成的缺陷,器件肖特基反向漏电减小三个量级,正向开启电压升高,理想因子从 3.07 降低到了 2.08.

关键词: GaN; 干法刻蚀; 栅漏电; 退火; N 空位

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