An 8～20GHz Monolithic SPDT GaAs pin Diode Switch*

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Abstract: Monolithic GaAs pin diode single pole double throw (SPDT) switches based on the fabrication technology of IMECAS are designed, fabricated, and tested. These SPDT switches achieve an insertion loss of 1.5dB, isolation of 32dB, and input and output return losses over 10dB from 8 to 20GHz. The switch design uses 2.5μm thick I-region GaAs pin diodes and a series-shunt-shunt switch topology in each arm. These performance characteristics are measured at a normal bias setting of 1.3V, which corresponds to 7mA of series diode bias current.

Key words: X/Ku-band; SPDT; switches; GaAs; pin diodes
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1 Introduction

Monolithic GaAs pin diodes have been successfully demonstrated as control elements in many monolithic microwave integrated circuits (MMICs), including attenuators/limiters[1,2], phase shifters[3], and switches[4,5]. These components are widely used in a variety of wireless RF and microwave communication circuits and systems, such as transmit/receive modules, multiplexers/de-multiplexers, canalized amplifiers, and sampling hold units.

The low on-state resistance and low off-state capacitance, coupled with the small physical size of the GaAs pin diodes, allow circuit topologies not possible with field effect transistor (FET)-based technology. Moreover, the pin diodes demonstrate a much higher cutoff frequency (900～1000GHz versus typical MESFET's 300GHz)[6]. Unlike the MESFET switches[7,8], the third-order intercept point of the pin diode switches increases with the frequency[9]. The vertical epitaxial structure of the pin diodes is expected to have power handling capability superior to that of MESFET.

This paper reports on a monolithic SPDT GaAs pin diode switch that exhibits an insertion loss of 1.5dB and isolation of 32dB, while maintaining input and output return losses greater than 10dB from 8 to 20GHz. The process and the model of GaAs pin diodes and the design and performance of the SPDT switches are discussed.

2 GaAs pin diode process and model

Diodes were manufactured on a molecular beam epitaxy (MBE) grown material provided by the Institute of Physics of the Chinese Academy of Sciences. The vertical epitaxial structure employs minimized intrinsic resistance and increased carrier injection efficiency compared to a planar structure. Diodes were fabricated on circular mesas using wet etching with $H_3PO_4 : H_2O_2 : H_2O = 2 : 3 : 30$ solution. The 12μm-radius diode shown here has a 0.4μm-thick p^+ top layer with a free hole concentration of $1\times10^{18}\sim5\times10^{19}cm^{-3}$. The p^+-layer was followed by a 2.5μm-thick intrinsic layer of $1\times10^{15}cm^{-3}$ n-type material and a 1μm, $3\times10^{18}cm^{-3}$ n^+ bottom layer. The p-type metal contact was made of Pt/Ti/Au. A Ni/Ge/Au/Ge/Ni/Au contact was then deposited on the n^+-layer. Both contacts were annealed at 375℃ for 1min at the same time. Diodes were passivated with 0.5μm Si_3N_4. Electroplating was used to implement the electrode down-leads instead of evaporation since evaporation is anisotropic and cannot cover the p^+- and i-layers step tightly, whereas the electroplating is isotropic. The diode structure is shown in Fig.1. Table 1 demonstrates the main parameters of each layer. The GaAs pin diode demonstrates a turn-on voltage of $V_{on} = 1.22V$ and a reverse breakdown voltage of $V_{BD} = -60V$.

The equivalent circuit model for the GaAs pin diodes was proposed by Institute of Microelectronics, Chinese Academy of Sciences[10], as shown in Fig.2.

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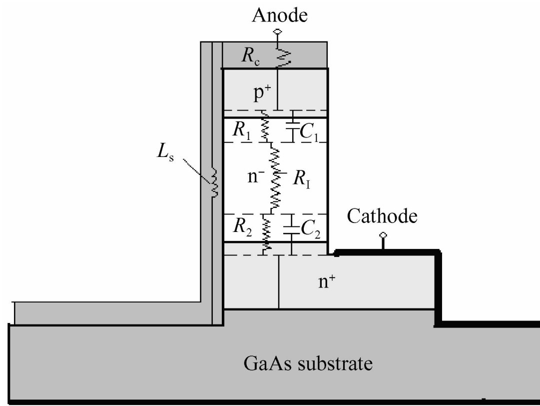

Fig.1　Cross-sectional view of the diode structure

Table 1　GaAs pin diode structure parameters

Layer	Doping /cm^{-3}	Width /μm	Radius /μm
p^+	$1\times10^{18}\sim5\times10^{19}$	0.4	12
i	1×10^{15}	2.5	12
n^+	3×10^{18}	1	80

The GaAs pin diode is divided into three parts, namely the p^+-n^- junction, the base region, and the n^--n^+ junction, and are modeled separately. The whole model of the pin diode is then formed by combining the three sub-models. In this model, R_1 is the p^+-n^- junction intrinsic resistor, C_1 is the p^+-n^- junction capacitor, R_I is the base region resistor, R_2 is the n^--n^+ junction intrinsic resistor, C_2 is the n^--n^+ junction capacitor, L_s is the parasitic inductor, and R_c is the contact resistor. The model can be simplified to a resistor in the on state and a capacitor in the off-state, as shown in Fig. 2(b). Taking advantage of this model, the value of the on-state resistance R_{on} and off-state capacitance C_{off} are extracted. The former is 1.3Ω at 7mA forward bias and the latter is 20fF at zero bias.

3　Circuit design

A single pole double throw (SPDT) switch circuit is designed with the GaAs diodes presented in section 2. Figure 3 shows the schematic of SPDT switches with a bias network. A series-shunt-shunt switch configuration is designed in each arm to minimize the through insertion loss and maximize the isolation. According to Fig. 3, the circuit "through" state (input to output1) is formed when the series diode D1 is forward biased and the shunt diodes D2 and D3 are reverse biased. Similarly, when D4 is reverse biased and D5 and D6 are forward biased, an "isolation" state (input to output2) of the circuit is formed.

The lengths of all the transmission lines are optimized for minimum insertion loss and relatively large isolation. To bias the diodes, a spiral inductor employed as an on-chip RF choke is an attractive option due to its relatively low loss. However, bias networks with quarter wavelength transmission lines are favored as a better choice for their advantages of higher modeling accuracy, which corresponds to more predictable responses. The lengths of L_5, L_6, and L_7 are calculated due to frequency range to minimize the signal leakage from bias networks. Due to their long length, especially at relatively low frequency, serpen-

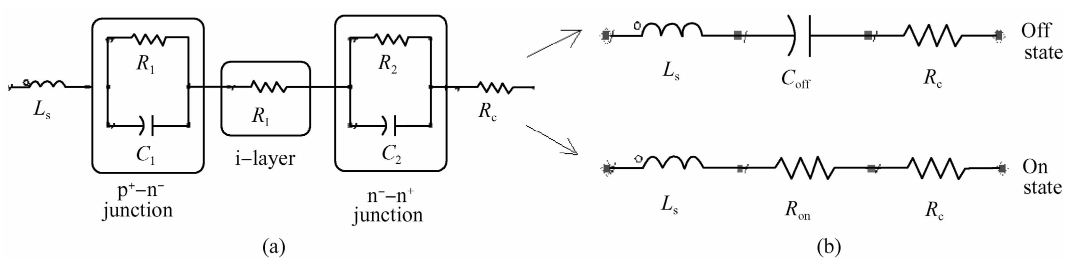

Fig.2　Equivalent circuit model of GaAs pin diodes　(a) Whole model; (b) Simplified model at on and off state

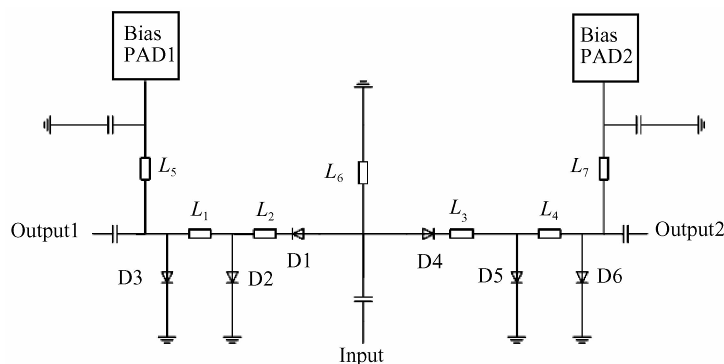

Fig.3　Schematic of the monolithic SPDT switch

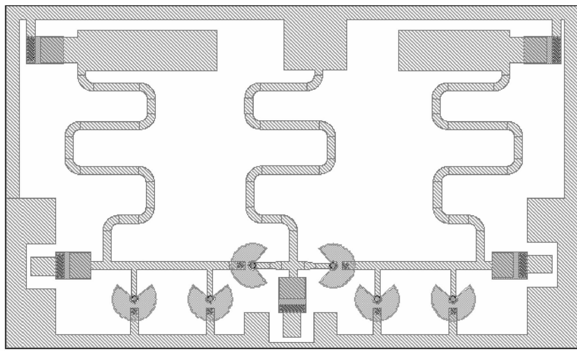

Fig. 4 Layout of the monolithic SPDT switch

tine lines are used to minimize the circuit size. It is necessary to optimize the serpentine lines to prevent electromagnetic coupling between them. The simulator of momentum is used to demonstrate the coupling effect between those serpentine lines.

4 Small signal performance

The SPDT switch circuit dimensions are 1265μm $\times$ 2105μm. The layout of the SPDT switch is shown in Fig. 4. The performance with an on-chip bias network SPDT switch was measured with bias1 of -1.3V and bias2 of 1.3V. The direct current of the series diode at the through state is 7mA.

Figure 5 shows the measured insertion loss of the through arm with bias1 of -1.3V and bias2 of 1.3V. In other words, the forward current of the through arm is only 7mA. From 8 to 20GHz, the insertion loss is less than 3.5dB, and the minimum value is 1.5dB. The return losses of both the input and output, as shown in Figs. 6 and 7, are greater than 10dB. Figure 8 shows the switch isolation is larger than 21dB, with a maximum value of 32dB. It is evident that the insertion loss of the switch will be further decreased by minimizing the off-state capacitance of GaAs pin diodes.

The power-handling capability of GaAs pin switches is evaluated on an automated on-wafer load-pull measurement system. Measurements are performed at 15GHz, at which large power signal sources are available. The $P_{0.1dB}$ is about 10dBm, as shown in Fig. 9.

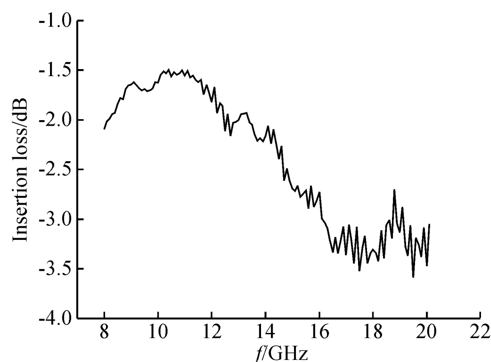

Fig. 5 Measured insertion loss from 8 to 20GHz of SPDT GaAs pin diode switches

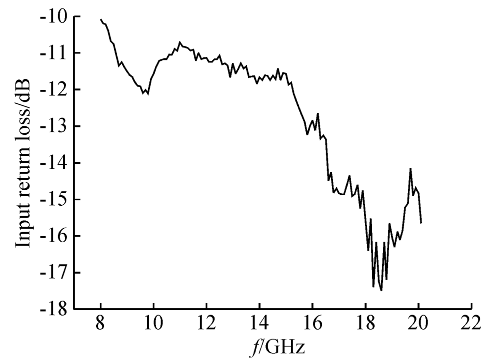

Fig. 6 Measured input return loss from 8 to 20GHz of SPDT GaAs pin diode switches

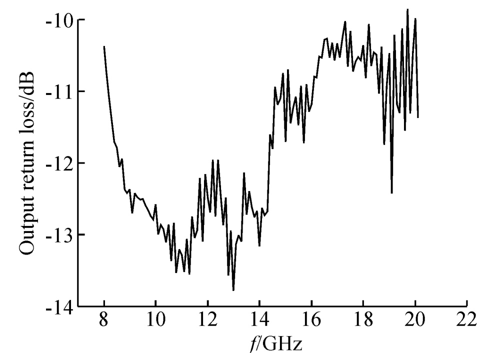

Fig. 7 Measured output return loss from 8 to 20GHz of SPDT GaAs pin diode switches

5 Conclusion

This paper reports a monolithic SPDT switch based on the fabrication technology of GaAs pin diodes from Institute of Microelectronics, Chinese Academy of Sciences, To simulate the SPDT switch, an accurate small signal model of GaAs pin diodes is developed. From 8 to 20GHz, the insertion loss of the

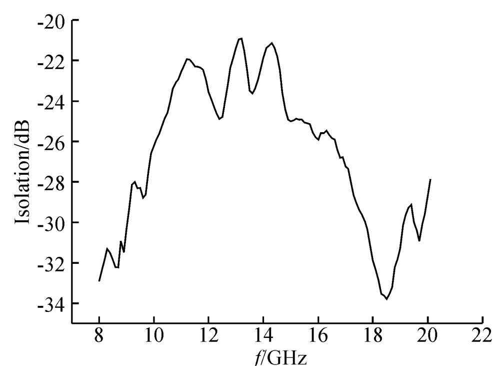

Fig. 8 Measured isolation from 8 to 20GHz of SPDT GaAs pin diode switches

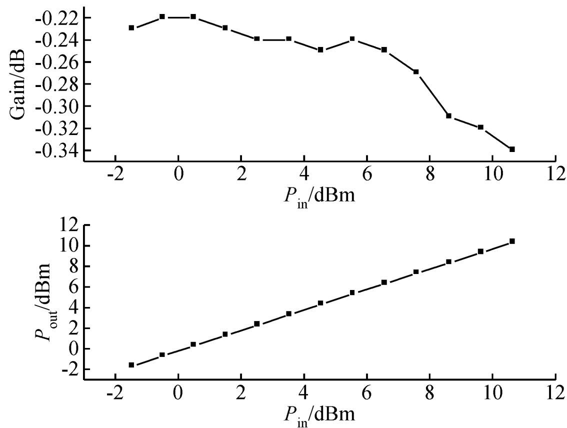

Fig. 9　$P_{0.1dB}$ of GaAs pin SPDT switches

SPDT switch is less than 3.5dB and the return loss is greater than 10dB while the isolation is larger than 21dB. The power consumption is only 9mW and $P_{0.1dB}$ is about 10dBm.

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8～20GHz GaAs pin 二极管单片单刀双掷开关*

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摘要： 基于中国科学院微电子研究所的 GaAs pin 二极管工艺，设计、制作并测试了一种单片单刀双掷开关. 在 8～20GHz 频段内，开关正向导通时的插入损耗最小值为 1.5dB，输入和输出端的回波损耗大于 10dB；开关关断状态的隔离度最大值为 32dB. 开关的支路采用串联-并联-并联的结构，其中的 GaAs pin 二极管基区厚为 2.5μm. 在 1.3V 的偏置电压下，正向导通的串联二极管工作电流为 7mA.

关键词： X/Ku 波段；单刀双掷；开关；GaAs；pin 二极管

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