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A 2GHz Power Amplifier Realized in IBM SiGe BiCMOS Technology 5PAe

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Abstract: A 2GHz power amplifier realized in IBM 5PAe 0.35μm SiGe BiCMOS technology is reported. This amplifier was implemented in a two-stage single-ended structure. All components except choking inductors were integrated on-chip. Full-frequency stability was achieved using serial resistors between the bases of the transistors and matching inductors. The off-chip test proved the stability under all the supplied voltages. At $V_C = 3.5V$, $V_B = 6V$, the small signal gain was 20.8dB, the input and output reflectance was less than −17 and −16dB, respectively, and the $P_{out\text{-}2dB}$ was about 24dBm. At the output power of 25.1dBm, the PAE was about 21.5%, and the second and third harmonics were less than −45 and −52dBc, respectively. This insures the linearity of the circuits.

Key words: power amplifier; silicon germanium; BiCMOS; heterojunction bipolar transistor
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1 Introduction

The PA (power amplifier) is one of the key components in wireless communication systems. Up to now, PAs working in RF (radio frequency) band have mostly realized in expensive technologies, such as GaAs. Compared with GaAs technology, SiGe BiCMOS technology has become more attractive for RF PA design owing to ultra-high f_T and f_{max}, high current gain, high breakdown voltage, and good thermal conductivity of the substrate. Moreover, due to its full compatibility with standard silicon processes, SiGe BiCMOS technology enables IC designers to easily integrate PAs with other modules to realize real single-chip RF transceivers, resulting in better chip performance and lower system costs[1~5].

The operating mode of the PA is determined by the signal type to be amplified. For a non-constancy envelope modulation in WCDMA systems, PAs of class A or class AB are widely used owing to their good linearity and simple structure in spite of their poor efficiency. The problem is how to obtain the optimum resistance R_{opt} in the PA design, because the largest output power can be achieved only when R_{opt} is obtained, and then the output matching network can be fixed. The classical method to obtain R_{opt} is using the load-pull technique with a load-pull system. If there is no such system, the simple calculation introduced by Cripps is substituted[6].

In this paper, a 2GHz PA realized in IBM 5PAe 0.35μm SiGe BiCMOS technology is reported. According to the off-chip test results, the circuit can work stably under all supply voltages. Under the condition of $V_C = 3.5V$, $V_B = 6V$, and $f = 2.0GHz$, the circuit has a small signal gain of 20.8dB, and the input and output reflectance are −17.2 and −16.4dB, respectively, indicating good input and output matching. The output power $P_{out\text{-}2dB}$ is about 24dBm. When the circuit delivers a power of 25.1dBm, the 2nd and 3rd harmonics are −45.1 and −52.1dBc, respectively. Although some parameter deviations exist between the simulation and the test results, and the process models should be improved, the technology proves to be effective for PA design. It is also proven that for RF PA application, the conventional GaAs technology can be replaced by SiGe technology.

2 Technology description

The 0.35μm SiGe BiCMOS technology 5PAe was introduced by IBM in 2007 as a developmental technology for PA design. Now, it is in a trial period of small scope for further evaluation. It was improved on the base of 0.5μm SiGe BiCMOS 5HP/AM/DM/PA technology. In the new technology, HB npn transistors and via holes through substrate to the back side were introduced.

The 5PAe technology provides rich types of components for PA design, including the HB npn transistor with $f_T = 25GHz$, $BV_{ceo} = 7.5V$, and $\beta > 130$; the polyresistor, n^+ diffusion resistor, p^+ diffusion resistor, PE poly resistor, NS resistor, siliced resistor, L1 TaN BEOL resistor, thick oxide MOS, single MIM and

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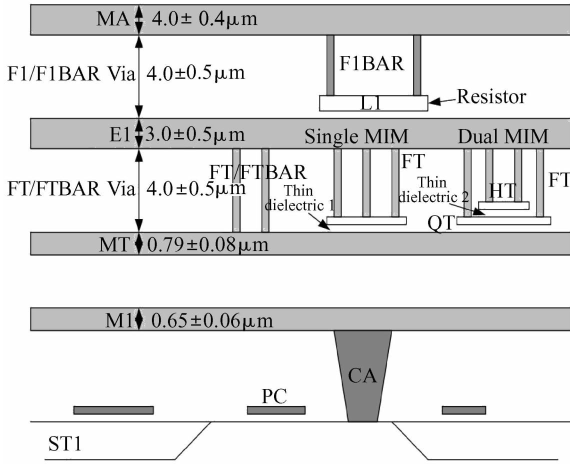

Fig. 1 Sketch map of metal levels, L1 resistor, high density metal to metal (MIM) capacitor, and dual MIM capacitor (not drawn to scale)

double MIM capacitors, single metal layer and double metal layer inductors, via holes, diodes, and so on.

The technology has 4 metal layers, as shown in Fig. 1. The thicknesses and materials are M1 (0.65 ± 0.06μm, Cu), MT (0.79 ± 0.08μm, Al), E1 (3.0 ± 0.5μm, Cu), and MA (4.0 ± 0.4μm, Al), respectively. The rich metal layers are convenient and flexible. This technology appends an L1 resistor with low parasitic capacitance between MA and E1, a high density and double MIM capacitance whose model has four types of backboard selection, with the schema shown in Fig. 1. This makes the simulation results closer to the situation of the real layout.

In the trial technology, the HB transistor has only one component model and layout with a fixed size of $3 \times 20\mu m \times 0.8\mu m = 48\mu m^2$, and the collector current density is $0.23mA/\mu m^2$ at the peak value f_T ($V_{cb} = 3V$).

3 Circuit design

The structure and operating state of a PA are determined by the requirements of practical application. Generally, the single-ended topology is most popular. For the application of non-constant envelope, where a linear PA is needed to reduce the envelope distortion, a class-A or class-AB PA is usually adopted. The stage number is usually determined by the output power and gain of the amplifier. Most PAs need two or three stages. In this design, a two-stage configuration was adopted. Figure 2 shows the schematic of the PA.

In Fig. 2, HBT_1 consists of 12 single transistors, while HBT_2 consists of 48 transistors. The emitter areas of HBT_1 and HBT_2 are 576 and $2304\mu m^2$, respectively. Considering the current capacity, the collector choke inductances are realized off-chip while all other components are integrated on-chip.

The design of the matching networks of the PA is critical because they affect not only the reflection but also the effective output power. The matching networks of a two-stage PA include the input, the intermediate, and the output stage. In order to achieve the maximal output power, the output matching network must be designed correctly in order to realize the maximal power transmission. Generally, when the optimum load impedance Z_{opt} of the transistor is obtained, the circuit has the largest output power and power matching can be achieved. We obtain Z_{opt} by exploiting the load pull technique, which relies on a special system not owned by all designers. Without the system, a brief calculation with Cripps's method is adopted to obtain the real part R_{opt} of Z_{opt}, usually[6].

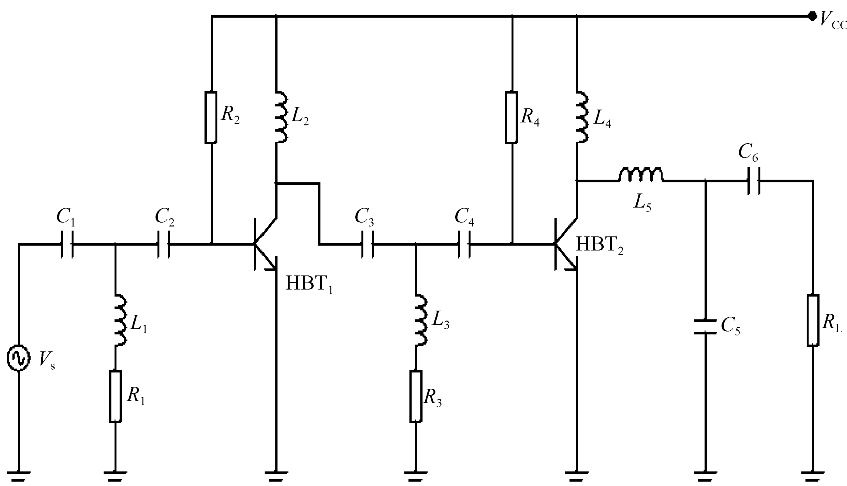

Fig. 2 Schematic of the PA

$$R_{opt} = \frac{V_{CC}}{I_{fund}} \tag{1}$$

$$P_{opt} = \frac{V_{CC} I_{fund}}{2} \tag{2}$$

where V_{CC} is the power supply, I_{fund} is the fundamental component of the collector current, which is equal to the DC current I_{DC} in case of class-A, and P_{opt} is the optimum output power, which is the object output power in general.

Combining Eqs. (1) and (2) and considering the saturation voltage V_{CEsat}, R_{opt} can be given as:

$$R_{opt} = \frac{(V_{CC} - V_{CEsat})^2}{2P_{opt}} \tag{3}$$

In practice, any collector choke inductor is not ideal. There is always a little resistance R_{RFC}, resulting in a voltage drop that makes the practical result less than that of the calculation. Thus, we can modify Eq. (3) as:

$$R_{opt} = \frac{(V_{CC} - V_{CEsat} - R_{RFC} I_{DCmax})^2}{2P_{opt}} \tag{4}$$

Based on the above equations, we can calculate, re-adjust, and optimize R_{opt} in conjunction with the simulation. Then, we can get Z_{opt}, and decide the output matching network. There are many structures for matching networks. In this design, a T-type structure is selected to achieve a near match for the resistance values. Based on the simulation and comparison, the output matching with serial inductors can reject the harmonics output effectively. The intermediate matching network is similar to that at the output. For the input matching, the traditional conjugate matching method is used.

The stability of the amplifier (that is, the rejection for oscillation) should be considered especially for PA design. Generally, the stability of the amplifier is related with the S-parameters of the transistors, the matching networks, and other factors. A two-port network may oscillate when the input or output port produces a negative resistance. In order to guarantee the stability over the whole frequency band, it is necessary to assure that each stage is stable in the frequency band. An effective method to achieve stability is to insert a serial resistor in the base of the transistor or in the negative feedback branch from the collector to the base of the transistor. A serial resistor in the base of the transistor not only can achieve alternating stability, but also can prevent the transistor damage caused by current worsening and improve thermal stability. So this method is exploited in this design[7]. The higher the value of the serial resistor, the more stable the circuit is, but with a decrease in gain. So, it is necessary to make a trade-off. In this design, a proper serial resistor was selected. The serial resistors R_1 and

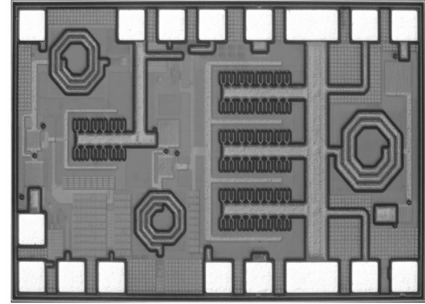

Fig. 3　Chip photo of power amplifier

R_3 with a small value were inserted between the input stage and inter-stage match inductance to assure further stability.

The circuit simulation is executed with Cadence's Specter®. The layout photo is shown in Fig. 3, and the chip area is only 1.55mm × 0.95mm.

4　Test results

Bonding test was used. Figure 4 shows the bonded test base.

The test was executed in the chip test laboratory of the Institute of RF- & OE-ICs in Southeast University. The testing equipment includes a DC power supply 66309D, a network analyzer E5071B (300kHz ~ 8.5GHz), a signal generator E4438C (250kHz ~ 6.0GHz), and a spectrum analyzer E4440A (3Hz ~ 26.5GHz), which are all Agilent products.

The DC test was made first. At $V_B = 6V$ and $V_C = 3.5V$, I_{C1} and I_{C2} were 88.2 and 325.2mA, respectively. As a comparison, the simulation results showed that I_{C1} and I_{C2} were 83.9 and 331.8mA, respectively, but at $V_B = 3V$ and $V_C = 3.5V$. The test results show that the values of the serial resistors R_2 and R_4 may be the same as that in simulation. The result indicates that the β of the transistor in practice is only about half of that in the simulation model. Thus, the tested amplifier gain decreased about 3dB.

Figure 5 shows the experimental and simulated results of the small signal S-parameters.

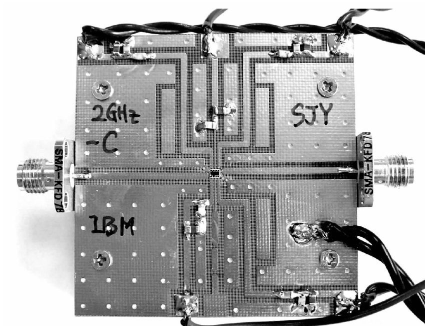

Fig. 4　Photo of bonded test base

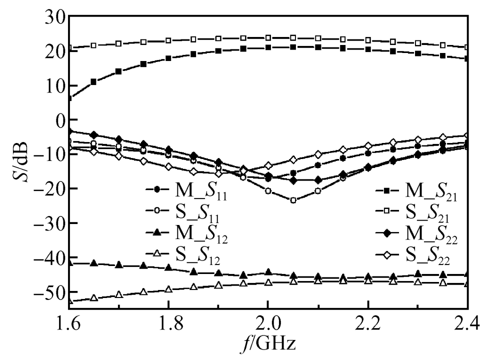

Fig. 5 Experimental and simulated results of the small signal S-parameters

Figure 6 shows the experimental and simulated results of the output power and harmonics.

The experimental results indicate that: under the condition $V_C = 3.5V$, $V_B = 6V$, and $f = 2.0GHz$, the circuit has a gain close to 21dB; the input and output reflectance are −17.2 and −16.4dB, respectively, indicating that the circuit has good input and output matching. The experimental output power $P_{out\text{-}2dB}$ was about 24dBm. At the output power of 25.1dBm, the PAE is about 21.5% and the 2nd and 3rd harmonics are less than −45 and −52dBc, respectively, indicating that the circuit has good linearity.

5 Conclusion and analysis

In this paper, a 2GHz PA was designed and fabricated in SiGe BiCMOS trial technology 5PAe introduced by IBM. A two-stage single-ended circuit structure was adopted. Excluding collector choke inductors, all the other components were integrated on-chip. The circuit simulation was executed with Cadence's Specter®. The Z_{opt} demanded for each stage was estimated with Cripps's method to achieve the optimum matching. By inserting serial resistors between transistor bases and matching inductors, full-band stability was achieved. The off-chip test results indicated that the circuit can work stably under all supply voltages. Under the condition $V_C = 3.5V$, $V_B = 6V$, and $f = 2.0GHz$, the circuit had a small gain of 20.8dB, and the input and output reflectance were less than −17 and −16dB, respectively, indicating good input and output matching. The tested output power $P_{out\text{-}2dB}$ was about 24dBm. When the circuit delivered a power of 25.1dBm, the PAE was about 21.5%, and the 2nd and 3rd harmonics were −45.1 and −52.1dBc, respectively, indicating that the circuit has good linearity. The designed PA achieves better performance than the previous work in Ref. [5] in terms of output power, PAE, and so on under equivalent conditions. The deviation between the experimental and simulated results indicates that the process models need to be improved. The tested and simulated output power has good consistency, proving the feasibility of the technology in the design of PAs.

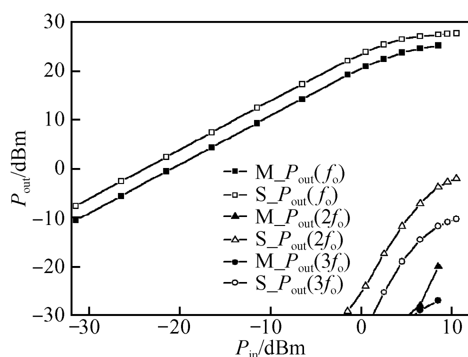

Fig. 6 Experimental and simulated results of the output power and harmonics

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References

[1] Joseph A, Liu Q, Hodge W, et al. A 0.35μm SiGe BiCMOS technology for power amplifier applications. IEEE Bipolar/BiCMOS Circuits and Technology Meeting, 2007: 198

[2] Kitlinski K, Donig G, Kapfelsperger B, et al. Si-Ge power amplifier for WCDMA handheld applications. 15th International Conference on Micnowave, Radar and Wireless Communication, 2004, 1: 363

[3] Carrara F, Scuderi A, Bottiglieri G, et al. Silicon bipolar linear power amplifier for WCDMA mobile applications. IEEE International Symposium on Circuits and Systems, 2005, 3: 2679

[4] Rippke I, Duster J, Kornegay K. A fully integrated, single-chip handset power amplifier in SiGe BiCMOS for W-CDMA applications. Radio Frequency Integrated Circuits Symposium, 2003: 667

[5] Wang A, Gua X, Feng H, et al. A 2.4GHz fully integrated class-A power amplifier in 0.35μm SiGe BiCMOS technology. 6th International Conference on ASIC, 2005: 360

[6] Cripps S. RF power amplifiers for wireless communications. Norwood, MA, Artech House, 1999

[7] Brown S A, Carroll J M. Compact, 1 watt, power amplifier MMICs for K-band applications. Gallium Arsenide Integrated Circuit Symposium, 2000: 223

基于 IBM SiGe BiCMOS 工艺 5PAe 的 2GHz 功率放大器设计

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摘要： 采用 IBM 公司刚刚推出试用的 0.35μm SiGe BiCMOS 开发性工艺 5PAe 设计并实现了一个 2GHz 功率放大器.该放大器采用两级单端结构，除集电极扼流电感外，其余元件全部片上实现，具有集成度高、结构简单的特点.通过在管子基极和匹配电感中串联电阻，实现了全频段稳定.键合测试表明，在所有电源电压下电路均能稳定工作.在 $V_C = 3.5V$，$V_B = 6V$，$f = 2.0GHz$ 时，小信号增益为 20.8dB，输入输出反射系数分别小于 −17 和 −16dB，$P_{out\text{-}2dB}$ 约为 24dBm.而在输出功率为 25.1dBm 时，功率附加效率达到 21.5%，二次和三次谐波分别小于 −45 和 −52dBc，因而具有较好的线性度.

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