A 3GHz Low-Power and Low-Phase-Noise LC VCO with a Self-Biasing Current Source *

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Abstract: A fully integrated 3GHz low-power and low-phase-noise voltage-controlled oscillator (VCO) with a self-biasing current source was implemented in a standard 0.18μm CMOS process. A trade-off between noise and power was realized through the optimization of the improved current source. The VCO can be tuned from 2.83 to 3.25GHz with a 13.8% tuning range. The measured phase noise at 1MHz offset is −111dBc/Hz at a frequency of 3.22GHz while the core circuit draws less than 2mA from a 1.8V supply voltage. These results make the circuit suitable for a 5GHz wireless local area network (WLAN) receiver and 3.4 to 3.6GHz world interoperability for microwave access (WiMAX) application.

Key words: 3GHz LC VCO; phase noise; self-biasing current source; CMOS
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1　Introduction

The VCO is an essential building block in modern communication systems. Being the heart of the frequency synthesizer, the VCO plays an indispensable role in RF transceivers. For systems with high dynamic range requirements, the VCO must achieve a correspondingly high degree of spectral purity. With the rapid development of CMOS technology and large demand for wireless communication, low cost and low power consumption are the most significant considerations for circuit design. In any integrated wireless transceiver systems, the frequency synthesizer usually consumes the most power, excluding the PA. To achieve low power and low phase noise, the VCO, as the core of the synthesizer, should be properly designed[1,2]. However, it is a great challenge to design a high-performance VCO in a low-power application. Because traditional oscillators generally work in the current-limited region, there is a strong relationship between the phase noise and the current: a drop in the core current will result in the deterioration of the phase noise by 20dB/dec[1,2].

So far, a number of methods to improve the phase noise have been proposed. In Ref. [3], by using a filtering technology, a tail current noise reduction lowered the phase noise, but the shortcomings of this method was to use an extra inductor and capacitor to form a passive LC filter, resulting in increased chip area and cost. In Ref. [4], removing the bias current source improved the phase noise, but it was problematic due to increased sensitivity to power supply noise. The contribution of the current source, however, dominates other sources of phase noise, like the tank resistance and the differential pair FETs. It is feasible to greatly improve the phase noise performance by optimizing the sizes of the current source transistors, which is the focus of our work.

In this paper, we present a completely integrated 3GHz current-biased differential VCO in a 0.18μm process. Through the optimization of an improved self-biasing current source, we achieve low power consumption, low phase noise performance, and small chip area without any off-chip components, reducing the complexity and the costs.

2　Circuit design

It is difficult to realize a widely tuned VCO with a trade-off between low phase noise and low power consumption. Here we adopt a proper VCO topology and apply an improved self-biasing current source to reduce phase noise and power, both of which will be introduced below.

2.1　LC VCO

The VCO core is based on conventional cross-coupled negative-G_m topology, as shown in Fig. 1.
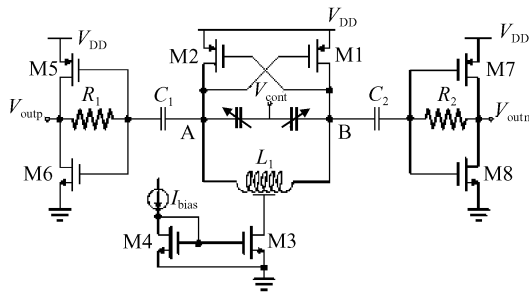
To reduce the phase noise, we designed an LC

Fig.1   Simplified schematic of the VCO

tank with high Q, composed of a symmetric spiral inductor with center-tap and an accumulation-mode MOS (A-MOS) varactor. The selection of on-chip inductors is crucial to the design of low-phase-noise VCOs. In our design, an inductor library of widespread values and different qualities was provided by the foundry. Figure 2 shows the inductor values, qualities, and turns at the operating frequency of around 3GHz. From the chart, we choose a proper inductor for our design. In addition, we use two cross-coupled pMOS transistors M1 and M2 to generate the negative impedance required to cancel the losses of the LC tank, which reduce phase noise, for the pMOS transistors to attain a lower close-in noise than the nMOS transistors[5,6]. Finally, a structure of improved current source is also adopted to lower the phase noise, which will be described in the following section.

To reduce the power consumption, we limit the current to less than 2mA and keep the VCO working in the current-limited region. To get a large frequency tuning range, we adopt an accumulation-mode MOS (A-MOS) varactor of moderate value.

In order to drive 50Ω, we have adopted a self-biased inverter-type buffer amplifier, as shown in Fig.1[7]. By careful design, the effect of the buffer amplifiers on the phase noise can be diminished.

2.2 Self-biasing current source
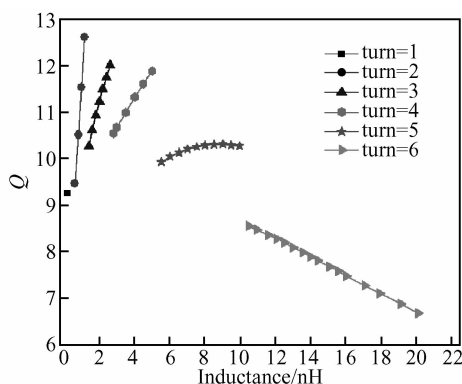
The current of the LC tank is provided by the

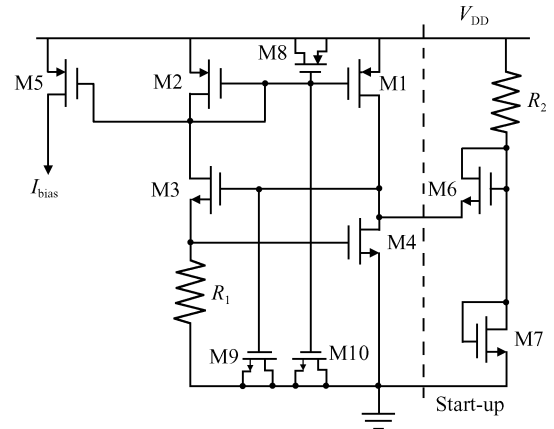Fig.2   Relationship between inductance, qualities and turns at 3GHz

Fig.3   Schematic of the self-biasing current source

improved self-biasing current source shown in Fig.3. On the right side of the chart is a startup circuit employed to avoid I_{bias} being zero. I_{bias} variation is lower than 1% for voltage supply variations of 10%[8]. This technology is known as the V_T reference, also called the bootstrap reference[9]. By adjusting the resistor R_1 in Fig.3, a suitable current for the VCO core module can be supplied.

The noise contribution of the current source can affect the VCO's phase noise significantly through up-conversion. The degradation in phase noise due to bias noise is shown to be a function of MOS device sizing. By exploiting this dependency, bias noise contributions to phase noise can be minimized by design rather than through filtering. The smaller the product of the current source transconductance and the tank resistance, the smaller the contribution of the current source to the oscillator noise factor F. So, we can reduce the current source device transconductance as a more viable alternative. For a current source device with a larger W/L, the overdrive is smaller and therefore, the lowest "available" phase noise is lower than that with a larger W/L. In addition, a larger current source transistor reduces the device flicker noise, which is inversely proportional to the transistor[1,2].

By optimizing the proportion among the dimensions of M5, M2, and M1, and adding two poles with M8, M9, and M10 to filter out any noise from the reference circuit, we can achieve a great improvement in phase noise performance. This circuit itself has lower current consumption, less than $200\mu A$.

3   Experimental results

The VCO was fabricated in a commercial $0.18\mu m$ CMOS process. The measurement is performed on an FR-4 PCB test fixture. An HP8591 spectrum analyzer is used to measure the spectral density of the proposed VCO. The measured spectral densities give the funda-
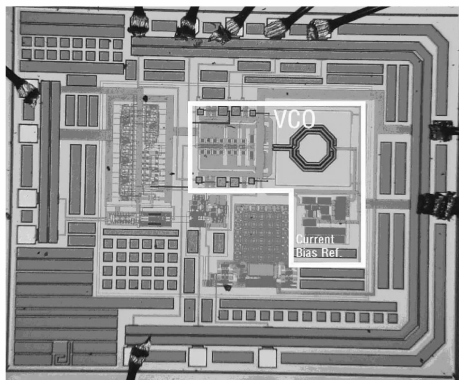
Fig. 4　Chip photograph of the LC tank VCO

Fig. 6　Tuning characteristics of the 3. 22GHz VCO

mental frequency of 3. 22GHz and the output power is around −12dBm.

　　Figure 4 shows the microphotograph of the fabricated chip. All pads are ESD protected and the on-chip inductors are implemented with top metal to get a higher Q. Figure 5 shows the output spectrum at 3. 22GHz,with −12dBm output power for the circuit with the operated tail current of 2mA.

　　From the delta-mode marker in Fig. 5,we get a phase noise of about −111dBc/Hz at 1MHz offset from the following equation：

$$L(f_{offset}) = 10\lg\frac{P_{SSB}}{P_S} = P_m + C_m - 10\lg\frac{B_m}{1Hz} - P_S \tag{1}$$

where $L(f_{offset})$ is the phase noise at offset frequency f_{offset} from the carrier (in dBc/Hz),B_m is the measurement bandwidth (in Hz),C_m is the calibration coefficient of the testing system (about 2~3dB),P_m is the noise power in measurement bandwidth (in dBm), and P_S is the signal power (in dBm)[10].

　　Figure 6 shows the simulation results of the schematic circuits (150MHz higher than that through Assura to extract parasitic resistors and capacitors) and experimental results. The figure indicates that the test results are around 150MHz lower than the simulation results.

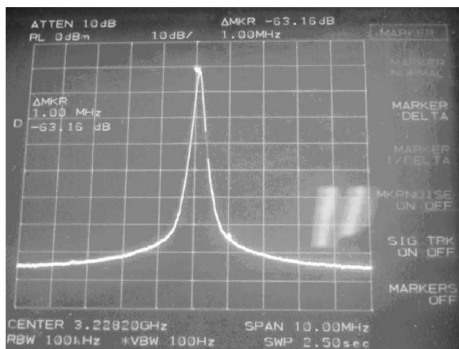　　A widely used figure of merit (FOM) to compare VCOs is defined as

$$FOM = \left(\frac{f_o}{\Delta f}\right)^2 \times \frac{1}{L(\Delta f)P} \tag{2}$$

where $L(\Delta f)$ is the SSB phase noise measured at Δf offset from f_o carrier frequency and P is the DC power consumption in mW.

　　Table 1 summarizes the measured performance of the designed 3GHz CMOS VCO with self-biasing current source. Table 2 shows a performance comparison with recent works using the FOM calculation expressed by Eq. (2).

4　Conclusion

　　A monolithic low-power and low-phase-noise VCO based on a symmetric spiral inductor with center-tap and A-MOS varactors was implemented in a 0. 18μm CMOS process with six metal layers. The optimization of the improved current source allows a trade-off between noise and power. The fabricated

Table 1　Measurement performances summary of the CMOS VCO

Frequency range	2. 83 to 3. 25GHz(13. 8% tuning range)
Phase noise (PN)	−111dBc/Hz @ 1MHz offset
Supply voltage	1.8V
Current consumption	2mA (output buffer de-embedded)
Figure-of-merit (FOM)	−175. 6dB
Chip area	590×300(VCO core) + 163×175 (Current Ref.) μm²(excluding pads)
Technology	0. 18μm CMOS

Table 2　Comparison with recently published VCOs

Reference	Tech /μm	Power diss /mW (output buffer de-embedded)	$(\Delta f/f_o)$ /(M/GHz)	Phase-noise /(dBc/Hz)	FOM /(dBc/Hz)
This work	CMOS 0.18	3.6	1/3.228	−111	−175.6
Ref.[11]	CMOS 0.18	12.6~26.28	1/3.17	−111~−102	−170
Ref.[12]	CMOS 0.18	12	1/3.2	−101	−160.3
Ref.[13]	CMOS 0.25	13.2	1/3.031	−118	−176.4
Ref.[14]	CMOS 0.18	3.6	1/3.05	−111.4	−173.8
Ref.[15]	CMOS 0.18	18	1/3	−119	−176

Fig. 5　Output spectrum of the VCO at 3. 22GHz

VCO operates between 2.83 and 3.25GHz，corresponding to a 13% tuning range，at a 1.8V supply voltage and less than 2mA supply current for the VCO's core circuit. Phase-noise measurements show a phase-noise of －111dBc/Hz at 1MHz from the 3.22GHz carrier.

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3GHz 低功耗低相位噪声的带自偏置电流源的 LC 压控振荡器*

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摘要：利用 0.18μm CMOS 工艺实现了一个全集成的工作于 3GHz 的低功耗、低相位噪声的压控振荡器，且带有自偏置电流源. 通过对改进的电流源进行优化，在噪声与功耗之间达到了折中. 该压控振荡器可工作于 2.83 至 3.25GHz 频段内，调谐范围达到 13.8%. 当工作于 3.22GHz 时，测得的相位噪声在 1MHz 频偏处为 －111dBc/Hz. 在 1.8V 电源电压下，核心模块消耗电流小于 2mA. 表明该电路适合 5GHz 的无线局域网接收机以及 3.4 至 3.6GHz 的全球微波互联接入(WiMAX)应用.

关键词：3GHz LC 压控振荡器；相位噪声；自偏置电流源；互补-MOS 型集成电路
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