A PWM/Pseudo-PFM Auto-Mode-Applied Buck DC/DC Switching Regulator*

Liu Lianxi†, Yang Yintang, and Zhu Zhangming

(*Key Laboratory of Wide Band-Gap Semiconductor Materials and Devices of the Ministry of Education, Institute of Microelectronics, Xidian University, Xi'an 710071, China*)

Abstract: A buck DC/DC switching regulator is implemented by automatically altering the modulation mode according to the load current that ranges from 0.01 to 3A. The pseudo-PFM mode is applied when duty cycle is less than 20%, and the PWM mode is selected in a range of duty cycle from 20% to 100%. The average conversion efficiency of the regulator is about 90% when the output current varies. The proposed dual-mode-control die is implemented in a 0.5μm DPDM CMOS mixed-signal process and a power p-MOSFET is used in the chip by hybrid integration.

Key words: pulse-width-modulation; pseudo-pulse-frequency-modulation; duty cycle; hybrid integrated
EEACC: 2570; 1280
CLC number: TN402 **Document code**: A **Article ID**: 0253-4177(2008)10-1956-07

1 Introduction

More portable applications like adapters of notebook PC, PDA, etc, need a wide supply current range. On the one hand, a large supply current can change the battery quickly, and on the other hand, little current is needed at the pre-charge or the end of the charge for security. So integrated switching power supplies with multimode control are gaining popularity in state-of-the-art portable applications because of their ability to adapt to various loading conditions and therefore achieve high efficiency over a wide load-current range.

Maintaining high efficiency over a wide load range is critical in determining power-savings because portable devices mostly idle and remain at light loads, but high-performance and high power events have a significant toll on the battery. Unfortunately, when a switching converter designed for high efficiency at a particular peak power level operates under medium-to-light load conditions, its efficiency and therefore battery life performance degrades. Fixed-frequency, pulse width modulated (PWM) supplies suffer from this effect because switching losses constitute a major portion of the total power loss when lightly loaded. The key to achieve high efficiency under moderate-to-light loading conditions is to reduce the load independent power losses, most dominant of which are the switching losses[1,2]. A lower switching frequency in PWM mode reduces switching losses, but results in a higher peak current flowing through the power inductor and power transistors, thereby not only incurring higher conduction losses but also increasing their respective current ratings and die size requirements, that is, increasing cost.

Pulse-frequency modulation (PFM) control in discontinuous-conduction mode (DCM)[3] is an attractive alternative for light-to-moderate loads because of lower switching frequencies and therefore reduced switching losses. PFM may be implemented in various forms. For any of these approaches to generate the pulses, the pulse position can be solved iteratively to determine the beginning and the end of each pulse cycle[4]. Obtaining the pulse position data in this manner requires a lengthy numerical calculation. Alternatively, calculation time can be reduced if the frequency is assumed to be fixed at the value at the beginning of a pulse period. In this case, the pulse positions are not found exactly, but the reduction in calculation time may be useful in some PFM applications[5,6]. This manner of pulse position calculation is referred to as "approximate PFM" or "pseudo-PFM".

A PWM/PDM dual mode controlled multi resonant high-frequency inverter constructed by discrete devices is proposed in Ref. [7]. However, this is only an output stage without control circuits, and is hard to integrate in a package. A PWM/PFM dual mode controlled DC-DC converter was introduced in 2007[8]. Though this converter can switch control-mode according load current to get high efficiency, its output driving current range is too small (from 3 to 300mA),

* Project supported by the National Natural Science Foundation of China (Nos. 60676009, 60776034), the Doctor Foundation of Ministry of Education (No. 20050701015), and the National Outstanding Young Scientist Foundation of China (No. 60725415)
† Corresponding author. Email: lxliu@mail.xidian.edu.cn
Received 9 May 2008, revised manuscript received 19 June 2008

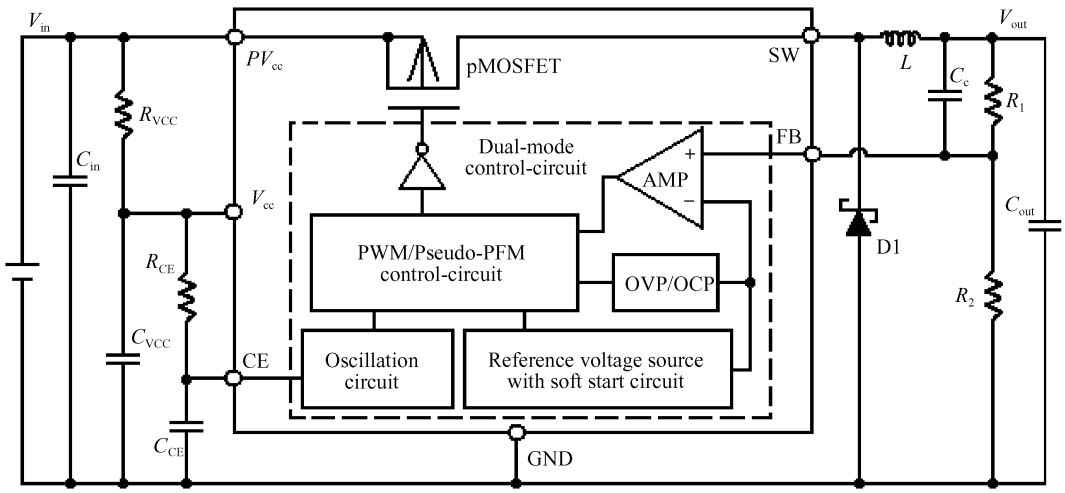

Fig. 1　Block diagram of the chip and external devices

confining its practical application.

In this paper, a novel PWM/pseudo-PFM auto-mode-selected buck DC/DC switching regulator is presented. According to the rank of the load current, the control-circuit automatically changes the mode of modulation, which provides high efficiency and low ripple in the wide load current range. A pMOSFET is hybrid integrated in the package with the control-circuit for fewer external devices.

2　System configuration

Figure 1 shows the block diagram of the proposed PWM/pseudo-PFM auto-mode-selected buck DC/DC switching regulator and external devices. The chip can be divided into two parts: pMOSFET as the output device and the dual-mode control-circuit. PV_{cc} and V_{cc} are the power supply, SW is the output of the pMOSFET, FB is the input of the feedback signal from sample resistors, and CE is the chip-enable signal input. The dual-mode control-circuit consists of an oscillator, error amplifier, reference voltage source, over current and over voltage protection circuit, and mode-selected control-circuit.

Using the node voltage analysis method, the output voltage of the chip is given by

$$V_{out} = V_{ref} \times \left(1 + \frac{R_1}{R_2}\right) \tag{1}$$

where V_{ref} is the output of the inner reference voltage source, and R_1 and R_2 are the external sample resistors.

2.1　PWM/pseudo-PFM control-circuit

When in PWM, the oscillator works continuously and the frequency is normally 600kHz; but in pseudo-PFM, it works intermittently. So, over a long period of time, the equivalent frequency is variable. Because the frequency of the oscillator, when it works, is always about 600kHz, the external filter is easy to design. As stated earlier, to maintain high efficiency over a wide load current range, the key is to automatically select the mode of modulation according to the load current. That is to say, the pulse-width-modulation is selected under heavy load conditions, but the pseudo-pulse-frequency-modulation is selected under light load current conditions.

Because the sample resistance is big, the load current is almost the same as the drain-source current of the pMOSFET, which is the function of the gate control voltage[9]. Duty cycle D is defined as

$$D = \frac{t_{on}}{T_s}, \quad T_s = t_{on} + t_{off} \tag{2}$$

where t_{on} is the on-time of the pMOSFET, t_{off} is its off-time, and T_s is the signal period of the gate control voltage. The relation of V_{in} and V_{out} can be expressed as

$$V_{out} = DV_{in} \tag{3}$$

So, in the continuous condition, the average load current can be given by

$$I_{load} = \frac{DV_{in}}{R_{load}} \tag{4}$$

As shown in Eq. (4), I_{load} is proportional to the duty cycle D. When the duty cycle D is bigger, which means the on-time of the pMOSFET is longer, the I_{load} is bigger; whereas, when the on-time is short, the I_{load} is lower. So, we can detect the duty cycle D instead of detecting the load current. When D is less than 20%, it is the light-load condition, otherwise it is the heavy-load condition. For high efficiency over the whole load current range, the pseudo-pulse-frequency-modulation is selected when D is less than 20%, and the pulse-width-modulation is selected when D is bigger than 20%.

It is not easy to detect the duty cycle of the con-

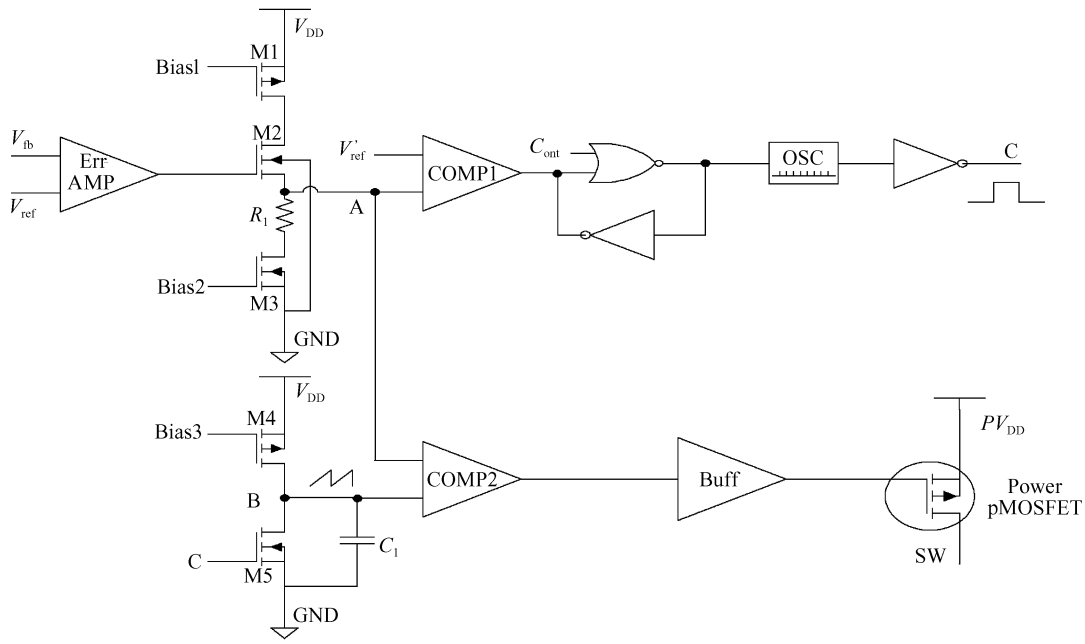

Fig. 2 Schematic of the proposed auto-mode-selected controlled circuit

trol signal directly in an analog circuit, so the duty cycle detection should be transformed to voltage detection. Figure 2 shows the schematic of the proposed auto-mode-selected control circuit. The difference of the feedback voltage and the reference voltage is amplified by the err-amplifier, and then transformed to the comparable voltage V_A by common drain device M2. The signal V_C is the output of the oscillator, and as shown in Fig. 2, it is a pulse with about a 50% duty cycle. The transistor M5 works as a switch, changing the pulse V_C to a sawtooth signal V_B by charging and discharging the capacitor C_1. When the oscillator works, the frequency of its output signal V_C is fixed, and when the transistor M5 is off, the charging current from the transistor M4 is constant. The charging current is given by

$$I_{charge} = \frac{1}{2} u_p c_{ox} \left(\frac{W}{L}\right)_{M4} [V_{GS} - (V_{TH})_{M4}]^2 \quad (5)$$

Ignoring the conducting resistance of M5, the amplitude of the sawtooth signal V_B is given as

$$V_{Ba} = \frac{1}{2C} u_p c_{ox} \left(\frac{W}{L}\right)_{M4} [V_{GS} - (V_{TH})_{M4}]^2 \times 50\% T_S \quad (6)$$

Like all other traditional PWM controllers, the sawtooth signal V_B is compared with V_A by the comparator COMP2 to produce the gate control signal of the power-pMOSFET and the duty cycle of the control signal is decided by the ratio of voltage V_A and V_{Ba}. As V_{Ba} is constant, the duty cycle D is decided by the voltage V_A.

We consider it under the light load condition when the duty cycle of the gate control signal is less than 20%. We assume the duty cycle D is 20% corresponds to when the voltage value of the point A is V'_{ref}. When the voltage value of A is less than V'_{ref}, the oscillator works all through and the whole system works in traditional PWM mode. When the voltage value of A is bigger than V'_{ref}, the output of the comparator COMP1 will change from low state to high to disable the oscillator, which makes V_C become high. Then V_B will become low, and the output signal of the comparator COMP2 turns the pMOSFET off. Consequently, the load current and the feedback voltage V_{fb} (as V_{fb} is proportional to V_{out}) decreases, which makes V_A increase and enables the oscillator again. Thus, the oscillator works intermittently for the whole system in the discontinuous PWM. Over a long time, the discontinuous PWM can be equivalent to the change of the pulse frequency. This condition can be considered as a pseudo-PFM.

2.2 Two stage error amplifier circuit

There is a typical two stage error-amplifier in the control-circuit, as shown in Fig. 3. Between the first differential input stage and the second gain stage, there is a frequency compensation circuit. The amplifier consists of a folded cascode amplifier first stage and a common source output stage for additional gain. Figure 3 shows the differential-mode amplifier schematic excluding bias circuits and frequency compensation circuits. A common source output stage was chosen for additional gain and maximum output swing under 5V supply operation. R_1 changes the differential input voltage into current and makes the output current of the folded cascode amplifier's first stage linear with respect to the input differential voltage.

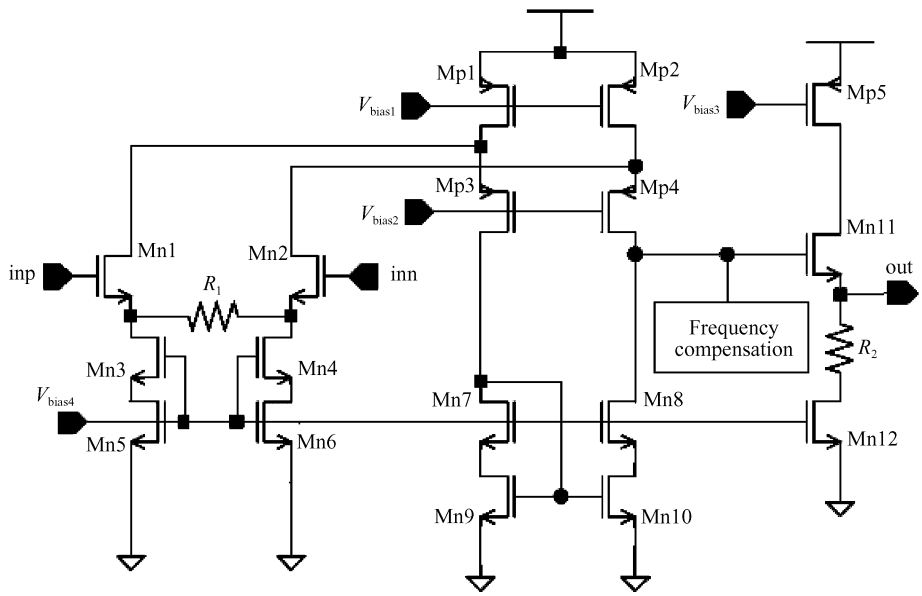

Fig. 3　Schematic of the error amplifier circuit proposed

Mn3, Mn5 are the same as Mn4, Mn6, and can be equivalent to one transistor. They work as loads of the differential input devices: Mn1 and Mn2.

The four transistors Mn3 ~ Mn6 should work in the saturation region to provide the bias voltage needed by two other devices, Mn9 and Mn10. R_{18} can increase the output resistance of the common source stage to get additional gain. It also limits the minimum output voltage of the whole amplifier, and then confirms the minimum output common-mode voltage.

2.3　Comparator circuit

There are two comparators in the control-circuit: the pseudo-PFM comparator (COMP1) and PWM comparator (COMP2). Their structure is the same, as shown in Fig. 4, which is composed of a two stage comparator and a driving inverter.

This structure can drive a big capacitive load well, but without loss in conversion rate of the comparator. The difference between the two comparators is that the input devices (Mp7, Mp8) of the PWM comparator are symmetrical, while those of the pseudo-PFM comparator are not. The asymmetrical inn is connected to GND, and when the voltage applied on inp exceeds (V'_{ref} − GND), the output of the pseudo-PFM comparator (COMP1) will change. Then, this change will make the inner oscillator work intermittently. The discontinuous PWM is determined by the devices' asymmetry. So the stability of the mode change is determined by the precision of the PWM comparator.

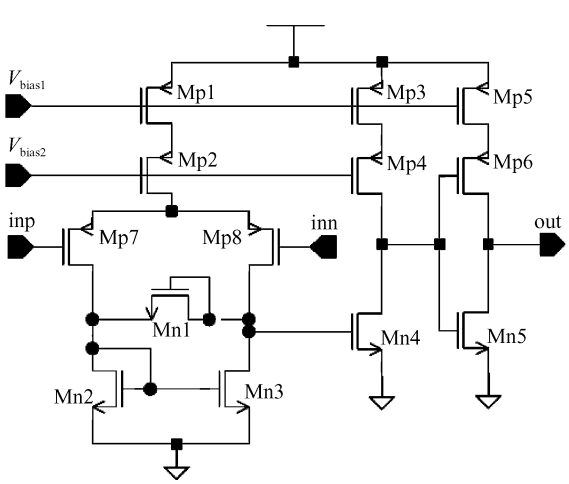

Fig. 4　Schematic of the comparator circuit proposed

3　Simulation

Based on the Bsim3V3 model of 0.5μm DPDM CMOS mixed-signal process, the whole system is simulated by Hspice . Figure 5 (a) shows the simulation waves of gate-control and of the whole system output when the load current is 0.01A. Figure 5 (b) shows those waves when the load current is 3.0A. As seen from these figures, when the load is light (such as 0.01A), the load current required is small. After a short "on" time, the pMOSFET turns to "off" for a long time (the duty cycle is 0%). When the output voltage decreases to less than the pre-specified value, the PWM will be applied for a short time, which will bring on a relatively long "off" time for the pMOSFET. The equivalent frequency of the control signal is changed during this time, so the modulation is called pseudo-PFM. In this condition, the ripple of the output voltage decided by the interval of the two neighbor PWM, as shown in Fig. 5 (a), is about 25mV.

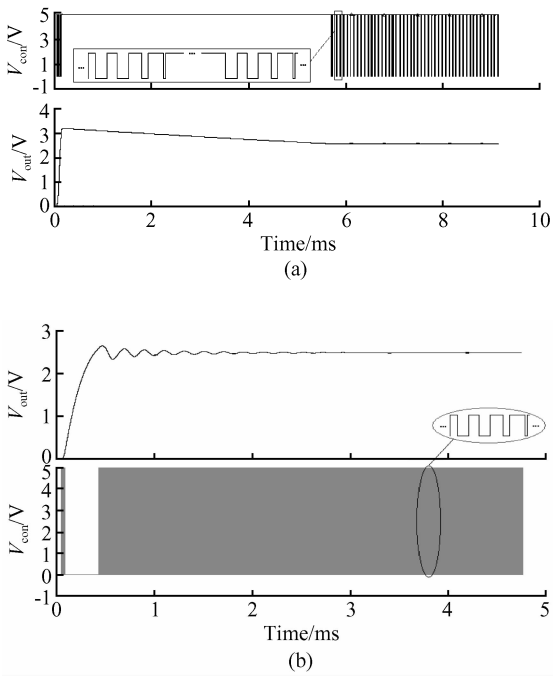

Fig. 5 (a) Voltage waves of the control and output signals at 0.01A load current; (b) Voltage waves of the control and output signals at 3.0A load current

On the other hand, when the load is heavy (such as 3.0A), the PWM is applied. Because the load current required is big at the start, the pMOSFET is "on" all along (the duty cycle is 100%). When the load current or the output voltage increases, the state of the pMOSFET turns from "on" to "off" and the duty cycle begins to decrease from 100%. Until the output voltage approaches the value pre-specified, the duty cycle D is close to the value that is decided by Eq. (3) and the whole system is in the equilibrium of PWM. In this condition, the ripple of output voltage decided by the frequency of control signal, as shown in Fig. 5 (b), is about 3.5mV.

4 Experimental results

The proposed dual-mode-control die is implemented in a 0.5μm DPDM CMOS mixed-signal process. The test chip comprises a dual-mode-control die and a pMOSFET in hybrid integration. The dual-mode-control die's total area is 0.84mm × 0.79mm and the pMOSFET's area is 0.91mm × 1.09mm. With a coil, some capacitors, and a diode connected externally, it can function as a step-down switching regulator (Fig. 1). These ICs serve as ideal power supply units for portable devices when coupled with the TSSOP-8L mini-package, providing such outstanding features as low current consumption.

Figure 6 shows the X-ray photo of the test chip, comprising a dual-mode-control die and a pMOSFET. Some experimental results of the proposed converter in Fig. 1 are listed in Table 1. The line regulation is less than 0.5% and the load regulation less than 1.1%. As the nonlinear load varies, the average efficiency of the proposed converter reaches up to about 90%.

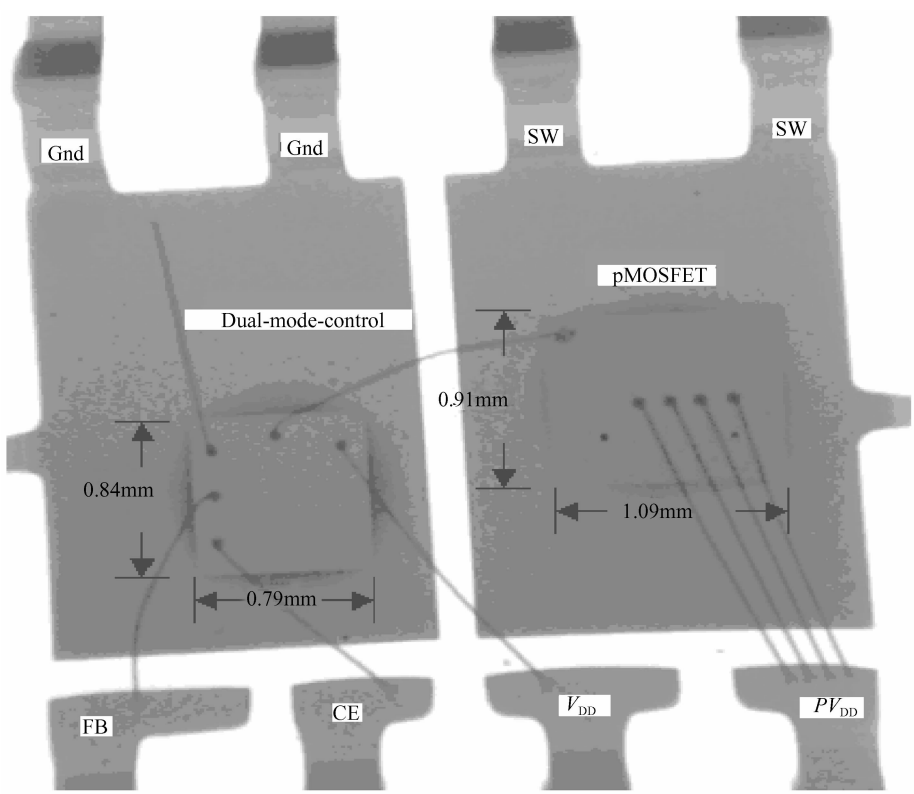

Fig. 6 Pin assignments and the condition of internal connection

Table 1　Experimental results

Parameter	Symbol	Test condition	Value/Unit(Typical)
Current consumption during power on	I_{SS}	$V_{CC}=5V$, $V_{OUT}=2.5V$	1.2mA
Current consumption during power off	I_{SSS}	$V_{CC}=5V$, $V_{CE}=0V$	65μA
Line regulation	R_{Vin}	$V_{CC}=2.5\sim7V@I_{OUT}=0.01A$	0.5%
Load regulation	R_{Vout}	$I_{OUT}=0.01\sim3A$	1.1%
Efficiency1	E_{FF1}	$V_{CC}=5V$, $V_{OUT}=2.5V@I_{OUT}=1.0A$	89%
Efficiency2	E_{FF2}	$V_{CC}=5V$, $V_{OUT}=2.5V@I_{OUT}=0.01A$	92%
Oscillation frequency	F_{osc}	$V_{CC}=5V$	598kHz
Internal reference voltage	V_{ref}	$V_{CC}=5V$	1.21V
Ripple voltage	V_{Rip}	$V_{OUT}=2.5V$; $I_{OUT}=0.01A$	30mV
		$V_{OUT}=2.5V$; $I_{OUT}=3A$	5mV

Figure 7 shows how the efficiency of the proposed bulk DC/DC switching regulator varies with the output current when the input voltage is 3.6V and output voltage is 1.8V. The lower the working temperature is, the higher the conversion efficiency is. When the output current is about 600mA, the efficiency of the proposed bulk DC/DC switching regulator is maximal. Figure 8 is the load transient response between pseudo-PFM and PWM operation, when the load current changes from 300 (the duty cycle is about 15%) to 1300mA (the duty cycle is about 45%).

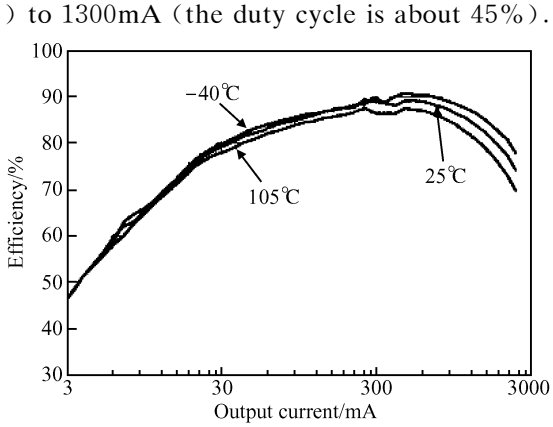

Fig. 7　Efficiency versus output current (V_{in} = 3.6V, V_{out} = 1.8V)

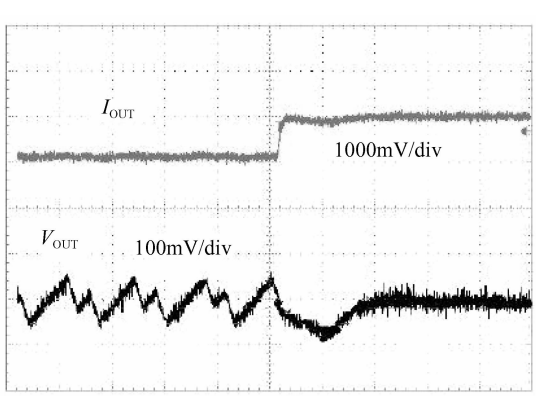

Fig. 8　Load transient response between pseudo-PFM and PWM operation (from 300 to 1300mA)

5　Conclusion

A high-efficiency low-power multimode DC-DC converter with PWM/ pseudo-PFM is proposed in this paper. If duty cycle is greater than 20%, the converter works in PWM mode at 600kHz. When the duty cycle is less than 20%, the converter enters pseudo-PFM mode. In this mode, the equivalent frequency is less than 100kHz, ensuring high efficiency within a large range (10～3000mA) of load current variation. With a coil, some capacitors, and a diode connected externally, the proposed IC achieved an average efficiency of 90%. Therefore, it can provide a low-ripple power over broad ranges of load current. Since this converter can accommodate an input voltage of up to 7.5V, it is also ideal when operating via an AC adapter. These features make the converter in keeping with adapters for portable or hand-held devices.

References

[1] Chung H S H, Hui S Y, Tang S C. Development of a multistage current controlled switched-capacitor step-down DC/DC converter with continuous input current. IEEE Trans Circuit Syst I, 2000, 47(7): 1017

[2] Geng Li, Chen Zhiming, Liu Xianfeng. A monolithically integrated 12V/5V switched capacitor DC-DC converter. Chinese Journal of Semiconductors, 2000, 21(6): 529

[3] Geng Li, Chen Zhiming, Zhao Minling. A novel regulation technique and its application to design SC DC-DC converters. Chinese Journal of Semiconductors, 2004, 25(4): 372

[4] Wu Ge, Shi Yin. Realization of high precision single-way analog switch circuits based on CMOS technology. Chinese Journal of Semiconductors, 2000, 21(12): 1214

[5] Lee C F, Mork P K T. A monolithic current-mode CMOS DC-DC converter with on-chip current-sensing technique. IEEE J Solid-State Circuits, 2004, 39(1): 3

[6] Reed B, Ovens K, Chen J, et al. A high efficiency ultra-deep submicron DC-DC converter for microprocessor applications. 16th International Symposium on Power Semiconductor Devices and

ICs, Kitakyushu, 2004: 59
[7] Fathy K, Miura Y, Yasui K, et al. PWM/PDM dual mode controlled soft switching multi resonant high-frequency inverter. IEEE International Conference on Industrial Technology, 2005: 1450
[8] Wang Jing, Gong Wenchao, He Lenian. Design and implementation of high-efficiency and low-power DC-DC converter with PWM/PFM modes. 7th International Conference on ASIC, 2007: 596
[9] Angel V P, Xiao J W, Sanders S R. Architecture and IC implementation of a digital VRM controller. IEEE Trans Power Electron, 2003, 18(1): 54

一种 PWM/伪 PFM 双模调制的降压型 DC/DC 开关电源*

刘帘曦† 杨银堂 朱樟明

(西安电子科技大学微电子学院，宽禁带半导体材料与器件教育部重点实验室，西安 710071)

摘要：利用根据负载电流的大小变换调制模式的方法实现了一种降压型高转换效率的 DC/DC 开关电源. 当控制电压占空比小于 20%时，采用伪 PFM(pseudo-pulse-frequency modulation)模式调制；占空比大于 20%时，采用 PWM(pulse-width modulation)模式调制，平均转换效率约为 90%，输出电流范围为 0.01～3.0A. 控制芯片采用 0.5μm DPDM CMOS 工艺制造，并采用二次集成的方式在封装内部集成了功率 p-MOSFET.

关键词：脉宽调制；伪频宽调制；占空比；二次集成
EEACC：2570；1280
中图分类号：TN402 **文献标识码**：A **文章编号**：0253-4177(2008)10-1956-07

* 国家自然科学基金(批准号：60776034，60676009)，教育部博士点基金(批准号：20050701015)及国家杰出青年科学基金(批准号：60725415)资助项目
† 通信作者. Email: lxliu@mail.xidian.edu.cn
2008-05-09 收到，2008-06-19 定稿