Modeling of High-Voltage LDMOS for PDP Driver ICs*

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Abstract: A SPICE sub-circuit model is developed for high-voltage LDMOS transistors integrated in PDP driver ICs. The model accounts for intrinsic LDMOS phenomena such as the quasi-saturation effects, voltage-dependent drift resistance, self-heating effects, and Miller capacitance. In contrast to most physical or sub-circuit models, the proposed model not only provides precise simulated results, but also brings a very fast modeling procedure. Furthermore, the model also can be embedded in a commercial SPICE simulator easily. The simulation results using the presented models agree well with the measured ones and the error is less than 5%.

Key words: model; LDMOS; sub-circuit; PDP driver ICs
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1 Introduction

PDP driver ICs play a major role in plasma display panels (PDPs). Nowadays, PDPs have developed towards larger screens and higher resolution. As a result, both the high voltage circuit output pins and frequency in one PDP driver IC increases fast. Optimal design of the output circuit requires an efficient and accurate high voltage LDMOS model. Then, the PDP-driver-IC interrelated LDMOS characteristics must be covered first, such as the quasi-saturation effects, voltage-dependent drift resistance, self-heating effects, and Miller capacitance and so on, but uncharacteristics, like the substrate bias effect and the sub VT effect, can be ignored.

So far, various LDMOS models have been developed. In the customized physical device models[1~6], the internal potentials were solved by a numerical iteration procedure inside the model itself. This approach was valuable due to its relative simplicity and numerical efficiency. The drawbacks of most physical models, however, were high cost, cumbersome parameter extraction and unavailability in commercial simulators. In the sub-circuit models[7~12], the LDMOS transistor was usually described by a combination of circuit elements, including MOS transistors, capacitances, resistances, and diodes and so on. This approach was frequently followed for flexibility, practicality, and compatibility. However, most sub-circuit models could not achieve an adequate level of simulation accuracy for LDMOS transistors, especially when the breakdown voltage was larger.

The purpose of this paper is to propose a 100V nLDMOS model. Every component in this model is not described with the standard MOS transistor, capacitance, resistance, or diode like most research papers[9~12]. They are still sub-circuits and constituted by a SPICE interior voltage controlled source (VCS) and current controlled source (CCS). So the model is compatible with the commercial SPICE simulator. All those different sub-circuits have employed the measured data by a piecewise linear function. This method is an effective solution of modeling intrinsic nLDMOS characteristics.

2 Device description

The nLDMOS transistor investigated in this paper is shown in Fig. 1. In this structure, the n-drift is used to improve the breakdown voltage, and the p-well adjusts the threshold voltage. To make the voltage drop mainly in drain region, n-drift doping must be very low.

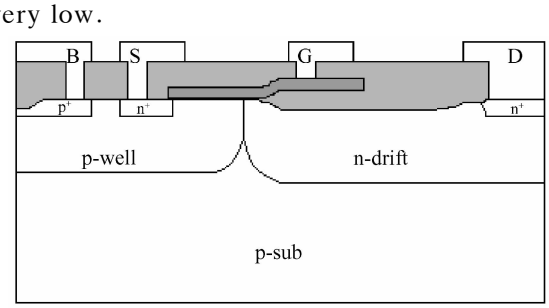

Fig. 1 Cross section of a high-voltage nLDMOS transistor based on 100V CDMOS process

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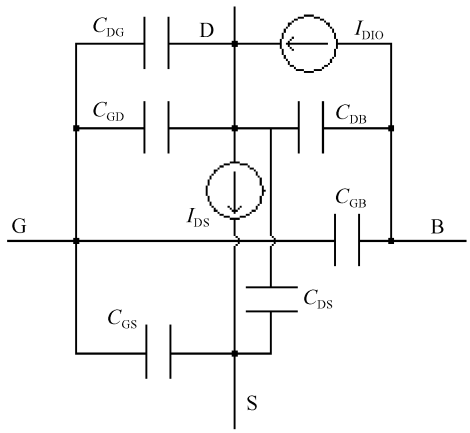

Fig. 2　Sub-circuit model of the high-voltage nLDMOS

This device was fabricated based on a 100V CDMOS process, with 1×10^{15} atoms/cm^3 p-type silicon substrate and 300nm gate oxide. The length and the depth of n-drift are 6 and 2.5μm, respectively, and the effective channel length is 3.5μm. Experimental results indicate that the threshold voltage is 1.7V and the breakdown voltage is 115V.

3　Sub-circuit model

Figure 2 shows the schematic diagram of the complete sub-circuit model. The model is divided into two parts[13]. One is the static current model constituted by a channel current I_{DS} and a drain-to-bulk junction current I_{DIO}, and another is the dynamic capacitance model composed by six capacitances: C_{GS}, C_{GB}, C_{GD}, C_{DS}, C_{DB}, and C_{DG}. Here, C_{DG} and C_{GD} are not the same capacitance. The drain-to-gate parasitical capacitance separated into two elements to recover Miller effects caused by the large drift region series resistances, which depended on the drain and gate voltage. For the same method of static and dynamic model, the static current model will be discussed in detail in the following.

In the static current model, the drain-to-bulk junction current hardly changes with V_{GS}, but the channel current associates with both V_{GD} and V_{DS}. Therefore, the junction and the channel current models are described as 2D and 3D models, respectively.

The 2D current model can be easily obtained by VCCS (voltage controlled current source). Then,

$$I_{DIO} = K_{PLF} V_{DB}$$

where K_{PLF} is the piecewise linear function of V_{DB}.

The 3D current model is illustrated in Fig. 3. It is composed of VCCS, CCCS (current controlled current source), and VCVS (voltage controlled voltage source). All those elements can be embedded in a SPICE simulator easily.

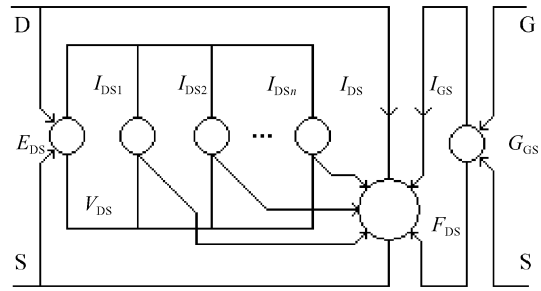

Fig. 3　3D current sub-circuit model of the high-voltage nLDMOS

V_{DS} and I_{GS} are brought by VCVS E_{DS} and VCCS G_{GS}, respectively. I_{DS1}, I_{DS2}, $\cdots$, I_{DSn} are VCCS and reproduce the measured I_{DS}-V_{DS} curves by a SPICE piecewise linear function under various V_{GS} values. n is the number of measured I_{DS}-V_{DS} curves. Finally, I_{GS} and I_{DSi} will be calculated by a VCCS F_{DS} to get the model output I_{DS}. The I_{DSi} can be written as

$$I_{DSi} = K_{PLFi} V_{DS}, \quad i = 1, 2, \cdots, n \tag{1}$$

where K_{PLFi} is the piecewise linear function of V_{DS}. To set up the relationship between I_{DS} and V_{GS}, an assistant function I_{SWITCH} is given, as shown in Eq. (2).

$$I_{SWITCH} = K_{SWT(i+1)i} V_{GS} \tag{2}$$

where $K_{SWT(i+1)i}$ is the piecewise linear function of V_{GS}. If V_{GS} locates in $[V_{GSi}, V_{GS(i+1)}]$, $K_{SWT(i+1)i}$ is a constant. Otherwise, $K_{SWT(i+1)i}$ is zero. In other words, I_{SWITCH} is a switch function.

To acquire a 3D current model, it is assumed that I_{DS} is a linear current in $[V_{GSi}, V_{GS(i+1)}]$, when V_{DS} is constant and the interval is small enough. Then a continuous function is achieved in Eq. (3).

$$I_{DS} = \sum_{i=1}^{n} [(1 - A) I_{DSi} + A I_{DS(i+1)}] I_{SWITCH} \tag{3}$$

where

$$A = \frac{V_{GS} - V_{GSi}}{V_{GS(i+1)} - V_{GSi}} \tag{4}$$

Substituting Eqs. (1), (2), and (4) into Eq. (3), the following equation can be obtained:

$$I_{DS} = \sum_{i=1}^{n} \left[\left(1 - \frac{V_{GS} - V_{GSi}}{V_{GS(i+1)} - V_{GSi}}\right) K_{PLFi} V_{DS} + \frac{V_{GS} - V_{GSi}}{V_{GS(i+1)} - V_{GSi}} \times K_{PLF(i+1)} V_{DS} \right] K_{SWT(i+1)i} V_{GS} \tag{5}$$

where I_{DS} is a continuous function of V_{DS} and V_{GS}. The measured and modeled I_{DS}-V_{GS} curve is shown in Fig. 4. The test condition is that $V_{DS} = 0.1$V and $W_{LDMOS} = 80\mu$m. As can be seen in Fig. 4, the modeled results deviate from measured ones when $1\text{V} < V_{GS} < 2\text{V}$. This is mainly because I_{DS} is a logarithmic function of V_{GS}, when a small voltage adds to the gate. But when the gate voltage is large enough, I_{DS} changes to a linear function of V_{GS}. Therefore, Equation (3) is changed to Eq. (6) when V_{GS} is less than 2V.

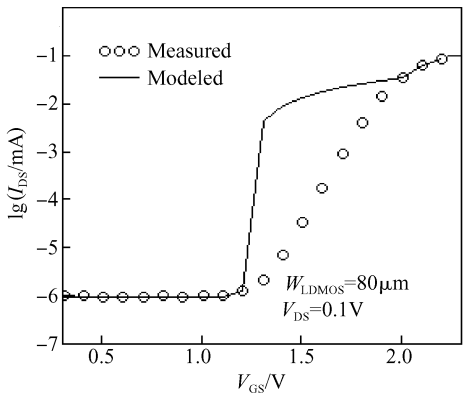

Fig. 4 Modeled (solid lines) and measured (symbols) I_{DS}-V_{GS} curves for W_{LDMOS} = 80μm at V_{DS} = 0.1V

$$I_{DS}=\sum_{i=1}^{n} e^{[(1-A)\lg I_{DSi}+A\lg I_{DS(i+1)}]} \times I_{SWITCH}, \quad V_{GS} < 2V \tag{6}$$

Then:

$$I_{DS} = \sum_{i=1}^{n} {I_{DSi}}^{1-A} \times {I_{DS(i+1)}}^{A} \times I_{SWITCH}, \quad V_{GS} < 2V \tag{7}$$

Substituting Eqs. (1), (2), and (4) into Eq. (7), the following equation can be obtained:

$$I_{DS} = \sum_{i=1}^{n} (K_{PLFi}V_{DS})^{1-\left(\frac{V_{GS}-V_{GSi}}{V_{GS(i+1)}-V_{GSi}}\right)} \times (K_{PLFi}V_{DS})^{\frac{V_{GS}-V_{GSi}}{V_{GS(i+1)}-V_{GSi}}} K_{SWT(i+1)i}V_{GS} \tag{8}$$

4 Results and discussion

Figure 5 (a) shows the measured and the modeled drain-to-bulk junction current curves. The 2D modeled result tallies with the real one very well when V_{GS} = 0V, V_{BD} < 1.1V and W_{LDMOS} = 80μm. In this figure, the maximum tested voltage is only 1.1V, for 20mA current limitation of HP4155. In order to model a continuous junction current, an exponential function is assumed, as V_{BD} > 1.1V.

In Fig. 5 (b), the modeled and measured channel current is plotted versus gate voltage, at V_{DS} = 0.1V. In comparison to Fig. 4, the curve fits better over the whole gate-bias range. In Fig. 5 (c), the modeled and measured channel current is plotted versus drain voltage, at V_{GS} = 3, 4, and 5V. The modeled results are in a good agreement with the measured ones in all tested conditions. In additional, a negative output conductance can be obtained in modeled results, which clearly demonstrates the effect of self-heating.

With the same method, the dynamic capacitance model can be finished. Furthermore, the pLDMOS sub-circuit model can also be set up very easily.

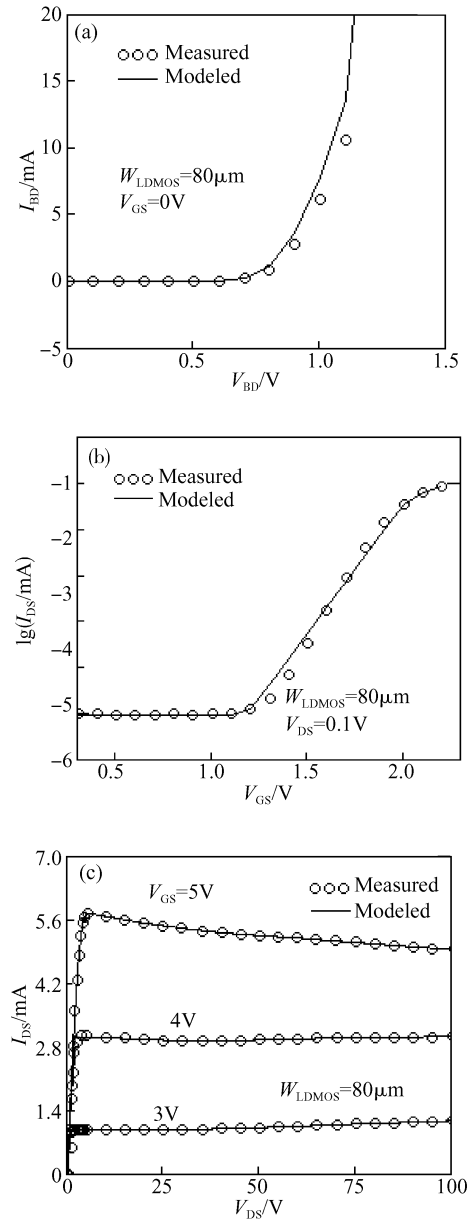

Fig. 5 Modeled (solid lines) and measured (symbols) current curves for W_{LDMOS} = 80μm (a) I_{BD}-V_{BD}, at V_{GS} = 0V; (b) I_{DS}-V_{GS}, at V_{DS} = 0.1V; (c) I_{DS}-V_{DS}, at V_{GS} = 3, 4, and 5V

5 Circuit application

The proposed nLDMOS model is used to simulate a low-to-high voltage driver circuit of PDP driver ICs. The circuit is shown in Fig. 6. P1, P2, and P3 are the high-voltage pLDMOS, and N1, N2, and N3 are the high-voltage nLDMOS. LV1, LV2, and LV3 are low voltage control signal and Q is the high-voltage output. The circuit is simulated with the sub-circuit models to compare with the oscilloscope measured data at V_{PP} = 30, 60, and 90V respectively. During testing, the load capacitance is selected 50pF. However, during simulation, 65pF load capacitance is chosen. This is mainly because the oscilloscope probe has an inherent 10pF capacitance approximately, and the

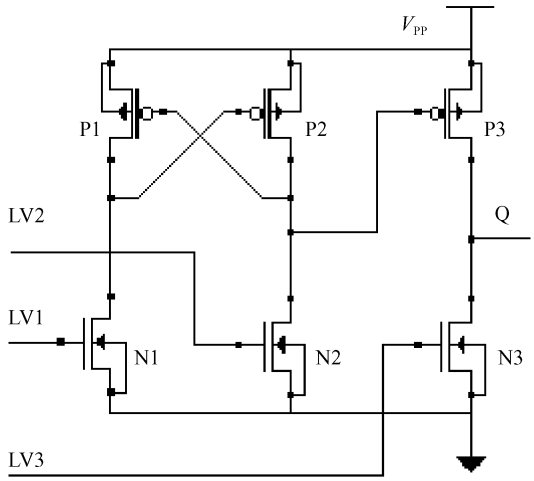

Fig. 6　Low-to-high voltage diver circuit of PDP driver ICs

PCB and IC package also have parasitical capacitance of about 5pF.

Figure 7 shows the rise time and the fall time of high-voltage output waveforms, at V_{PP} = 30, 60, and 90V. The model's simulated results agree with the measured ones very well, and the error is less than 5%.

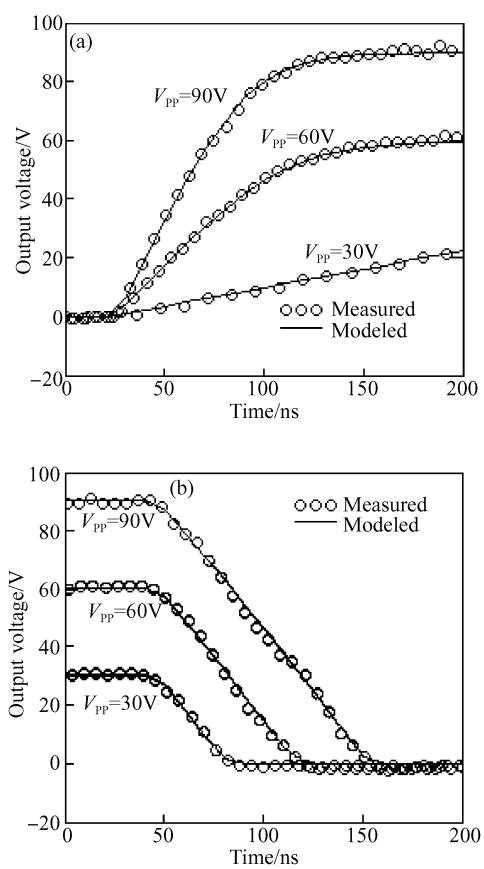

Fig. 7　Modeled (solid lines) and measured (symbols) high-voltage output curves, at V_{PP} = 30, 60, and 90V　(a) Rise time; (b) Fall time

6　Conclusion

In this paper, an efficient and accurate nLDMOS sub-circuit model has been suggested. In the model, every component was not described by the standard MOS transistor, capacitance, resistance, or diode. They are still sub-circuits and constituted by a SPICE interior voltage controlled source (VCS) and current controlled source (CCS). So the model also could be embedded in a commercial SPICE simulator easily. When the proposed model was applied to simulate a low-to-high voltage circuit of PDP driver ICs, it was shown that measured and simulated results fitted well, which proves the presented model is valuable.

References

[1] D'Halleweyn N, Tiemeijer N V, Benson L F, et al. Charge model for SOI LDMOST with lateral doping gradient. Power Semiconductor Devices and ICs, 2001

[2] Chauhan Y S, Anghel C, Krummenacher F, et al. Scalable general high voltage MOSFET model including quasi-saturation and self-heating effect. Solid-State Electron, 2006, 50(11/12): 1801

[3] Aarts A, D'Halleweyn N, van Langevelde R. A surface-potential-based high-voltage compact LDMOS transistor model. IEEE Trans Electron Devices, 2005, 52(5): 999

[4] Aarts A, Kloosterman W. Compact modeling of high-voltage LDMOS devices including quasi-saturation. IEEE Trans Electron Devices, 2006, 53(4): 897

[5] Aarts A C T, Kloosterman W J. Compact modeling of high-voltage LDMOS devices including quasi-saturation. IEEE Trans Electron Devices, 2006, 53(4): 897

[6] Chauhan Y S, Krummenacher F, Gillon R, et al. Compact modeling of lateral nonuniform doping in high-voltage MOSFETs. IEEE Trans Electron Devices, 2007, 54: 1527

[7] Cuoco V, vd Heijden M, de Vreede L C N. The "Smoothie" data base model for the correct modeling of non-linear distortion in FET devices. IEEE MTT-S, 2002, 3: 2149

[8] Pawel S, Kusano H, Nakamura Y, et al. Simulator-independent capacitance macro model for power DMOS transistors. ISPSD, 2003: 287

[9] Moncqut D, Fareng D, Rossel P, et al. LDMOS transistor for smart power circuits: modeling and design. Proc IEEE BCTM, 1996: 216

[10] Driffith E C, Power J A, Elebert P, et al. Characterization and modeling of LDMOS transistors on a 0.6μm CMOS technology. ICMTS, 2000: 175

[11] Canepari A, Bertrand G, Giry A, et al. LDMOS modeling for analog and RF circuit design. Proceedings of ESSDERC, Grenoble, France, 2005: 469

[12] Scott R S, Franz G A, Johnson J L. An accurate model for power DMOSFET's including interelectrode capacitances. IEEE Trans Power Electron, 1991, 6(2): 192

[13] Li Haisong, Sun Weifeng, Yi Yangbo, et al. Parasitical capacitance of NLDMOS for a flat panel display driver IC. Chinese Journal of Semiconductors, 2005, 26(7): 1379 (in Chinese) [李海松, 孙伟锋, 易扬波, 等. 平板显示器驱动芯片中 NLDMOS 寄生电容. 半导体学报, 2005, 26(7): 1379]

PDP 驱动芯片中高压 LDMOS 建模*

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摘要：建立了 PDP 驱动芯片用高压 LDMOS 的 SPICE 子电路模型，该模型集成了 LDMOS 固有特性：准饱和特性、电压控漂移区电阻、自热效应、密勒电容等.与其他物理模型和子电路模型比较，该模型不但能提供准确的模拟结果，而且建模简单快捷，另外该模型可较容易地嵌入 SPICE 模拟软件中.模型的实际应用结果显示：模拟与实测结果误差在 5%以内.

关键词：模型；LDMOS；子电路；PDP 驱动芯片

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