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Output Characteristics of n-Buried-pSOI Sandwiched RF Power LDMOS

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Abstract: A novel n-buried-pSOI sandwiched structure for an RF power LDMOS is proposed. The output characteristics of the RF power LDMOS are greatly affected by the drain-substrate parasitic capacitance. The output characteristics become better as the drain-substrate parasitic capacitance decreases. Results show that the drain-substrate capacitance of the n-buried-pSOI sandwiched LDMOS is 46.6% less than that of the normal LDMOS, and 11.5% less than that of the n-buried-pSOI LDMOS, respectively. At 1dB compression point, its output power is 188% higher than that of the normal LDMOS, and 10.6% higher than that of the n-buried-pSOI LDMOS, respectively. The power-added efficiency of the proposed structure is 38.3%. The breakdown voltage of the proposed structure is 11% more than that of the normal LDMOS.

Key words: n-buried-pSOI; sandwiched; parasitic capacitance; output characteristics; RF power LDMOS
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1 Introduction

The RF power device is considered as a very important basis for wireless communication technology[1~3]. RF power LDMOS is widely used in narrowband and high-gain technology for wireless communication and is regarded as a very successful RF power device[2,4,5]. The advantages are as follows. First, its high constant transconductance in a wide current range creates a large dynamic range of linear amplification, leading to great linear gain when output power is high. Second, the cross modulation distortion level is low. Third, the performance-cost ratio is high. However, the parasitic output capacitance of LDMOS will directly affect its output characteristics, including power gain, power-added efficiency, and so on.

Scholars proposed the SOI LDMOS structure in order to alleviate the parasitic effects and increase breakdown voltage[5~9], but the self-heat effect and parasitic pin inductances of the SOI structure badly affected its exploitation and application. Therefore, researchers put forward pSOI and n-buried-pSOI LDMOS, which can help to reduce the output capacitance, increase breakdown voltage, and optimize output characteristics[1,2,5,12].

To obtain much lower output capacitance, an n-buried-pSOI sandwiched structure of RF power LDMOS is proposed in this paper. The output characteristics of the n-buried-pSOI sandwiched, n-buried-pSOI and normal RF power LDMOS are analyzed, and they are numerically evaluated with the help of MEDICI and the RF power emulator Affirma. The breakdown voltages of the three devices are also analyzed.

2 Device structure

The structures of normal, n-buried-pSOI and n-buried-pSOI sandwiched RF power LDMOS are illustrated in Figs. 1(a), 1(b), and 1(c), respectively. The dashed lines indicate the boundaries of depletion regions. To make the analysis easier, the dotted line in Fig. 1(a) trisects the depletion region, forming an n^+-drain/p^--epitaxy junction. t_n and L_{drift} indicate the oxide thickness and drift area length, respectively, and L_b indicates the lateral distance of the depletion region corresponding to C_b. In RF power LDMOS, the output capacitance consists of the drain-substrate capacitance C_{ds}, the drain-gate capacitance C_{gd}, and the metal connection capacitance between the drain and source. The metal connection capacitance can be decreased by layout design, while C_{ds} and C_{gd} can be reduced only through structural design and optimization.

3 Output characteristics

The small-signal equivalent circuit for the RF power LDMOS is shown in Fig. 2. We obtain the output power transmitted to load R_L as[1,10]

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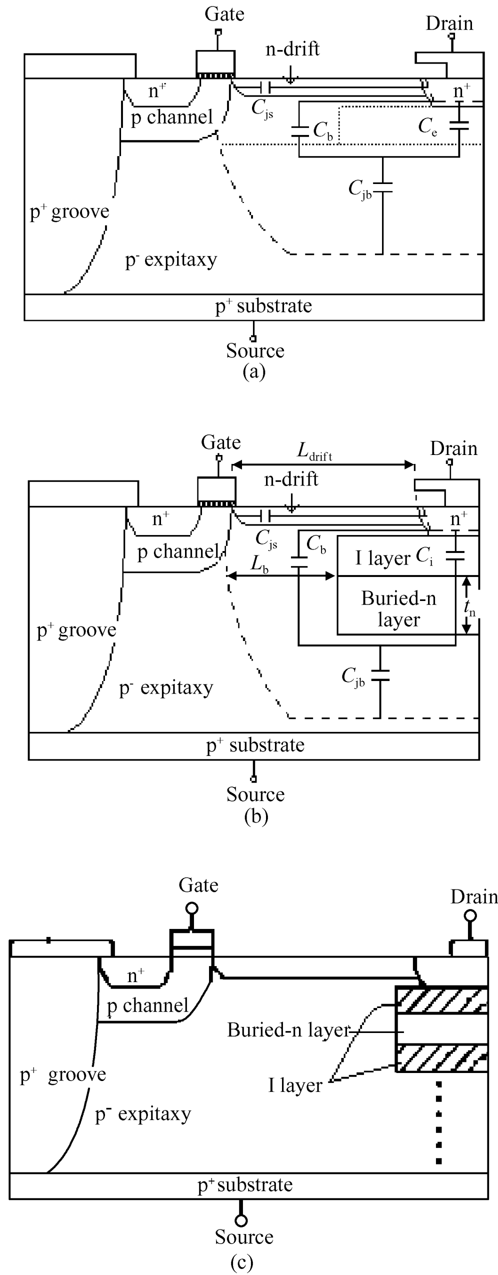

Fig. 1 Cross section of three structures of RF power LDMOS (a) Normal; (b) n-buried-pSOI; (c) n-buried-pSOI sandwiched

$$P_{out} = \frac{V_{in}^2 g_m^2 R_L}{2(1 + \omega^2 C_{oss}^2 R_L^2)} \tag{1}$$

where V_{in} is the input voltage, ω the working frequency, g_m the device transconductance, and C_{oss} the output capacitance, which is given by $C_{oss} = C_{gd} + C_{ds}$. Equation (1) shows that the output power P_{out} decreases as C_{oss} increases, especially when the frequency is high.

In Fig. 1(a), the drain-substrate capacitance is mostly n^+-drain/p^--epitaxy junction capacitance and is determined by the depletion region width, junction area, reverse biased voltage, and the doping concentration of p^- epitaxy. C_{ds} is given by

$$C_{ds} = \frac{(C_b + C_e) C_{jb}}{C_b + C_e + C_{jb}} + C_{js} \tag{2}$$

where C_{js} is the depletion capacitance in the n^--drift

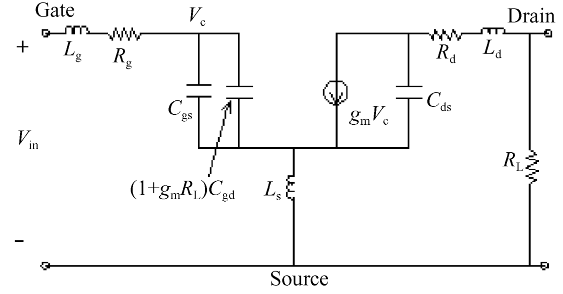

Fig. 2 Small-signal equivalent circuit of the LDMOS device

region, and C_b, C_e, and C_{jb} are the capacitances corresponding to the depletion regions divided by the dotted line in Fig. 1(a), respectively. The junction capacitance is equivalent to parallel planar capacitance, so it can be reduced by decreasing the junction area. However, this will increase the contact resistance and decrease the drive current. Therefore, the output capacitance cannot be reduced completely by decreasing the junction area.

In Fig. 1(b), pSOI is introduced between the n^+-drain and p^--epitaxy. C_{ds} of the device is given by

$$C_{ds} = \frac{(C_b + C_i) C_{jb}}{C_b + C_i + C_{jb}} + C_{js} \tag{3}$$

where C_i is capacitance of the buried oxide. To make the analysis easier, we assume that L_b in the epitaxial depletion region is unchanged, and the buried oxide simply replaces the depletion region there (C_i replaces C_e). C_i is less than C_e because the relative dielectric constant of SiO_2 is less than that of Si. Then we obtain that the output capacitance of RF power LDMOS is less than that of the normal LDMOS. In fact, the existence of I layer makes the direction of the electric field change, and L_b in Fig. 1(b) corresponding to C_b is reduced, so is C_b. Therefore, the presence of buried oxide causes C_{ds} to decrease. The depletion area corresponding to C_{jb} increases and the drain-substrate capacitance is reduced after introducing the buried-n structure. With the help of Gauss theory, we determine that C_{jb} can be further reduced if we introduce an n-buried-pSOI sandwiched structure, which is shown in Fig. 1(c).

The optimized structure parameters of the three devices are as follows: the junction depth of drain and source is 1μm, the doping concentration of the drain and source is $1.6 \times 10^{19} cm^{-3}$, the junction depth, doping concentration and length of the drift region are 0.5μm, $1.3 \times 10^{16} cm^{-3}$, and 4.5$\mu$m respectively, the doping concentration is $4.2 \times 10^{16} cm^{-3}$ for p channel, $1 \times 10^{18} cm^{-3}$ for substrate, $4.9 \times 10^{14} cm^{-3}$ for epitaxy and $2.1 \times 10^{18} cm^{-3}$ for p^+ groove. The thickness of epitaxy is 6μm. In the n-buried-pSOI structure, the thickness of I layer is 1.5μm, and the thickness and doping concentration of buried-n layer are 3.5μm and

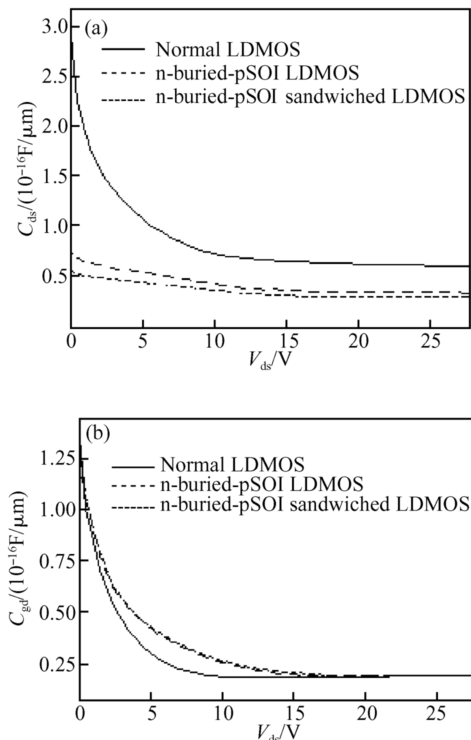

Fig. 3 (a) C_{ds} of three structures versus V_{ds}; (b) C_{gd} of three structures versus V_{ds}

$5\times10^{14}cm^{-3}$ each. In the n-buried-pSOI sandwiched structure, the thickness is 1μm for the upper I layer, 1μm for the upper buried-n layer, 1μm for the lower I layer, and 2μm for the lower buried-n layer. The doping concentration of the upper and lower buried-n layers is $6\times10^{14}cm^{-3}$.

The relationship between C_{gd} and V_{ds} of the three structures obtained with the two-dimensional emulator MEDICI, when $V_{gs}=0V$, $f=1MHz$, are measured and shown in Figs. 3 (a) and 3 (b). As shown in Fig. 3 (a), when $V_{ds}=0V$, C_{ds} of the n-buried-pSOI sandwiched LDMOS is $5.406\times10^{-17}F/\mu m$, 81.6% lower than that of the normal LDMOS, $2.94\times10^{-16}F/\mu m$, and 11.9% lower than that of the n-buried-pSOI LDMOS, $6.13\times10^{-17}F/\mu m$. In working condition, when $V_{ds}=28V$, C_{ds} of the n-buried-pSOI sandwiched LDMOS is $3.036\times10^{-17}F/\mu m$, 46.6% lower than that of the normal LDMOS, $5.687\times10^{-17}F/\mu m$, and 12.3% lower than that of the n-buried-pSOI LDMOS, $3.465\times10^{-17}F/\mu m$.

In all, C_{gd} of the three structures is built by a series combination of C_{js} and oxide capacitance formed by the drift region and gate overlapping[11]. In this paper, the three structures are of the same dimensions, therefore their capacitances formed by drift region and gate overlapping are equal. For n-buried-pSOI and n-buried-pSOI sandwiched structures, when $V_{ds}=28V$, the existence of I layer and buried-n layer changes the vertical electric field distribution, but has little impact on the lateral electric field distribution. So C_{js} of the three structures are basically equal. According to Fig. 3(b), C_{gd} of the three structures is 1.33×10^{-16} F/μm for $V_{ds}=0V$, and $1.94\times10^{-17}F/\mu m$ for $V_{ds}=28V$.

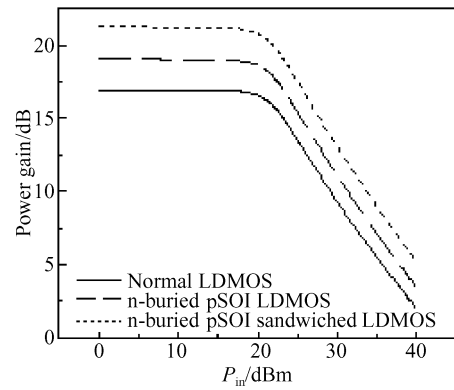

Fig. 4 Power gain versus input power

Analyzing the output characteristics of LDMOS by means of an RF power emulator Affirma, we obtain that the dependence of the power gain and the power-added efficiency on the input power are as plotted in Fig. 4 and Fig. 5. For all the three structures, the threshold voltage is $V_{th}=3.75V$, channel length is 0.8μm, and gate width is 1474μm. At 1dB compression point, the output power of the n-buried-pSOI sandwiched LDMOS is 18.86W. It is 188% higher than that of the normal LDMOS, 6.54W, and 10.6% higher than that of the n-buried-pSOI LDMOS, 16.86W. The output power gain of the n-buried-pSOI sandwiched LDMOS is 20.55dB. It is 30.6% higher than that of the normal LDMOS, 15.73dB, and 4% higher than that of the n-buried-pSOI LDMOS, 19.78dB. The power-added efficiency of the n-buried-pSOI sandwiched LDMOS is 38.3%, while that of the normal and n-buried-pSOI LDMOS is 32.1% and 37.3% each.

The relations between the breakdown voltage and drift area length of LDMOS are shown in Fig. 6.

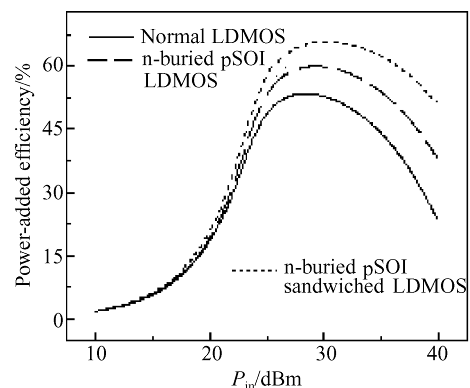

Fig. 5 Power-added efficiency versus input power

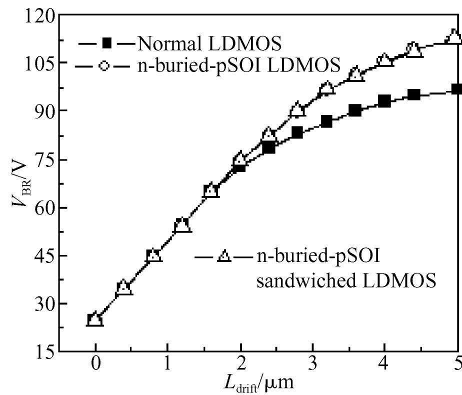

Fig.6 Breakdown voltage versus length of the drift region of three structures

This figure shows that the breakdown voltages of the n-buried-pSOI sandwiched structure and the n-buried-pSOI LDMOS are almost the same. When L_{drift} = 5.0μm, the breakdown voltage is 110.5V for the n-buried-pSOI sandwiched LDMOS, and 110V for the n-buried-pSOI LDMOS. Both are about 11% higher than that of the conventional LDMOS, 99.1V. The reason is that the buried oxide I layer enhances the breakdown voltages of the device, especially when the drift length is larger.

All the LDMOS devices shown above are n channel. The structures can also be used in p channel LDMOS and the output characteristics of these structures show obvious improvements compared to the normal LDMOS and pSOI LDMOS. The buried layer of the pchannel LDMOS is p-type.

The two buried n-layers pSOI sandwiched structure of LDMOS will be realized using the SOI method[13], shown in Fig.7. The process of the technology is: first, grow a p^- epitaxy on the p^+ substrate, infuse n-type impurity and anneal to form the n-type buried layer; Then etch grooves and fill the insulators in, and polish to get a lower I layer. After that, grow a p^- layer by hetero-epitaxy technology, and by the infusion of n-type impurity and annealing to form the upper n-type buried layer; Then etch grooves and fill the insulators in, polish again to form the upper I layer. Finally, grow a p^- layer by the hetero-epitaxy technology. Then the structure and device are completed. The multilayer of the n-buried-pSOI is obtained by replaying the n-buried, trench, and p^- epitaxy. Because the output characteristics are promoted weakly when there are more than 3 layers and the exposal level is inaccurate, the n-buried-pSOI sandwiched RF LDMOS is built with two buried n-layers.

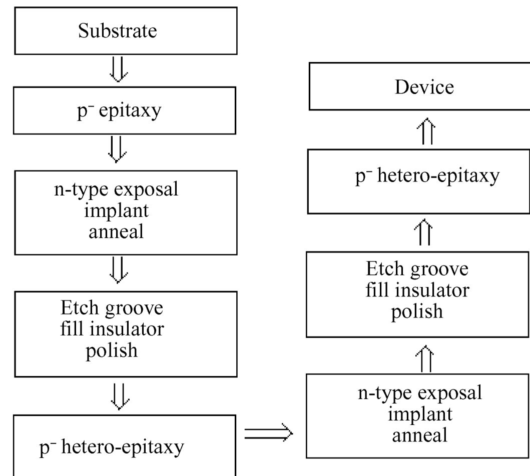

Fig.7 Method of the buried-n-pSOI sandwiched structure

4 Conclusion

The paper puts forward a novel n-buried-pSOI sandwiched structure of RF power LDMOS. The analysis indicates that the output characteristics of this device are improved greatly over the conventional LDMOS and the n-buried-pSOI RF power LDMOS previously proposed by the authors. When V_{ds} = 0V, C_{ds} of the n-buried-pSOI sandwiched structure is 81.6% and 11.9% lower than that of the conventional LDMOS and the n-buried-pSOI RF power LDMOS, respectively. In working condition, its drain-substrate junction capacitance is 46.6% and 11.5% lower than that of the conventional LDMOS and the n-buried-pSOI RF power LDMOS, respectively. Its output power at the 1dB compression point is 188% and 10.6% higher than that of the conventional LDMOS and the n-buried-pSOI RF power LDMOS. The power-added efficiency increases from 37.3% for the n-buried-pSOI LDMOS to 38.3% for this structure. At the same time, the breakdown voltage of this device is enhanced around 11% compared to that of the normal LDMOS. We also gave the fabrication method of the structure.

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具有 n 埋层 pSOI 三明治结构的射频功率 LDMOS 的输出特性

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摘要: 提出了具有 n 埋层 pSOI 三明治结构的射频功率 LDMOS 器件.漏至衬底寄生电容是影响射频功率 LDMOS 器件输出特性的重要因素之一,寄生电容越小,输出特性越好.分析表明 n 埋层 pSOI 三明治结构的射频功率 LDMOS 漏至衬底的结电容比常规射频功率 LDMOS 和 n 埋层 pSOI 射频功率 LDMOS 分别降低 46.6% 和 11.5%.该结构器件 1dB 压缩点处的输出功率比常规 LDMOS 和 n 埋层 pSOI LDMOS 分别提高 188% 和 10.6%,附加功率效率从 n 埋层 pSOI LDMOS 的 37.3% 增加到 38.3%.同时该结构器件的耐压比常规 LDMOS 提高了约 11%.

关键词: n 埋层 pSOI; 三明治; 寄生电容; 输出特性; 射频功率 LDMOS

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