A 10bit 100MS/s Pipelined ADC with an Improved 1.5bit/Stage Architecture*

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Abstract: This paper presents a 10bit 100MS/s CMOS pipelined analog-to-digital converter (ADC) based on an improved 1.5bit/stage architecture. The ADC achieves a peak signal-to-noise-and-distortion ratio (SNDR) of 57dB and maintains 51dB up to 57MHz, the Nyquist frequency for a clock rate of 100Msample/s. The differential non-linearity (DNL) and integral non-linearity (INL) are typically measured as 0.3LSB and 1.0LSB, respectively. The ADC is implemented in a 0.18μm mixed-signal CMOS technology and occupies 0.76mm^2.

Key words: analog-to-digital converter; pipeline; improved 1.5bit/stage architecture
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1 Introduction

High performance ADCs are necessary in versatile applications such as wireless communication systems, high speed instrumentations and high quality video systems. Higher resolution, higher sampling rate and lower power consumption are usually the main concerns for the ADCs used in these applications. The pipelined ADC has been largely studied and widely used because of the good trade-off among the speed, resolution, power consumption and chip area. In previous studies, most design interests were focused on the first pipelined stage, wideband SHA or other techniques for performance improvement[1~3], but seldom on the last stage of pipelined ADC. However, the non-monotonicity of pipelined ADC caused by the last stage will reduce the linearity and should not be ignored.

In this paper, the non-monotonicity of the traditional 1.5bit/stage pipelined ADC is analyzed, and an improved 1.5bit/stage pipelined architecture with a new last stage is proposed. To demonstrate the improvement, a 10bit 100MS/s pipelined ADC with an extra correction stage is implemented in a 0.18μm mixed-signal CMOS technology.

2 Analysis of non-monotonicity

Usually, 1.5bit/stage architecture[4] is applied to most 10bit pipelined ADCs because of its power-optimized per stage resolution, which also relaxes the requirement of sub-ADC comparators. If the output of an ADC is k bit, the conventional ADC is composed of $k-2$ pipelined stages and a 2bit flash ADC as the last stage.

According to the 1.5bit/stage algorithm and pipeline theory, we can derive the residue output of the $(k-2)_{\text{th}}$ stage which is also the analog input of the last stage from the digital outputs of the previous stages.

$$V_i(k-1) = V_o(k-2) = 2^{k-2}V_{\text{in}} - [2^{k-3}D_1 + \cdots + D_{k-2} - (2^{k-3} + \cdots + 1)]V_r \quad (1)$$

where V_{in} is the input signal, D_k is the digital output of the $(k)_{\text{th}}$ stage, and V_r is the reference voltage.

As to the last stage, it is a standard 2bit flash ADC which has three decision levels: $-V_r/2$, 0 and $V_r/2$. Assuming that the offset errors of these decision levels are ε_1, ε_2 and ε_3, the decision ranges of the last stage are given by

$$\begin{cases} D_{k-1} = 0(00)_2 \Rightarrow V_i(k-1) \in [-V_r, -V_2/2 + \varepsilon_1] \\ D_{k-1} = 1(01)_2 \Rightarrow V_i(k-1) \in [-V_2/2 + \varepsilon_1, \varepsilon_2] \\ D_{k-1} = 2(10)_2 \Rightarrow V_i(k-1) \in [\varepsilon_2, +V_r/2 + \varepsilon_3] \\ D_{k-1} = 3(11)_2 \Rightarrow V_i(k-1) \in [+V_r/2 + \varepsilon_3, V_r] \end{cases} \quad (2)$$

where D_{k-1} and $V_i(k-1)$ is the digital output and analog input of the last stage.

Also according to the digital correction algorithm, the output code of the pipelined ADC can be written as

$$D = 2^{k-2}D_1 + 2^{k-3}D_2 + \cdots + 2D_{k-2} + D_{k-1} \quad (3)$$

So if the output code of ADC is an even number

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(assuming $D=2N$), the last stage output D_{k-1} must be an even number. Contrary wise, If D is an odd number ($D=2N+1$), D_{k-1} must be an odd number.

$$\begin{cases} D=2N, D_{k-1}=0(00)_2 \Rightarrow V_{in} \in \left[\frac{2N}{2^k}\times 2V_r - V_r, \frac{2N+1}{2^k}\times 2V_r - V_r + \frac{\varepsilon_1}{2^{k-2}}\right] \\ D=2N+1, D_{k-1}=1(01)_2 \Rightarrow V_{in} \in \left[\frac{2N+1}{2^k}\times 2V_r - V_r + \frac{\varepsilon_1}{2^{k-2}}, \frac{2N+2}{2^k}\times 2V_r - V_r + \frac{\varepsilon_2}{2^{k-2}}\right] \\ D=2N, D_{k-1}=2(10)_2 \Rightarrow V_{in} \in \left[\frac{2N}{2^k}\times 2V_r - V_r + \frac{\varepsilon_2}{2^{k-2}}, \frac{2N+1}{2^k}\times 2V_r - V_r + \frac{\varepsilon_3}{2^{k-2}}\right] \\ D=2N+1, D_{k-1}=3(11)_2 \Rightarrow V_{in} \in \left[\frac{2N+1}{2^k}\times 2V_r - V_r + \frac{\varepsilon_3}{2^{k-2}}, \frac{2N+2}{2^k}\times 2V_r - V_r\right] \end{cases} \quad (4)$$

It is also can be shown by Fig. 1, where

$$X_1 = \frac{2N}{2^k}\times 2V_r - V_r; X_2 = \frac{2N+1}{2^k}\times 2V_r - V_r;$$

$$X_3 = \frac{2N+2}{2^k}\times 2V_r - V_r$$

If $\varepsilon_1 > \varepsilon_3$, the decision range of $D=2N$ and $D_{k-1}=00$, which is noted as $2N(00)$ for short, would overlap with the decision range of $2N+1$ (11). If the input of ADC increases through the overlapping range in Fig. 1, for example, a D_{k-1} path is (10→11→00), the output path of ADC would be ($2N \rightarrow 2N+1 \rightarrow 2N$). In the last stage, the offset errors of the three comparators in 2bit flash ADC are independent and uncontrollable. As a result, decision range overlapping is inevitable and will cause non-monotonicity in the conventional 1.5bit/stage architecture.

3 Converter architecture

To avoid this non-monotonicity, improved last stage architecture of the pipelined ADC is proposed in Fig. 2. The flash ADC is substituted by a typical pipelined stage to output 2bit and an extra comparator which is used to introduce a redundant bit. Because the decision levels are only determined by the threshold of the extra comparator, the non-monotonicity of the ADC could be entirely eliminated by a digital-correction when the offsets of comparators are less than $1/4V_r$. Assuming that the decision level of the last comparator is δ_c, then we can rewrite Eqs. (1), (2) and (3):

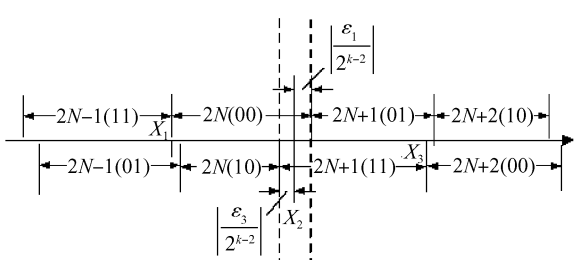

Fig. 1 Decision levels and output code

Combining Eqs. (1) ~ (3), one can derive the input decision ranges from the output code of the whole ADC and the last stage,

$$V_i(k) = V_o(k-1) = 2^{k-1}V_{in} - [2^{k-2}D_1 + \cdots + D_{k-1} - (2^{k-2} + \cdots + 1)]V_r \quad (5)$$

$$\begin{cases} D_k = 0 \Rightarrow V_i(k) < \delta_C \\ D_k = 1 \Rightarrow V_i(k) \geqslant \delta_C \end{cases} \quad (6)$$

$$D = 2^{k-1}D_1 + 2^{k-3}D_2 + \cdots + 2D_{k-2} + D_{k-1} + D_k \quad (7)$$

If the output code of whole ADC is N. we can get from the above three equations:

$$\begin{cases} D=N, D_k=0 \Rightarrow V_{in} < \frac{N+1}{2^k}\times 2V_r - V_r + \frac{\delta_C}{2^{k-1}} \\ D=N, D_k=1 \Rightarrow V_{in} \geqslant \frac{N}{2^k}\times 2V_r - V_r + V_r + \frac{\delta_C}{2^{k-1}} \end{cases} \quad (8)$$

It can be seen that there is no overlapping area in the decision range, the digital output increases one by one when the ADC input signal increases, so the non-monotonicity of ADC is entirely eliminated. Figure 2 compares the simulation results of the conventional architecture and the improved architecture and shows an up-to-5dB improvement of SNR achieved by eliminating the non-monotonicity of the pipelined ADC.

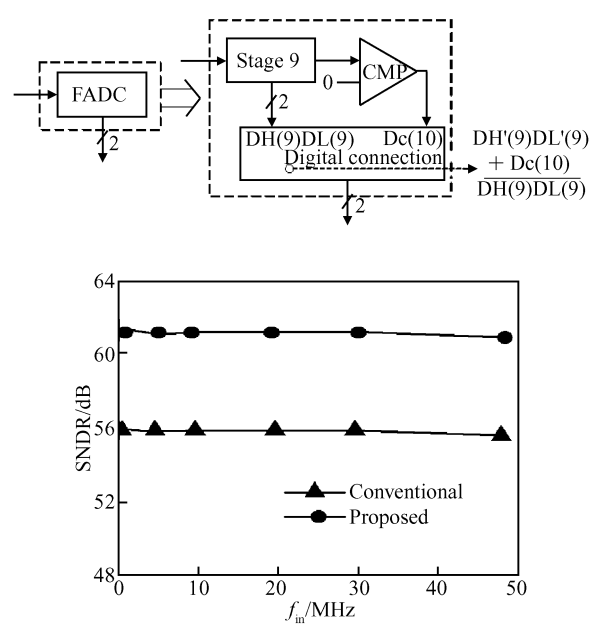

Fig. 2 Proposed architecture and simulation results

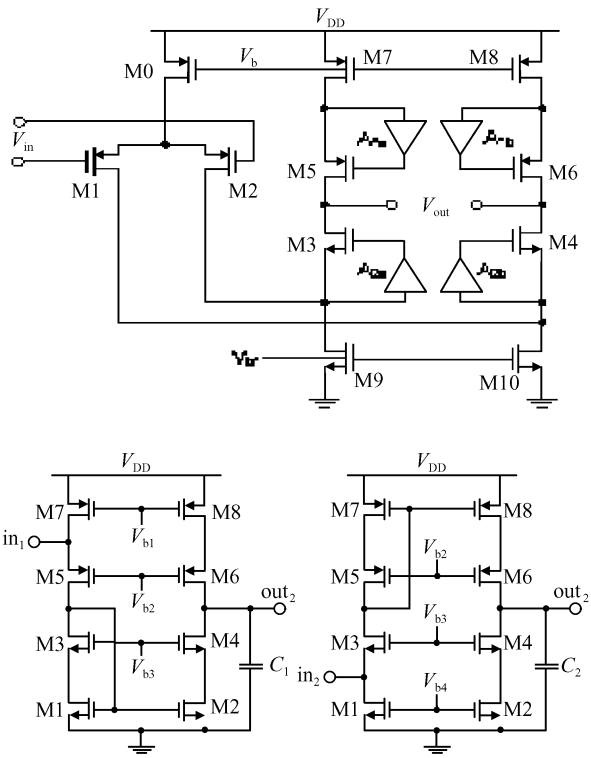

Fig. 3　Gain boosting folded cascade opamp

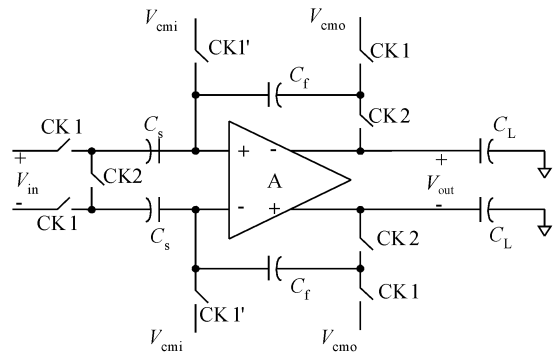

Fig. 4　Sample and hold architecture

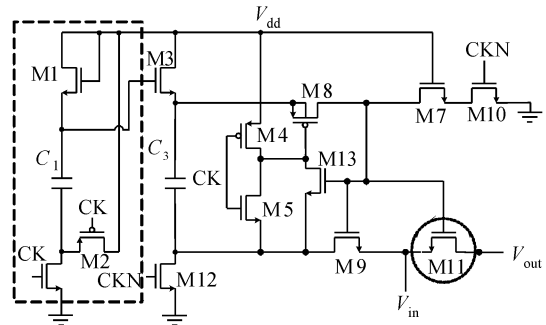

Fig. 5　Bootstrapped input sampling switch

4　Circuit implementation

4.1　Opamp

Single-stage folded cascode OPAMP is used in SHA and other pipelined stages to obtain excellent bandwidth and output swing for low voltage application. As shown in Fig. 3, two gain-boosting feedback amplifiers are used to increase the output impedance of the folded cascode amplifier. In order to minimize the output swing reduction caused by the additional amplifiers, the input voltages of the two regulation current amplifiers are adopted to equalize $V_{DD} - V_{dsat-p}$ or V_{dsat-n}. The compensation capacitors C_1 and C_2 at the output of the two additional amplifiers eliminate the extra zeros introduced by the additional amplifiers. The simulation results show that the OPAMP has a DC gain of 95dB and unity gain bandwidth of about 860MHz with a 2pF capacitance load.

4.2　SHA and bootstrapped switch

Sample and hold (SHA) circuit is shown in Fig. 4. The input and output common mode voltages can be adjusted by the values of V_{cmi} and V_{cmo}, respectively, for different input common mode levels. In order to deal with high input swing and reduce signal distortion, the gate-source voltage of the input switches has to be boosted to a fixed voltage independent of input signal. A bootstrapped, high swing MOS switch[5] is employed in this SHA, which is shown in Fig. 5. When CK is high, the voltage of C_1 is pre-charged to $V_{DD} - V_t$, where V_t is the source-gate voltage of M1. In the next phase, the bottom plate of C_1 connects to V_{DD} and the top plate of C_1 pre-charged to $2V_{DD} - V_t$, which turns M3 on and charges C_3 to V_{DD}. When M3 is off, the voltage of C_3 keeps the gate-source voltage of the switch M11 to a fixed voltage. Only one capacitor is used in this boosting circuit (dotted box), which results in a smaller area than a clock multiplier in the conventional design.

5　Prototype measurements

The prototype ADC was fabricated in a 0.18μm CMOS process. Capacitors were implemented using metal-insulator-metal (MIM) structures. The die photo is shown in Fig. 6. The ADC occupies an active die

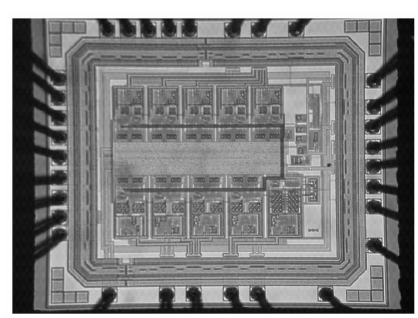

Fig. 6　Die photograph

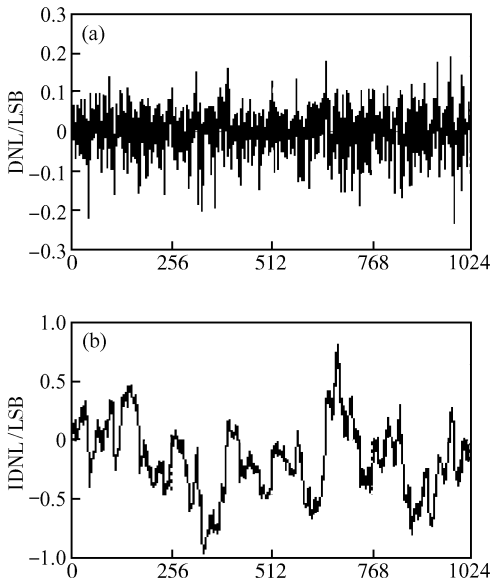

Fig. 7 Measured DNL and INL

area of 0.76mm^2 and dissipates a power of 126mW at a supply voltage of 1.8V and a sampling rate of 100MS/s.

The measured DNL and INL profiles are shown in Fig. 7. The maximum DNL is 0.3 LSB and the maximum INL is 1.05 LSB. The dynamic performance of the ADC was characterized by analyzing a fast Fourier transform (FFT) of the output code input. The measured signal-to-noise-and-distortion (SNDR) is about 57.4dB with a 5MHz input, equivalent to 9.23 effective numbers of bits (ENOB). Under the same condition, the signal-to-noise (SNR) is about 58.6dB, the spurious free dynamic range (SFDR) is about 68.5dB, the total of harmonic distortion (THD) is −63.3dB. The measured dynamic performance versus input frequency is shown in Fig. 8. The measured performance of the prototype ADC is summarized in Table 1.

6 Conclusion

A 10bit 100MS/s pipelined ADC is designed and fabricated in a 0.18μm mixed signal CMOS technology. An improved 1.5bit/stage pipelined architecture has been used in this work to eliminate non-monotonicity of the traditional pipelined ADC architecture.

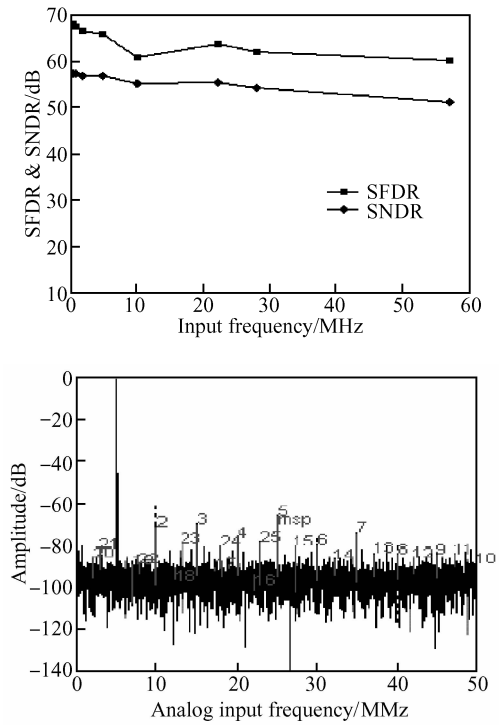

Fig. 8 SNDR/SFDR versus input frequency

Table 1 Summary of ADC performance

Resolution	10bit
Conversion rate	100MHz
Technology	0.18μm CMOS
Power supply	1.8V
Total power	126mW
DNL/INL	0.3LSB/1.05LSB
SNR/SNDR/SFDR	58.6dB/57.4dB/68.5dB(f_{in} = 5MHz) 54.3dB/52.4dB/59.8dB(f_{in} = 57MHz)
THD	−63.3dB(f_{in} = 5MHz)
ENOB	9.23(f_{in} = 5MHz)
Area	0.74mm^2

References

[1] Park Y I, Karthikeyan S, Tsay F, et al. A 10b 100MSample/s CMOS pipelined ADC with 1.8V power supply. IEEE ISSCC Dig Tech Papers, 2001, 439: 130

[2] Oh T H, Yoo S M, Moon K H, et al. A 3.0V 72mW 10b 100 MSample/s Nyquist-rate CMOS pipelined ADC in 0.54mm^2. IEEE ISCAS, 2006

[3] Li J, Moon U K. A 1.8-V 67-mW 10-bit 100-MS/s pipelined ADC using time-shifted CDS technique. IEEE J Solid-State Circuits, 2004, 39: 1468

[4] Lewis S H, Fetterman H S, Gross G F, et al. A 10-b 20-MS/s analog-to-digital converter. IEEE J Solid-State Circuits, 1992, 27: 351

[5] Abo A, Gray P. A 1.5-V 10-bit 14.3-MS/s CMOS pipeline analog-to-digital converter. IEEE J Solid-State Circuits, 1999, 34: 599

采用改进型 1.5 位/级结构的 10 位 100MHz 流水线模数转换器*

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摘要：介绍了一个采用改进型 1.5 位/级结构的 10 位 100MHz 流水线结构模数转换器.测试结果表明,模数转换器的信噪失真比最高可以达到 57dB,在 100MHz 输入时钟下,输入信号为 57MHz 的奈奎斯特频率时,信噪失真比仍然可以达到 51dB.模数转换器的差分非线性和积分非线性分别为 0.3LSB 和 1.0LSB.电路采用 0.18μm 混合信号 CMOS 工艺实现,芯片面积为 0.76mm^2.

关键词：模数转换器；流水线结构；改进型 1.5 位/级结构

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