A Fully-Integrated Dual Band CMOS Power Amplifier Based on an Active Matching Transformer*

Jin Boshi†, Wu Qun, Yang Guohui, Meng Fanyi, and Fu Jiahui

(*Department of Electronic & Communications Engineering, Harbin Institute of Technology, Harbin 150001, China*)

Abstract: We propose a dual band CMOS power amplifier for mobile WiMAX systems. The power amplifier, combined with an active matching transformer, is fully integrated and fabricated in a 0.13μm CMOS process. The transformer operates at dual bands with active matching circuit. The measured result shows that the transformer efficiency of 78.2% and 70.4% at 2.5 and 3.5GHz are realized, respectively, and 26.5 and 24.8dB gain are achieved. The PAE reaches 20% and 28% at 2.5 and 3.5GHz, respectively. The third inter-modulation (IM3) is lower than −30dBc at the 25dBm average power.

Key words: RF CMOS; power amplifier; transformer; WiMAX
EEACC: 2570D
CLC number: TN432 **Document code**: A **Article ID**: 0253-4177(2008)11-2204-05

1 Introduction

As communication technology advanced in recent years, wireless communication systems have raised a great demand on multi-band systems. For cost-effectiveness, the design of the multi-band subsystem has become one of the hot technique trends. Especially, CMOS power amplifiers try to compete with the GaAs based technologies in some advanced areas. Even though few products can be purchased in the market, the samples in the laboratory are becoming more mature and promising. To solve the shortcomings of CMOS power amplifiers, a differential configuration is widely used to offset the harmonics and the effect of source inductance, but an obstacle is to design a proper transformer to combine the power at the output end[1~3]. For the transformer, the low loss, high impedance transformation ratio, and compact size are required.

In this paper, a dual band transformer with impedance transformation is first analyzed with even and odd mode theory. Using the additional lumped components for matching, the size of the transformer is reduced greatly, and tuning the capacitance automatically at the output end with a transistor switch, the transformer matches at the dual operating frequency. Second, we develop a CMOS power amplifier combined with a dual band transformer that is applied for mobile WiMAX system demonstration. The linearity is a little tight at average power, but still can satisfy the WiMAX linearity basically.

2 Dual band transformer design

An ideal transformer is a three-port device and should satisfy the following relations in an S parameter system,

$$S_{21} = -S_{31} \tag{1}$$

$$S_{11} = 0 \tag{2}$$

In order to analyze the transformer with even and odd mode theory, first, we need transform the three-port S matrix to four-port S matrix system, and then we can use S parameters of the four-port S matrix to express a three-port S matrix easily, where S_{mn} and S'_{mn} are defined as the S parameter of the three-port and four-port S matrix, and $m, n = 1, 2, 3,$ or 4[1].

$$S_{11} = S'_{11} - \frac{S'_{14}S'_{41}}{(1+S'_{44})} \tag{3}$$

$$S_{31} = S'_{13} - \frac{S'_{14}S'_{43}}{(1+S'_{44})} \tag{4}$$

$$S_{21} = S'_{12} - \frac{S'_{14}S'_{42}}{(1+S'_{44})} \tag{5}$$

Substituting Eqs. (3)~(5) into Eqs. (1), (2) and applying even and odd mode theory on the transformer, we obtain Eqs. (6) and (7), where T_{even} is the transmission coefficient of the even mode circuit[2].

$$T_{even} = 0 \tag{6}$$

$$\frac{1}{Z_{even}} + \frac{1}{Z_{odd}} = 1 \tag{7}$$

Under the above condition, if we make the T_{even}

* Project supported by the Research Fund for the Doctoral Program of Higher Education of China
† Corresponding author. Email: bsjin@postech.ac.kr
Received 19 June 2008

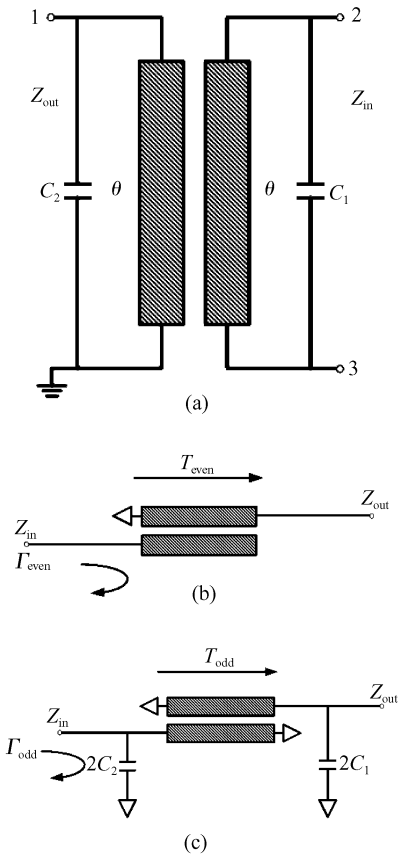


Fig. 1　Semi-lumped transformer with even mode and odd mode (a) Semi-lumped transformer; (b) Even mode circuit; (c) Odd mode circuit

stop and the even and odd modes impedance match simultaneously, it will operate as a transformer.

The proposed transformer model is shown in Fig. 1. The merits of this model is that it always presents the T_{even} stop in Eq. (6) and we can shorten the length of the transmission line by adding some capacitors at the input and output to satisfy the conditions in Eq. (7). Then it will operate as the transformer.

By deriving the admittance of the even and odd mode circuit continually, we get the even and odd mode admittance Y_{oe} and Y_{oo} implicit function with the C_1, C_2, θ, ω, Y_{in} and Y_{out} as independent variables in Eqs. (8) and (9), where C_1, C_2 are the input and output capacitors, θ is the electrical length, ω is the operation frequency, and Y_{in} and Y_{out} are the input and output impedance. All the design factors are included in the functions. By adjusting C_1 and C_2, we can reduce the electrical length to realize it on the chip level under the condition of $Y_{in} = 10\Omega$ and $Y_{out} = 50\Omega$, which is shown in Fig. 2. Furthermore, if we select the proper different capacitance to match at the different frequency point, we can make the transformer operate at dual frequency band.

$$Y_{oe} = f_1(C_1, C_2, \theta, \omega, Y_{in}, Y_{out}) \quad (8)$$

$$Y_{oo} = f_1(C_1, C_2, \theta, \omega, Y_{in}, Y_{out}) \quad (9)$$

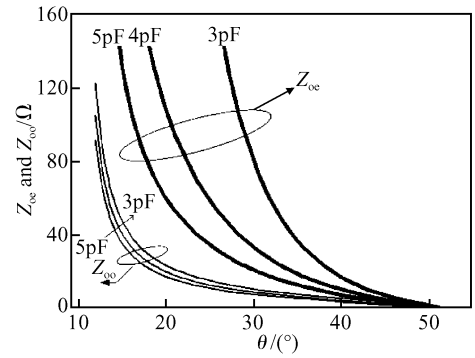


Fig. 2　Z_{oo} and Z_{oe} versus θ

The model of the dual band transformer with active matching is shown in Fig. 3 (a). To realize the matching at the output with different capacitances, we design the switch using a transistor. By making it operate at the on and off state, respectively, we can switch between the different capacitances and realize the matching at different frequency bands. When the switch is in the off state, the DC bias is 0V and the equivalent capacitance is $C_{21} \parallel C_{22}$, which is matched at 3.5GHz; when the transistor is in the on state, the DC bias is 3V, the capacitor C_{22} is shorted, and the equivalent capacitance equals C_{21}, which is matched at 2.5GHz, where the $C_{21} = 4.04$pF and $C_{22} = 8.78$pF. The matching impedances are shown in Fig. 3 (b). Because of the on-resistance of the transistor, the parasitic resistance of the capacitor is increased, which increases the loss of the transformer, but it can be reduced at the cost of a larger transistor.

3　Schematic design

3.1　Cascode configuration

Because of the low transconductance of the CMOS transistor, in order to offer enough gain, the cascode configuration is popular in the CMOS power amplifier design. The upper transistor of the common gate configuration can offer higher output impedance and improve gain, thus 25dB gain can be offered only by two stages instead of complex three stages, which is shown in Fig. 4 (a). But this topology has a burden

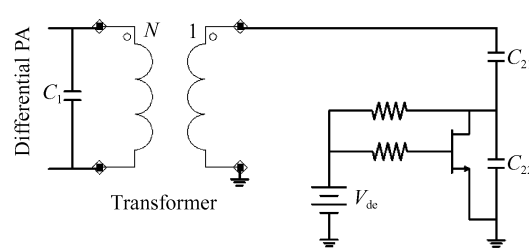


Fig. 3　(a) Schematic of dual-band transformer; (b) Matching impedances on the Smith chart

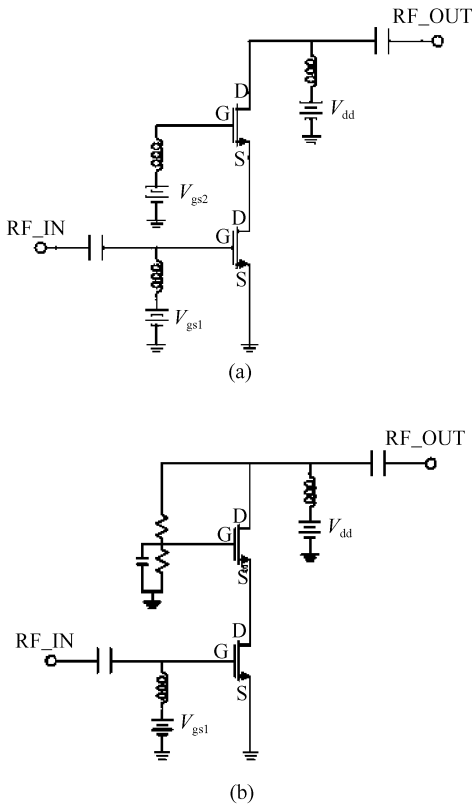


Fig. 4 Cascode amplifier (a) Traditional cascode amplifier; (b) Self-biased cascode amplifier

of gate-oxide breakdown and generates lots of nonlinear harmonics. For improving this, we utilize the self-bias configuration shown in Fig. 4 (b), and the upper device utilizes a self-bias circuit. It can adjust the gate bias voltage of the upper nMOS and evenly divide the drain bias for the upper and lower transistor. Thus not only the uneven dividing of drain bias is avoided but also the lowering the burden of gate-oxide breakdown and the hot-carrier degradation[3~5]. The parameters of the transistor are selected carefully to consider the breakdown voltage for both the transistor and the linearity. The finger length of the upper transistor is 0.28μm with the thick oxide nMOS model to enhance the breakdown voltage pressure and the lower transistor is 0.13μm with the thin oxide nMOS model to maximize the transconductance. The finger width of the upper and lower transistor is selected as 6 and 3μm with the consideration of the small signal performance. The number of fingers is 30 for both. The power cell and driver cell have the same parameters except the number of unit transistors. The power cell has 32 units, and the driver cell has 5 units. All the interconnection lines are simulated with a 2.5D EM simulator.

3.2 Input and inter-stage matching

The input balun usually offers enough bandwidth to cover the target bands, but because the input impedance changes with the frequency, we have to design the resonant circuit to make it match at different operation bands. The design is very similar to filter design, to make the input impedance match the conjugate.

The case of inter-stage matching is different from the input matching, because the output of the first stage requires the power match but the input matching requires the conjugate match. Thus it is different from the "filter design." For the input matching case, in this project, we use the different length of bonding wire series with the fixed capacitance for matching. For the real case, we can replace it with the varactor to control the matching capacitance[6].

3.3 Schematic design

The schematic and layout are shown in Figs. 5 (a) and 5 (b), in which all the components are fully integrated including the input balun, output transformer, and matching circuits. The drain bias of the power stage and second harmonic tuning utilizes the DC virtual ground of the transformer. The size of layout is 1.2mm × 2.0mm including pads. All of the matching components, including the input and output balun are fully integrated. The area of the transformer is 1.2mm × 0.6mm including the active matching switch. The transformer itself is only 0.7mm × 0.25mm, which is one of the most compact transformers reported. The metal of the signal line and transformer are 3.3μm copper, which employ the top layer in the process[7].

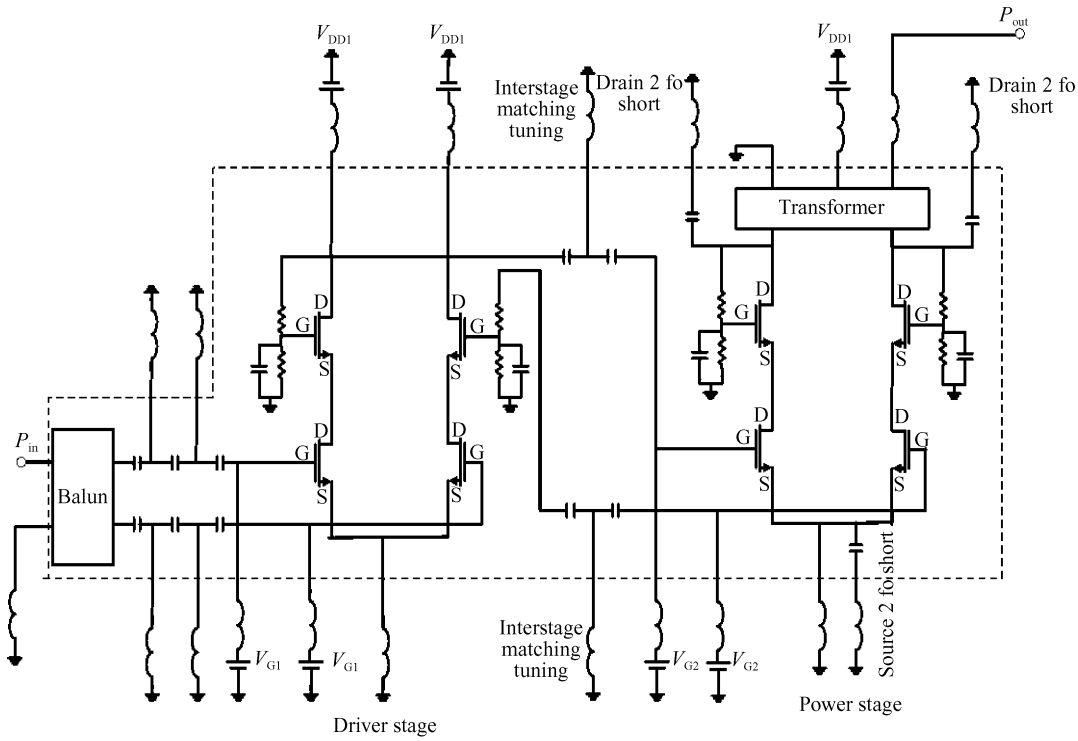
4 Measurement

4.1 Transformer measurement

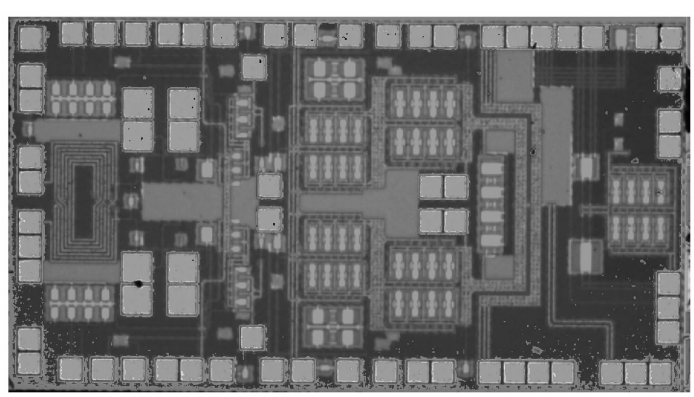
The loss of the transformer is measured by a network analyzer HP 8517B system independently. We cut the connection between the power cell and transformer and utilize the pads around the power cells (the layout is shown in Fig. 5(b)). The transformation efficiency is 78.2% and 70.4% at 2.5 and 3.5GHz. Compared with the off-chip matching, the efficiency is lower because of the on-resistance of the transistor, and we can reduce it further at the cost of a larger transistor.

4.2 Power amplifier measurement

The drain bias is 2.5V, and the gate bias of the power stage and driver stage are 0.35 and 0.45V. The losses of bonding-wires and evaluation printed circuit board interconnections are included in the measure-



(a)



(b)

Fig. 5　Dual-band CMOS power amplifier

ment. Figure 6(a) shows the measured gain and PAE versus output power. The gains are 26.5 and 24.8dB at 2.5 and 3.5GHz, respectively. The PAE are 20% and 28% at P1dB, respectively. The gain and PAE are 3dB and 10% lower than expectation because the quality factor of the interconnection lines in the real case is lower than the 2.5D EM simulator.

Figure 6 (b) shows the measured linearity with a

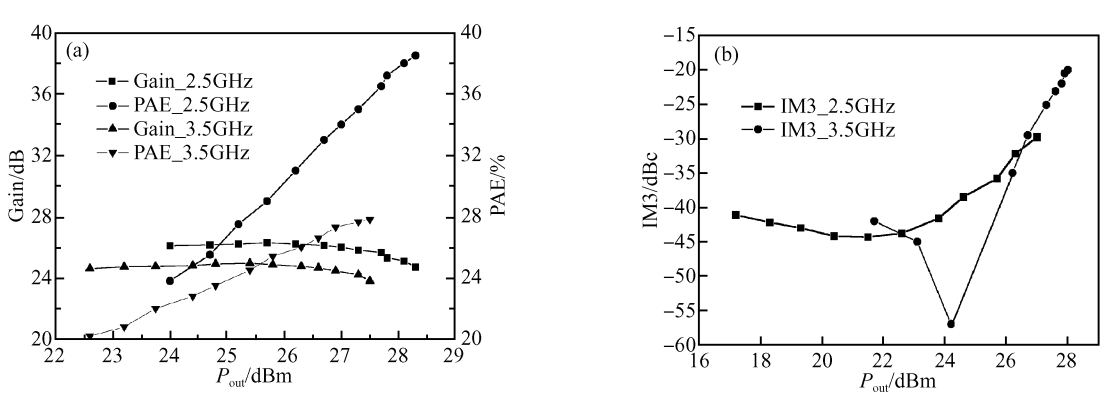


Fig. 6　Measurement of CMOS power amplifier　(a) Gain and PAE; (b) Third inter-modulation

5MHz two-tone signal. IM3 is lower than −30dBc at the 25dBm average power and can satisfy the linearity basically, and it should be verified further with the mobile WiMAX spectrum analysis, but the spectrum mask was not available in this experiment.

5 Conclusion

In this paper, a 2.5 and 3.5GHz dual band operation RF CMOS power amplifier is designed, which is applied on a mobile WiMAX system demonstration. The operation of the dual band transformer is implemented with the active matching circuit at the output port. The efficiency of the transformer is 78.2% and 70.4% at 2.5 and 3.5GHz and can be improved with a larger transistor. The gain and PAE can achieve 26.5 and 24.8dB, 20% and 28% at 2.5 and 3.5GHz, respectively. The IM3 are lower than −30dBc at the 25dBm average power for both cases.

References

[1] Ahn H R. Asymmetric passive components in microwave integrated circuits. New York: John Wiley & Sons, 2006

[2] Ang K S, Leong Y C, Lee C H. Analysis and design of miniaturized lumped-distributed impedance-transforming baluns. IEEE Trans Microw Theory Tech, 2003, 51: 1009

[3] Kang J, Yang Y, Kim B. Highly linear and efficient differential CMOS power amplifier with harmonic control. IEEE J Solid-State Circuit, 2006, 41(6): 1314

[4] Park K Y, Kim C, Hong H. CMOS RF power amplifier with reconfigurable transformer. Electron Lett, 2006, 42(1): 405

[5] Park C, Han J, Kim H, et al. A 1.8-GHz CMOS power amplifier using a dual-primary transformer with improved efficiency in the low power region. IEEE Trans Microw Theory Tech, 2008, 56: 782

[6] Jou C F, Cheng K H, Lin C M, et al. Dual band CMOS power amplifier for WLAN applications. Proceedings of the 46th IEEE International Midwest Symposium on Circuits and Systems, 2003, 3: 1227

[7] Aoki I, Kee S D, Rutledge D B, et al. Fully integrated CMOS power amplifier design using the distributed active-transformer architecture. IEEE J Solid-State Circuits, 2002, 37(2): 371

基于有源匹配转换器的全集成双频带射频 CMOS 功率放大器的设计*

金博识† 吴 群 杨国辉 孟繁义 傅佳辉

(哈尔滨工业大学电子通信工程系，哈尔滨 150001)

摘要：设计了基于有源转换器的双频带射频 CMOS 功率放大器，该放大器可以应用于移动 WiMAX 系统. 设计采用了 0.13μm CMOS 工艺并且所有的匹配完全集成在芯片内. 转换器可以通过有源匹配而在双频带工作，在 2.5 和 3.5GHz，转换器的效率为 78.2%和 70.4%，功率放大器的增益分别为 26.5 和 24.8dB，功率增加效率为 20%和 28%，在平均功率 25dBm 处，三阶交调系数均低于 −30dBc.

关键词：射频 CMOS；功率放大器；转换器；WiMAX

EEACC：2570D

中图分类号：TN432 **文献标识码**：A **文章编号**：0253-4177(2008)11-2204-05

* 高等学校博士学科点专项科研基金资助项目

† 通信作者. Email: bsjin@postech.ac.kr

2008-06-19 收到