Design and implementation of a high dimming ratio LED drive controller*

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Abstract: This paper presents a high dimming ratio light emitting diode (LED) drive controller chip with digital mode dimming (DMD). The chip is composed of a boost power converter and a dimming control block. A novel constant on time (COT) control strategy is proposed for boost converter to achieve high dimming ratio. In addition, a fast enough load transient response of the converter power stage ensures its high dimming ratio. The COT control circuit operates mainly based on two current-capacitor timers and a finite state machine (FSM). The LED drive controller chip is designed and fabricated in 1.5 μm bipolar CMOS-DMOS (BCD) process with a die area of 1.31×1.43 mm^2. Experimental results show that the proposed LED drive system works well. And, as expected, the minimum LED dimming on time of 1.0 μs and the corresponding dimming ratio of 1000 : 1 at 1 kHz dimming frequency are successfully achieved.

Key words: BCD process; boost converter; COT control; LED drive; high dimming ratio
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1. Introduction

Recently, as an environmentally friendly light source, the light emitting diode (LED) is more widely adopted in lighting and display systems. And in these applications, high and adjustable brightness of the LED is usually demanded.

However, the maximum brightness of a single LED is limited by current density and heat generation. In some cases, several LEDs are connected in series to get sufficient brightness. Since the forward voltage of a high power LED are typically ranging from 2.8 to 3.6 V, the total forward voltage of an LED string could be higher than the output voltage of most power supplies. Thus, boost power converters are widely adopted in LED drive systems.

As to brightness adjusting, analog mode dimming (AMD) is a conventional choice. However, it may give rise to a color shift issue because in AMD mode the brightness is adjusted by changing LED current density or current amplitude[1]. Another problem of AMD is that the analog control signal is hard to get. For example, in AMD mode, a DA converter will be needed for accurate brightness control, which increases the system complexity and cost. In contrast, the digital mode dimming (DMD) has been proven an effective way to alleviate these issues[1, 2], because it is implemented by pulse width modulation of LED current while the current amplitude is kept constant. Thus, in DMD mode the LED brightness is proportional to the duty cycle of the dimming control signal. Moreover, the PWM dimming control signal is easy to realize with a DSP or a microcontroller. As a result, DMD is preferable in most LED lighting systems.

LED with high dimming ratio is demanded to realize a high contrast ratio display. One high diming ratio control scheme based on a boost converter is described in Ref.[2]. During the dimming-on interval, the power stage operates as a traditional current mode boost converter with output current feedback. During the dimming-off internal, the inductor peak current information is saved on a capacitor, and the boost power switch is turned off in order to prevent excessive power transfer from the inductor to the output capacitor under the unloaded condition. Limited by the time of the inductor current recovery and boost switch turn on delay[3], the minimum dimming-on interval should be longer than three to four switching cycles, which decides the highest achievable dimming ratio.

In this paper, a high dimming ratio LED drive scheme is proposed. It features no minimum dimming-on interval limits mentioned above and works on the basis of a COT boost converter.

2. System constitution

Figure 1 shows the proposed high power LED drive system. It consists of a COT controlled boost power stage and a dimming control block, which is mainly an OTA.

When the DIM signal is high, the dimming switch SW_2 is turned on, and the OTA senses the current I_{LED} flowing through the LED string and outputs the error signal V_{CTRL} into the load capacitor C_{VTH}. V_{CTRL} is then used to set the power stage reference. The boost power stage is assembled by external power devices, and it works like a voltage-controlled-voltage-source (VCVS) to generate the corresponding output voltage V_{OUT}. When the DIM signal goes low, SW_2 is switched off and cuts off I_{LED}. At the same time, the sample-hold switch SW_1 is also switched off to make the control signal V_{CTRL} be held by C_{VTH} during dimming off interval. Therefore, the main feature of this dimming control scheme is that the output

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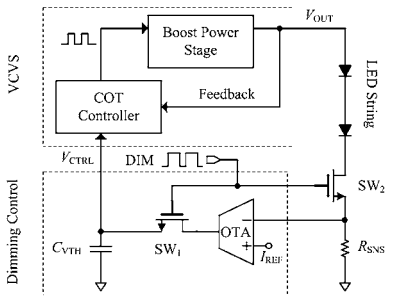

Fig.1. Block diagram of the proposed LED drive system.

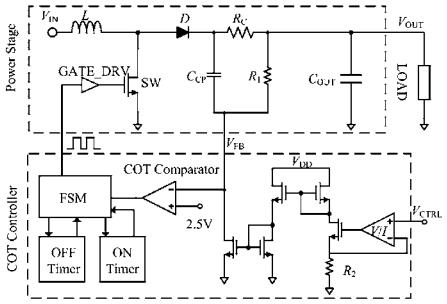

Fig.2. Schematic of the COT boost converter.

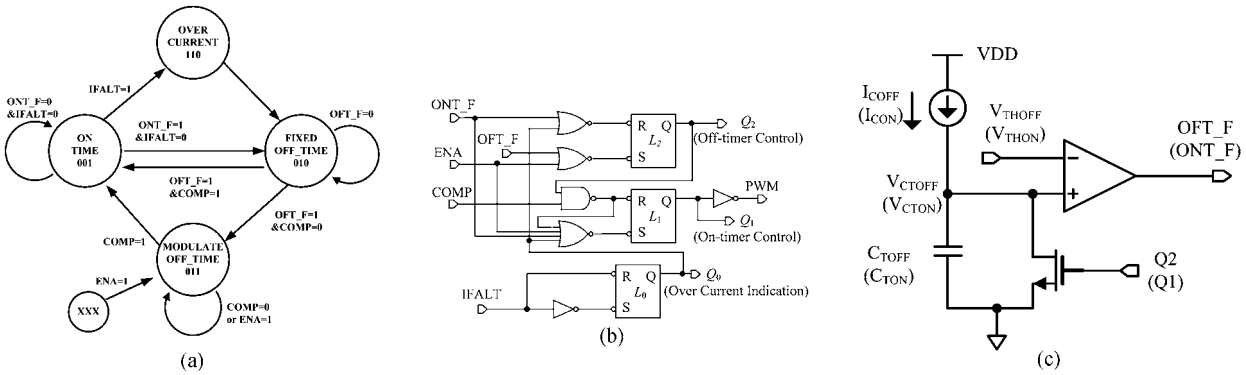

Fig.3. COT logic: (a) COT state-chart; (b) Synthesized of the control FSM; (c) Simplified circuit scheme of the off timer.

voltage is always maintained to supply the regulated LED current and avoid the problems in Ref.[2].

It should be noted that to realize the proposed LED control scheme, the load transient response of the power stage must be fast enough since at the turning-on instant of the LED string, the faster the load transient response of a boost converter is, the less the LED current settling time will be. Traditional current mode and voltage mode control boost power converter incorporates a right half plane zero in the control to output transfer function, which complicates the compensation loop design and limits the system bandwidth[4, 5]. Hysteretic control is considered to have the fastest load transient response so far. In addition, it usually does not require additional compensation loop. However, due to its discontinuous output current, it is more difficult for boost converter to implement traditional hysteretic control than for buck one. Some efforts were put into the research on hysteric boost converters such as that reported in Refs.[6, 7]. Those proposed systems are quite complex so that they are not widely adopted in practice.

In this paper, an easy-realized COT control scheme is proposed to control the boost converter. It provides an alternative way to the design of a fast load transient boost type voltage regulator.

3. Circuit design of COT controller

3.1. Principal of COT control

Figure 2 shows the block diagram of the proposed COT boost converter.

During continuous conduction mode (CCM), feedback voltage V_{FB} is compared with a fixed 2.5 V reference. If V_{FB} is below 2.5 V, the power switch SW is turned on and lasts a predefined time T_{ON}. Then SW is turned off. The off state duration of SW, T_{OFF}, is determined by the longer one of two time intervals: one is the time length of the off-timer, and the other is the time when V_{FB} drops below 2.5 V. The discontinuous conduction mode (DCM) can be analyzed in the same way. The only difference between them is that in DCM operation, the inductor current has reached zero when the next T_{ON} is triggered.

For the feedback structure, traditional resistor divider attenuates the ripple signal which is necessary for off time modulation. To avoid this effect, a current sink based feedback structure is adopted. Figure 2 shows its structure. V_{CTRL} signal that is given by the OTA is applied to a voltage to current (V/I) converter with a transconductance of $1/R_2$, then the corresponding output current is used to bias the DC current in R_1. At the same time, the gain of V_{CTRL} to V_{OUT} is also determined. As the feedback node (inverting input of the comparator) now becomes high impendence, a C_{CP} with several hundred picofarads is big enough to couple the ripple voltage without significant amplitude attenuation. Because the off time is still modulated in hysteretic way, the COT control maintains the fast transient response with a much simpler current sensing method compared with hysteretic control.

3.2. COT logic implementation

As indicated in the state-chart of Fig. 3 (a), five circuit states exist in COT control logic. To reduce the scale of combination logic, three output signals Q_0, Q_1, Q_2 are used to realize the COT FSM. Here Q_0 indicates the over current state, and Q_1 and Q_2 controls the on-timer and off-timer respectively. For

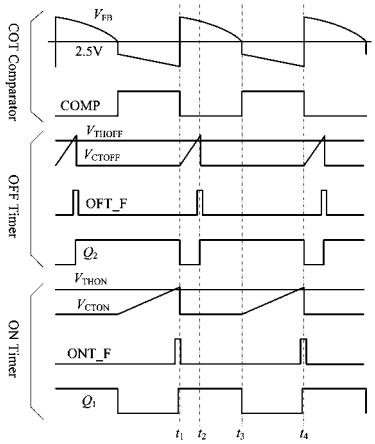

Fig.4. Key waveforms of the COT logic in CCM.

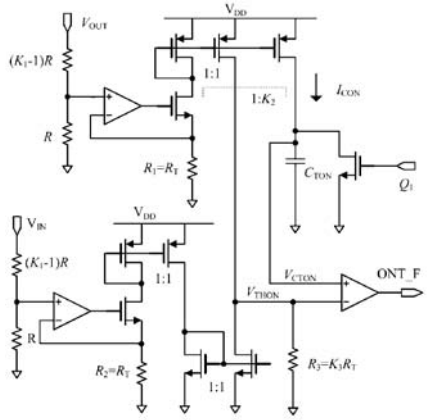

Fig.5. Proposed on time generator for CCM frequency control.

example, $Q_0Q_1Q_2 = 110$ corresponds to the over current state. Figure 3 (b) is the synthesized FSM based on three NAND RS latches L_{0-2}. The conceptual structure of the off-timer is shown in Fig. 3 (c), and the net or device names in bracket are the on-timer which has the similar structure with the off-timer.

Figure 4 gives the waveforms of the COT logic state transition during CCM operation while no over current occurs. From t_1 to t_2, the off-timer is timing, and the FSM is in state "010". Once the voltage on the capacitor of the off-timer reaches V_{THOFF}, the output of OFT_F will become high and set Q_2 through port S of L_2. Because COMP is low at the same time, Q_1 will remain high and the FSM consequently runs in state "011". State "011", the off time modulation state, lasts till COMP signal goes high and reset Q_1 through port R of L_1 at instant t_3 when V_{FB} is lower than V_{CTRL}. And during the following state "001", the boost switch is turned on and the on-timer starts timing until V_{CTON} reaches V_{THON}, at which ONT_F goes high and subsequently reset Q_2 through port R of L_2 and set Q_1 through port S of L_1 respectively. And the FSM goes to state "010", i.e. fixed off time state, again. Other state transitions can be analyzed in the similar way.

3.3. CCM frequency control

If the on time is fixed, regardless of the variation of the input voltage and different output voltage specifications, the operation frequency of this converter will vary, which complicates the output filter design under a specific output ripple.

Suppose the expected period of the boost converter switching is T_S, the relationship between T_S and T_{ON} is

$$T_S = T_{ON}\frac{V_{OUT}+V_D}{V_{OUT}+V_D-V_{IN}} \approx T_{ON}\frac{V_{OUT}}{V_{OUT}-V_{IN}}. \quad (1)$$

Here V_D is the boost rectifier diode forward voltage and can be neglected while it is much less than $V_{OUT} - V_{IN}$. Equation (1) reveals that if a constant T_S is expected, the T_{ON} should be proportional to $V_{OUT} - V_{IN}$ and inversely proportional to V_{OUT}. Since the timing period is proportional to the timing threshold V_{THON} and inversely proportional to the charging current I_{CON}, the simplest way to get such a T_{ON} is to make V_{THON} proportional to $V_{OUT} - V_{IN}$ and I_{CON} proportional to V_{OUT}. Figure 5 gives its circuit implementation.

In Fig.5, $V_{OUT} - V_{IN}$ is realized by subtraction of their corresponding current signal, and the threshold voltage V_{THON} for the on timer is

$$V_{THON} = \frac{K_3}{K_1}(V_{OUT} - V_{IN}). \quad (2)$$

The charging current I_{CON} is mirrored directly from the V_{OUT} through a voltage to current converter with a gain factor of K_2:

$$I_{CON} = \frac{K_2}{K_1 R_T} V_{OUT}. \quad (3)$$

From Eqs.(2) and (3), the on time period of this current-capacitor timer can be written as:

$$T_{ON} = \frac{K_3 R_T C_{TON}}{K_2}\frac{V_{OUT}-V_{IN}}{V_{OUT}}. \quad (4)$$

Substitute Eq. 4 into Eq. 1 and get the equation for the switching period as:

$$T_S = \frac{K_3 R_T C_{TON}}{K_2}. \quad (5)$$

Thus, if T_S is expected to be 1 μs, the timing parameters can be set to $R_T = 20$ kΩ, $C_{TON} = 5$ pF, $K_2 = 0.1$, and $K_3 = 1$. Resistors and capacitors at these values are suitable for integration.

4. OTA design

The OTA is used to realize LED current regulation. Thus, two features are needed by it. First, to accommodate the small feedback voltage on the current sensing resistor, the low limit of its input common mode range should be low enough. Moreover, to prevent output voltage overshoot during start up, the soft start function is necessary.

Figure 6 gives the schematics of the proposed OTA. Here the devices in dashed rectangular are external components. The basic transconductance amplifier is composed of MN_{1-4}, MP_{1-4}, T_1 and T_2. The OTA transconductance can be calculated by

$$g_m = 5\frac{I_{TAIL}}{V_T}. \quad (6)$$

V_T is the thermal voltage that is proportional to absolute temperature (PTAT). To keep a constant g_m over the wide temperature range, the tail current I_{TAIL} of the differential pair is also a PTAT current.

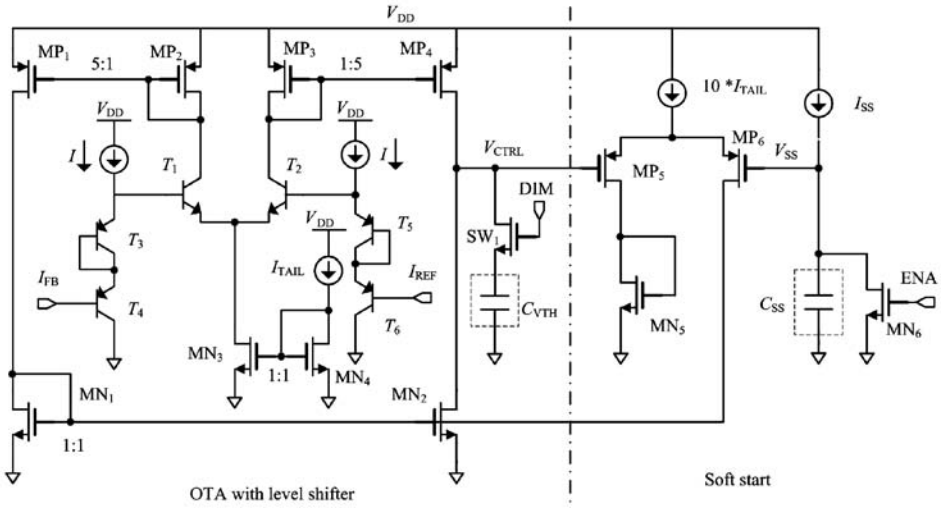

Fig.6. OTA with soft start.

To reduce the power dissipation on the LED current sensing resistor R_{SNS}, a small value R_{SNS} is preferred, which results in a small sensed voltage on it. To fit the small input common mode voltage of the OTA, a level shifter is used, which is composed of T_{3-6} and two biasing current source. The lowest input common mode voltage V_{CML} of the OTA with the level shifter is

$$V_{CML} = V_{DSAT} + V_{BEn} - 2V_{BEp}, \tag{7}$$

where V_{DSAT} is the over drive voltage of MN_3, V_{BEn} is the base-emitter voltage of T_2, and $2V_{BEp}$ is the sum of the base-emitter voltages of T_5 and T_6. The V_{CML} is a near ground common mode input voltage. Thus a small LED current sensing resistor can be used.

In order to prevent input current surge and output voltage overshoot during starting up, the control voltage of V_{CTRL} should be softly or gradually started. The soft start circuit is also shown in Fig.6. While starting up, soft start is activated once EAN goes low which means the boost converter is enabled, thenV_{SS} will rise slowly from zero, and V_{CTRL} will track this voltage by a negative feed back loop composed of MP_{4-6}, MN_1 and MN_2. In order to reduce the control error from V_{CTRL} to V_{SS}, MP_5 and MP_6 should be identically biased in DC. To do it, the bias current I_b of the soft start structure is about 10 times of I_{TAIL}, during soft starting, half of I_b current will flow through MP_5 and be mirrored to MN_2 to sink the approximately equal amount current from MP_4. And MN_5 should be of the same size as MN_1 in order to keep the same drain voltage of MP_5 and MP_6. The open loop transfer function of the soft start circuit is

$$G_{SS}(s) = -\frac{g_{mp5}}{g_{mn1}} g_{mn2}(r_{op4}//r_{on2}//sC_{VTH}). \tag{8}$$

g_{mp5}, g_{mn2}, g_{mn1} are the transconductance of the MP_5, MN_2 and MN_1 respectively,r_{op4} and r_{on2} are the small signal output resistance of MP_4 and MN_2. Equation (8) shows that the soft start circuit is with stable single pole loop.

The voltage on C_{SS} will be eventually charged to V_{DD} and the soft stat circuit will be disconnected from the OTA structure once MP_5 works in cut off region.

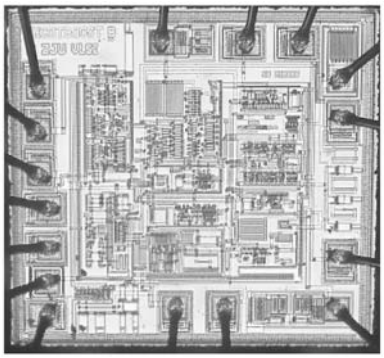

Fig.7. Chip photo.

Table 1. System parameters for simulation and test.

Description	Parameter	Value
Input voltage	V_{IN}	7–16 V
Output voltage	V_{OUT}	25 V
Output current	I_{OUT}	350 mA
Capacitance	C_{OUT}	4.7 μF Ceramic
Correction resistor	R_C	200 mΩ
Inductance	L	10 μH
Sensing resistor	R_{SNS}	0.3 Ω

5. Experimental results

The dimming controller is fabricated in 1.5 μm BCD process and the chip photograph is shown in Fig.7. And a demo board aimed to drive eight white LEDs connected in series is built. Parameters during test are listed in Table 1.

5.1. COT power stage operation

Figure 8 (a) shows the key waveforms in CCM operation. This operation mode occurs when the LED load is turned on. The upper curve is the waveform of V_{FB} ripple at the inverting input of the COT comparator, and the lower is the boost switch gate drive signal GATE_DRV. It shows that high frequency oscillation occurs at the instant of boost switch SW being turned off. To avoid abnormal trigger of the COT comparator, a fixed 160 ns off time is predefined by the off-timer so as to blank

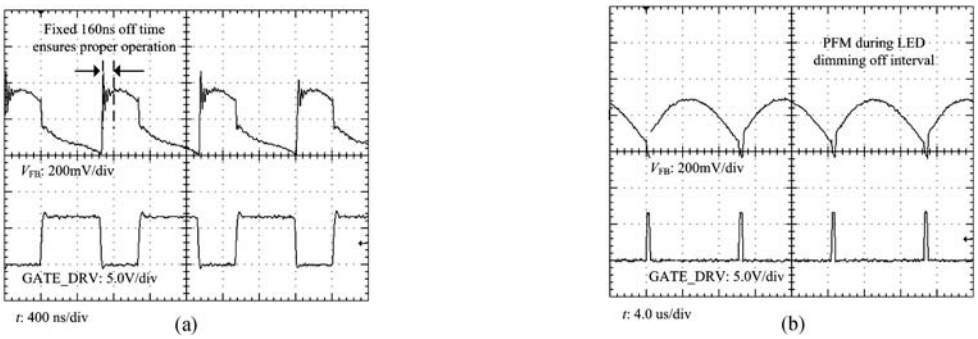

Fig.8. Feedback and gate drive signal in (a) CCM and (b) DCM operation.

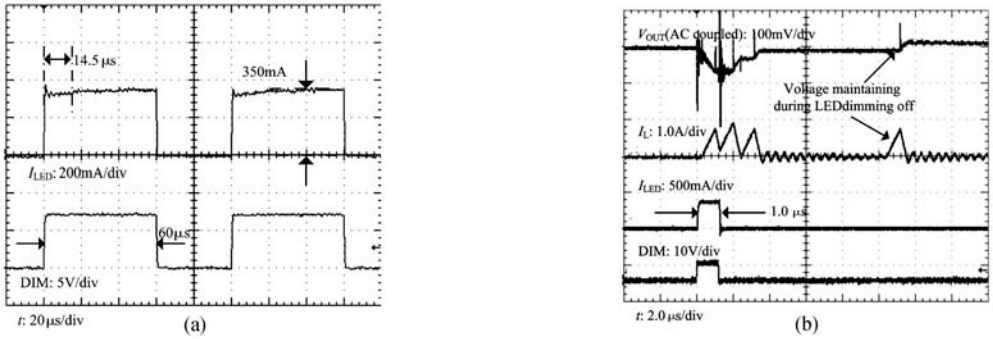

Fig.9. LED lamp dimming test: (a) Long dimming on time test; (b) Minimum dimming on time test.

this oscillation. And the switching frequency under CCM is about 960 kHz.

Figure 8 (b) shows the V_{FB} and GATE_DRV waveforms in deep DCM operation, which corresponds to the state of turning off the LED load. The operation frequency is reduced to about 100 kHz, which is much lower than that in CCM operation. The automatic PFM operation is effective to improve the light load efficiency of the proposed LED drive system.

5.2. LED dimming characteristic

Figure 9 (a) shows the waveforms in case of long dimming on interval. Here the dimming on interval is set to about 60 μs. DIM is the dimming control signal and I_{LED} is the forward LED current. It can be seen that while the LED load is turned on, a less than 15 μs current setting time is achieved.

From Fig.9 (b) it can be seen that the minimum dimming on interval can be reduced to 1 μs. And in this case, the quick drop of output voltage V_{OUT} will trigger switching of SW for several cycles to restore the charge loss of the output capacitor. After the dimming on interval, the dimming switch is switched off. Then there is only leakage current at the output node, and V_{OUT} decreases slowly. However, once V_{FB} reaches the trigger point of the COT comparator, a single switching pulse will occur to maintain V_{OUT} at the controlled value for the next LED dimming on interval. The system efficiency is not affected significantly under this low operation frequency.

On the other hand, the minimum dimming on time of 1 μs means a 1000 : 1 dimming ratio under a 1 kHz dimming frequency is achieved. Compared with a 300 : 1 dimming ratio in Ref.[2] under the same dimming frequency, there is about a three times enhancement on contrast ratio with the proposed control method.

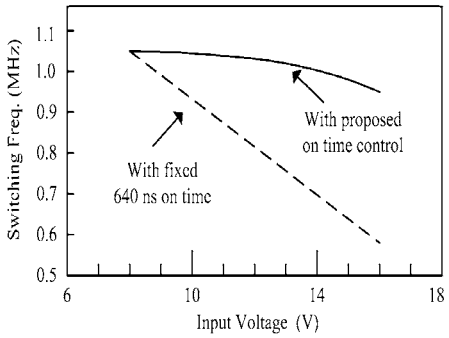

Fig.10. Operation frequency variation comparison with and without the on time control.

5.3. Output frequency control

Figure 10 gives the curve of frequency versus input voltage. It can be seen that the frequency variation with the proposed on time control is much smaller than that of with a fixed 640 ns on time one. The remained frequency variation with the proposed on time control is originated from the system non-ideality such like the parasitic resistors on the power switch and inductor. One method to improve the frequency control performance of COT buck converter is reported in Ref.[8]. And it can also be used here to get a more stable switching frequency.

6. Conclusion

A high power LED drive system with PWM dimming was proposed in this paper. It employed a novel COT control boost converter power stage. And the minimum dimming on time down to 1 μs was achieved, which corresponds to a 1000 : 1 dimming ratio at 1 kHz dimming frequency. The

LED controller was designed and fabricated in 1.5 μm BCD process with a die area of 1.31×1.43 mm^2. The experimental results demonstrated the feasibility of this control scheme.

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