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Temperature and Process Variations Aware Dual Threshold Voltage Footed Domino Circuits Leakage Management*

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Abstract: Considering the effect of temperature and process variations, the inputs and clock signals combination sleep state dependent leakage current characteristics is analyzed and the optimal sleep state is examined in sub-65nm dual threshold voltage (V_t) footed domino circuits. HSPICE simulations based on 65nm and 45nm BSIM4 models show that the proposed CLIL state (the clock signal and inputs are all low) is the optimal state to reduce the leakage current of the high fan-in footed domino circuits at high temperature and almost all footed domino circuits at room temperature, as compared to the conventional CHIL state (the clock signal is high and inputs are all low) and the CHIH state (the clock signal and inputs are all high). Further, the influence of the process variations on the leakage current characteristics of the dual V_t footed domino circuits is evaluated. At last, temperature and process variation aware new low leakage current setup guidelines are provided.

Key words: footed domino circuit; dual threshold voltage; leakage current; process variation
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1 Introduction

As the technology scales down below 65nm node, excess leakage current and variation are two of the most challenging obstacles for IC design[1,2]. With aggressive device scaling, the threshold voltage (V_t) scaling accompanies with the exponential increase in the sub-threshold leakage current (I_{sub}), which is a concern for both power consumption and noise immunity. Another challenge for technology scaling is to cope with the variation in the presence of increasing temperature and process variations. Temperature can vary significantly from one die area to another due to the unbalanced utilization and diversity of circuitry at different sections of an integrated circuit and environmental temperature fluctuations[3], thereby posing great impact on the leakage current. In addition, process variations, which are introduced during chip device fabrication steps, also have a significant effect on the leakage current[4~6].

As a common logic in high speed-performance chip design, domino circuits (dominos) can be classified into footed dominos and footless dominos [7~9]. The footed dominos have better robust characteristics because the footer isolates the pull-down network (PDN) from ground. And the footless dominos reduce both the circuit evaluation delay and the power consumption by omitting the footer.

However, both footed and footless dominos consume more leakage power compared to the static logic. To tackle the high I_{sub} problem of dominos, many circuit level approaches have been proposed including transistors stack effect[10], body-bias control[11], input vector control[12], dual V_t CMOS[13], and so on. The dual V_t CMOS technique proposed in Ref.[13] is shown to be especially efficient for dominos due to this circuit logic has the fixed transition directions. The dual V_t footless domino technique[13] is realized by assigning low V_t devices in the evaluation path while high V_t devices are used in the precharge path of the circuits. Kao *et al*.[13] indicated that a high clock signal with high inputs (CHIH) is preferable to reduce I_{sub} of a sleep dual V_t footless domino gate. Based on Kao's found, previous works in the area of footed dominos also adopt the CHIH state to reduce the leakage current of sleep circuits. These include the NMOS-sleep dominos[14], the sleep dominos[15], the low swing low power dominos[16], and so on.

Nevertheless, the CHIH sleep state produces great gate leakage current (I_{gate}) through the PDN transistors in both footed and footless dominos. In fact, I_{gate} increases exponentially with the scaling of the oxide thickness (t_{ox}). 2003 International Tech-

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nology Roadmap for Semiconductors (ITRS) predicts that oxide thickness will decrease from 1.3nm for the 65nm generation to 0.9nm for 35nm[1]. With such thin t_{ox}, accordingly, I_{gate} is becoming a significant contributor to the total leakage current as CMOS process advances to sub-65nm regime.

More recently, comprehensive analysis of the total leakage including I_{sub} and I_{gate} of footless dominos was carried out by Liu *et al*.[17]. Considering the impact of I_{gate} on the total leakage current, the study indicates that a high clock signal with low inputs sleep state (CHIL) is preferable in dual V_t footless dominos, particularly at low sleep temperature. However, for footed dominos with CHIL sleep state, the PDN exhibits great I_{sub} and the footer is in the maximum I_{gate} state. Thus, the CHIL sleep state does not solve the leakage current problem completely.

In this paper, we study the sources of leakage current in dual V_t footed dominos under temperature and process variations and propose the state with low clock signal and inputs (CLIL) to optimize the total leakage current. In addition, the robustness of dual V_t footed dominos with different sleep states to the process variations is studied and temperature and process variation aware new low leakage current setup guidelines are provided.

2 Temperature and process fluctuations induced MOSFET leakage current variation

2.1 Leakage current characteristics under temperature fluctuations

In this section, the impact of temperature fluctuations on the leakage current produced by a MOSFET is identified utilizing BSIM4 MOSFET current equations. I_{sub} and I_{gate} of a MOSFET are[18~20]

$$I_{sub} = u_{eff}\frac{W_{eff}}{L_{eff}}\sqrt{\frac{q\varepsilon_{si}N_{ch}}{2\Phi_s}}V_T^2\exp\left(\frac{V_{gs}-V_t}{nV_T}\right)\times\left[1-\exp\left(-\frac{V_{ds}}{V_T}\right)\right] \quad (1)$$

$$I_{gate} = W_{eff}L_{eff}A_g\left(\frac{V_{dd}}{t_{ox}}\right)^2\exp\left\{\frac{-B_g\left[1-\left(1-\frac{V_{dd}}{\Phi_{ox}}\right)^{\frac{3}{2}}\right]}{V_{dd}/t_{ox}}\right\} \quad (2)$$

where u_{eff}, W_{eff}, L_{eff}, V_T, ε_{si}, N_{ch}, Φ_s, n, Φ_{ox}, A_g, and B_g are effective carrier mobility, effective channel width, effective channel length, thermal voltage, permittivity of silicon, effective channel doping, surface potential, subthreshold swing, barrier height of the tunneling electron and process concerned physical parameters, respectively. And V_t and u_{eff} are given by[19]:

NMOS:

$$V_t(T) = V_t(T_0) + \left(\mathrm{KT1} + \frac{\mathrm{KT1L}}{L_{eff}} + V_{bseff}\mathrm{KT2}\right)\times\left(\frac{T}{T_0}-1\right) \quad (3)$$

PMOS:

$$V_t(T) = V_t(T_0) - \left(\mathrm{KT1} + \frac{\mathrm{KT1L}}{L_{eff}} + V_{bseff}\mathrm{KT2}\right)\times\left(\frac{T}{T_0}-1\right) \quad (4)$$

$$u_{eff}(T) = \left[U_0\left(\frac{T}{T_0}\right)^{U_{te}}\right]\left\{1+\left(\frac{V_{gsteff}+2V_t(T)}{T_{OXE}}\right)^2\times U_b(T)+(U_c(T)V_{bseff}+U_a(T))\left(\frac{V_{gsteff}+2V_t(T)}{T_{OXE}}\right)\right\}^{-1} \quad (5)$$

where KT1, KT1L, KT2, V_{bseff}, U_0, U_{te}, T_{OXE}, U_a, U_b, U_c, T_0 and T are the temperature coefficient for threshold voltage, channel length dependence of the temperature coefficient for threshold voltage, body-bias coefficient of threshold voltage temperature effect, effective substrate bias voltage, mobility at the reference temperature, mobility temperature exponent, electrical gate-oxide thickness, first order mobility degradation coefficient, second order mobility degradation coefficient, body effect of mobility degradation coefficient, reference temperature, and the operating temperature, respectively. KT1, KT1L and KT2 are constant empirical parameters while U_a, U_b and U_c are temperature dependent. These model parameter coefficients that determine the temperature fluctuation induced MOSFET leakage current variation in 65nm and 45nm CMOS technologies are listed in Table 1.

Based on these equations, we can see that as the temperature increases, I_{sub} increases significantly due to the reduction of V_t, but I_{gate} is almost insensitive to temperature. As also can be obtained, both I_{sub} and I_{gate} would increase with the upsizing of transistors. Figure 1 shows I_{sub} and I_{gate} for a 65nm NMOS device with minimum length as a function of temperature and W/L and it is clear that the simulation results match well with the analytical results.

Table 1 Temperature parameter coefficients in BSIM4 models

Model parameter	65nm		45nm	
	PMOS	NMOS	PMOS	NMOS
KT1	−0.11	−0.11	−0.34	−0.37
KT1L	0	0	0	0
KT2	0.022	0.022	−0.052	−0.042
U_{te}	−1.5	−1.5	−1.5	−1.5
U_a	4.31×10^{-9}	4.31×10^{-9}	-1×10^{-9}	1×10^{-9}
U_b	7.61×10^{-18}	7.61×10^{-18}	2×10^{-18}	-3.5×10^{-19}
U_c	-5.6×10^{-11}	-5.6×10^{-11}	0	0

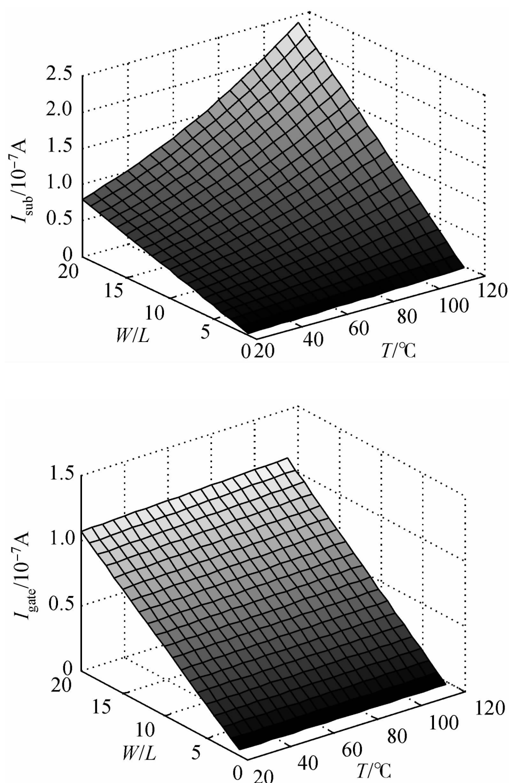


Fig.1 I_{sub} and I_{gate} produced by a 65nm NMOS device with minimum gate length.

Considering the impact of temperatures, in this paper, we examine the leakage current characteristics of dual V_t footed dominos at the upper and lower extremes of a typical temperature spectrum of high performance microprocessor dies: 110℃ which is assumed that the sleep mode is short and the temperature keeps 110℃ during the short sleep period and 25℃ which is assumed that the sleep period is long and the sleep temperature has fallen to the room temperature.

2.2 Leakage current characteristics under process fluctuations

As the CMOS process advances to sub-65nm era, scaling has resulted in significant increase in the variations of the process parameters. The most important of these variations are the variations in the effective channel length (L_{eff}), channel doping concentration (N_{ch}), and t_{ox}.

According to the ITRS[1], the spread in L_{eff} and t_{ox} should taken to be:

$$3\sigma L_{eff} \leqslant 10\% \quad (6)$$

$$3\sigma t_{ox} \leqslant 10\% \quad (7)$$

However, for sub-65nm technologies with L_{eff} much less than 65nm and t_{ox} no more than 1.3nm, the variations in L_{eff} and t_{ox} increase with the increasing difficulty in process controlling, which has significant effect on I_{sub} and I_{gate} due to their strong dependence on the two parameters.

In addition to variations in L_{eff} and t_{ox}, there is a statistical random fluctuation of the number of dopants due to the discreteness of atoms. The statistical variation of the number of dopants N increases as N decreases with technology scaling, and thus translates into I_{sub} fluctuation[21].

It is clear that these different sources of physical variation largely affect leakage mechanism. Accordingly, when we study the leakage current characteristics of dual V_t footed dominos, the effect of process variations is considered.

3 Leakage current analysis in dual V_t footed dominos

In this section, the leakage current conduction is analyzed firstly in the dual V_t footed dominos with different sleep state in detail. And in the second part the I_{sub} and I_{gate} analysis of a single transistor is presented.

3.1 Leakage current conduction in the dual V_t footed dominos

The leakage current conduction paths in the dual V_t footed dominos with different sleep states are identified. To make this discussion more clear, consider a typical 2-input dual V_t footed domino AND gate with the conventional CHIH and CHIL states as shown in Fig. 2. It can be seen that there are multiple sources of I_{gate} in a dual V_t footed domino circuit, but this work aims to reduce I_{gate} through the PDN and the footer (PDNF). One reason for this is that the remaindings of dominos are PMOS and high V_t NMOS transistors, which all produce less I_{gate} than the low V_t NMOS transistors in the PDNF. Second, the remaindings of different logic dual V_t footed dominos have the same structure, and yet the number of the PDNF is increased with the increasing of the fan-in. Thus, I_{gate} through the PDNF plays a crucial role in determining the total I_{gate}, especially in the high fan-in dominos.

As illustrated in Fig. 2, when the footed dominos are in the conventional CHIH and CHIL states, its leakage current characteristics is similar to the footless conditions analyzed in Ref.[17]. The CHIH state turns off all of the high V_t transistors, suppressing I_{sub}. But the PDNF are all turned on and produce the greatest forward I_{gate}. To reduce I_{gate}, the CHIL state cuts off the NMOS transistors in the PDN, which produce reverse and edge reverse I_{gate}. But in this case, significant I_{sub} flows through the PDN. Further, in the CHIL state, the footer exhibits maximum forward I_{gate} due to the high clock signal, which im-

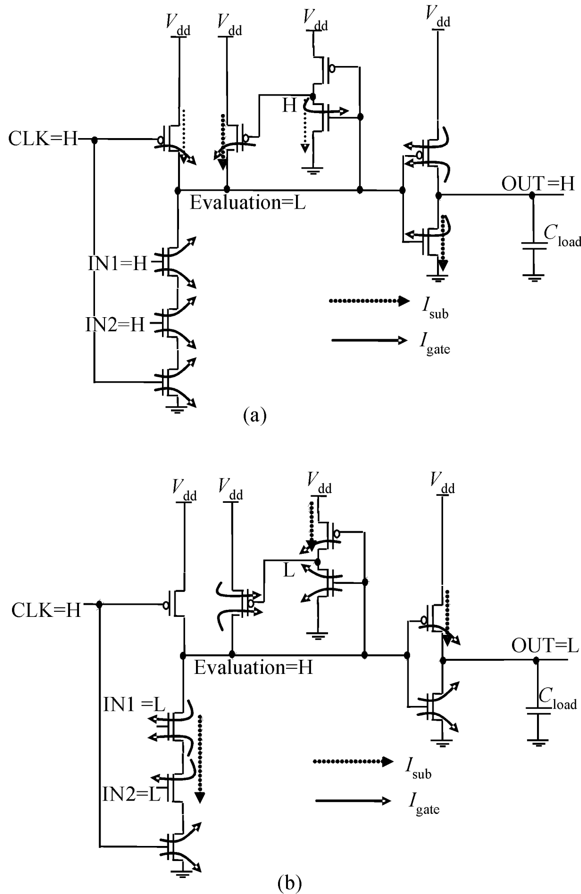


Fig.2　Variation of the I_{sub} and I_{gate} conduction paths with the two conventional sleep states in a 2-input dual V_t footed domino AND gate (The high V_t transistors are symbolically represented by a thick line in the channel region.)　(a) CHIH; (b) CHIL

poses a serious limitation to the leakage current reduction that can be provided by the dual V_t technique.

Therefore, to suppress the leakage current effectively, we propose the sleep state with low clock signal and inputs (CLIL) as shown in Fig. 3. For the CLIL state, since all the transistors in the PDNF are turned off, reverse and edge reverse I_{gate} exist in the PDNF, which is smaller than those in the CHIH and CHIL states. Also, the off PDNF in series prevents I_{sub} from increasing greatly due to the stack effect[10]. Hence, the CLIL state suppresses I_{gate} greatly and produces middling I_{sub}, compared to the CHIH and CHIL states.

Notice that, in general, the CHIH minimizes I_{sub}, the CLIL state leads to minimum I_{gate}, and the CHIL state has little its own predominance compared to the others. And between CHIH and CLIL states, which one is better for the total leakage current minimization is dependent on the relative contribution of I_{sub} and I_{gate} to the total leakage current. If I_{gate} is the highest source, the CLIL states are preferable; otherwise the CHIH state is the best choice.

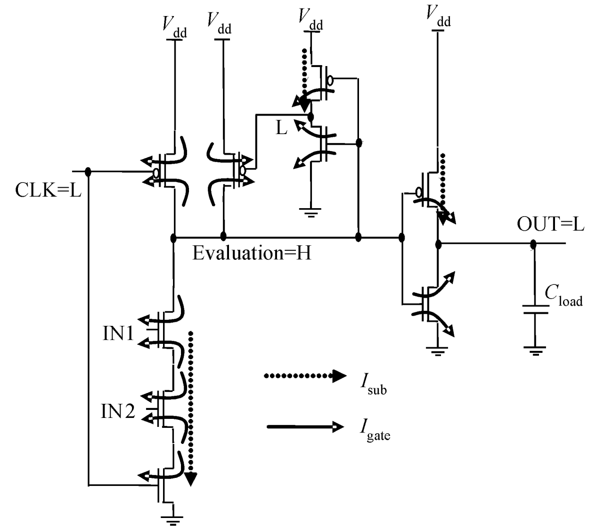


Fig.3　Variation of the I_{sub} and I_{gate} conduction paths with the CLIL state in a 2-input dual V_t footed domino AND gate

3.2　I_{sub} and I_{gate} analysis of a single transistor

In this part, the comparison of I_{sub} and I_{gate} of a single transistor is analyzed and the results are shown in Fig. 4. It is can be seen that I_{sub} produced by the low V_t transistors is the highest source of leakage current in sub-65nm technologies at 110℃. It is important to note that, for the 65nm technology at 110℃, the gap between I_{gate} and I_{sub} of the low V_t transistors is much narrower than that in the 45nm technology.

At 25℃, I_{gate} produced by low V_t NMOS transistors in the PDNF is the dominant source of the leakage current in sub-65nm technologies, as shown in Fig. 4.

The opposite results at two typical sleep temperatures are attributed to the different dependence of I_{sub} and I_{gate} on the temperature, as discussed in Section 2. At low temperature, I_{gate} is the bigger contributor and it has a very weak dependence on temperature. And yet I_{sub} increases exponentially with the temperature increasing, therefore, it dominates the leakage current at high temperature. However, for a domino circuit composed of many transistors, the relative contribution of I_{sub} and I_{gate} also varies with the fan-in, structure of the PDN[17]. It is shown that a quantitative analysis is needed to identify the optimum combination state of the inputs and clock signal with the minimum total leakage current at two typical sleep temperatures in sub-65nm era.

4　Leakage current characteristics of dual V_t footed dominos with different sleep states

In the following experiments, the leakage cur-

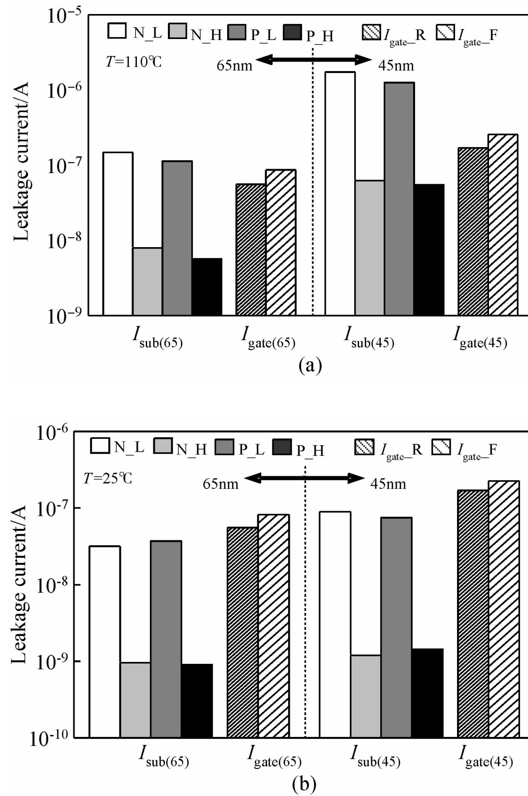


Fig.4 Comparison of I_{sub} and I_{gate} of a single sub-65nm transistor at two typical sleep temperatures (N_L: low V_t NMOS. N_H: high V_t NMOS. P_L: low V_t PMOS. P_H: high V_t PMOS. I_{gate}_R: reverse I_{gate}. I_{gate}_F: forward I_{gate}) (a) 110℃; (b) 25℃

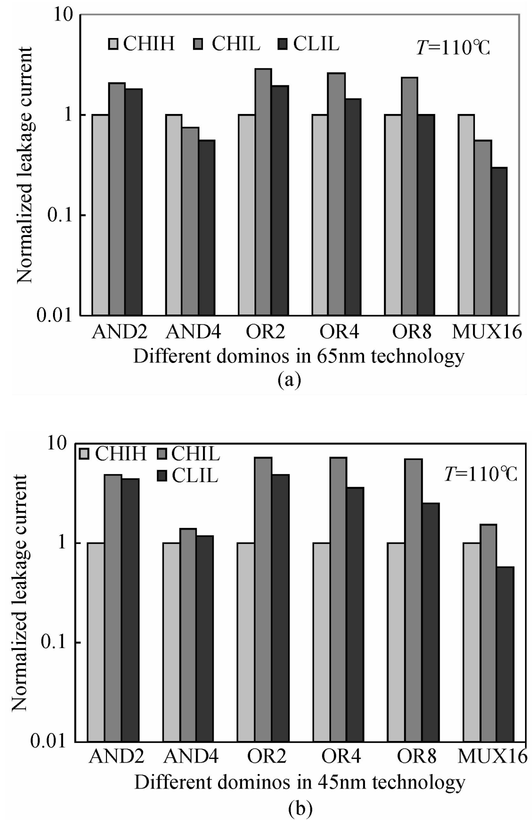


Fig.5 Comparison of the total leakage current of dual V_t footed dominos with three sleep states at 110℃ The leakage currents are all normalized to the total leakage current of corresponding gates with the CHIH state.

rent of sleep dual V_t footed dominos with different fan-in and PDN structure at two typical sleep temperatures is evaluated for CMOS 65nm and 45nm BSIM4 models[22], respectively. All the parameters are listed in Table 2. The benchmark circuits are all sized to operate with a 1GHz clock at a worst case temperature of 110℃. To have a comparison, the transistors in each type dominos have the same physical size, respectively.

4.1 Leakage current at high temperature

The leakage current of dual V_t footed dominos with three states at 110℃ is shown in Fig.5. As discussed above, I_{sub} produced by the low V_t transistors is the highest source of leakage current in sub-65nm technologies at 110℃. The CHIH state is, therefore, preferable to suppressing the total leakage current in

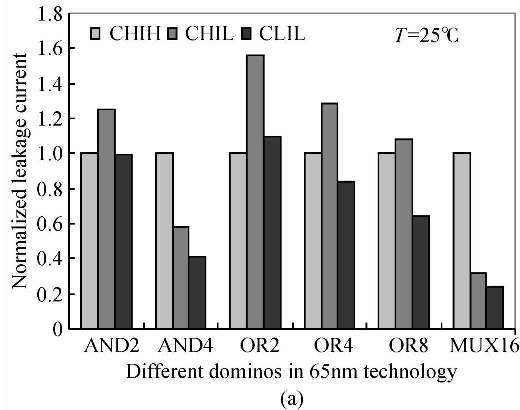
Table 2 Process parameter

Parameter	65nm	45nm
V_{DD}	1V	0.8V
L_{eff}	65nm	45nm
V_t of high V_t devices	0.35V/−0.35V	0.35V/−0.35V
V_t of low V_t devices	0.22V/−0.22V	0.22V/−0.22V
HSPICE LEVEL	54	54

the majority of dual V_t footed dominos as shown in Fig.5. However, as the increasing of parallel PDN paths, I_{gate} rises and catches up with I_{sub} gradually. Thus, I_{gate} becomes the bigger contributor in high fan-in wide dominos. For the MUX16 gate, therefore, the CLIL state minimizes the leakage current. Simulation results show a leakage improvement of upto 72% and 42% (MUX16) as compared to the CHIH state in 65nm and 45nm technology, respectively. Since for the 65nm technology the gap is much less than the 45nm technology, as mentioned before, I_{gate} is able to catch up with I_{sub} faster, therefore, the effectiveness of the CLIL state decreases with the technology scaling, as indicated in Fig.5.

4.2 Leakage current at low temperature

The leakage current of dual V_t sleep footed dominos with three sleep states at 25℃ is shown in Fig.6. At 25℃, I_{gate} produced by the low V_t NMOS transistors in the PDNF is the dominant source of the leakage current in sub-65nm technologies (Fig.4). Thus, unlike the previously published results, the CLIL state is preferable for minimizing the total leakage current in most dual V_t footed dominos except the OR2 gate (Table 3). As an example, a 65nm OR4



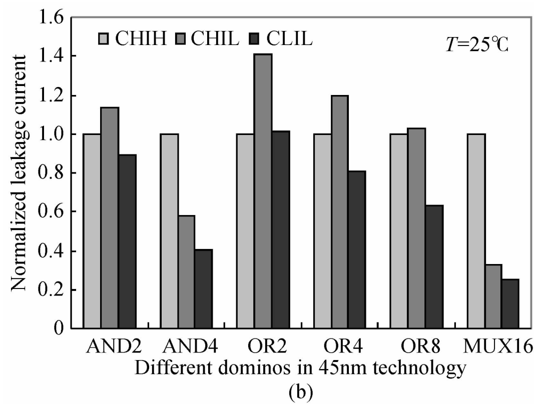


Fig. 6 Comparison of the total leakage current of dual V_t footed dominos with three sleep states at 25℃ The leakage currents are all normalized to the total leakage current of corresponding gates with the CHIH state.

gate would exhibit better leakage characteristics with CLIL state when the temperature is below 53℃ as showed in Fig. 7. In addition, the effectiveness of the CLIL state will become enhancive with the increasing of the fan-in, reducing the total leakage current by up to 76% and 75% (MUX16) in 65nm and 45nm technology, respectively, when compared to the conventional CHIH state.

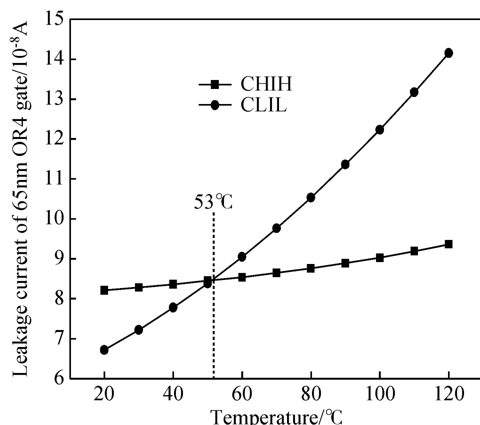


Fig. 7 Leakage current produced by 65nm OR4 domino gate at different temperatures

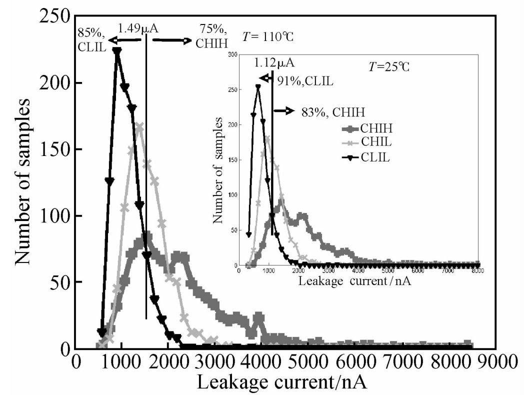


Fig. 8 Distribution of leakage current of MUX16 gate at two typical sleep temperatures

5 Leakage current characteristics of dual V_t footed dominos under process variations

To evaluate the impact of process variations in L_{gate}, N_{ch}, and t_{ox} on the leakage current of the dual V_t footed dominos with different sleep state, 1000 Monte Carlo simulations are done in 65nm CMOS technology. In the simulation, each parameter is assumed to follow Gaussian statistical distribution, with a three sigma (3σ) variation of 10%[17].

Figure 8 shows the leakage current distribution curves of the MUX16 with three different sleep states at two typical sleep temperatures as an example. It can be seen that the distribution curves of the CHIH and CLIL states cross at 1.49μA and 1.12μA at high and low temperatures, respectively. At 110℃, 85% of the samples with the CLIL state produce leakage current lower than 1.49μA and the leakage current of 75% of the samples with the CHIH state is higher than 1.49μA. Alternatively, 91% of the samples with the CLIL state produce leakage current lower than 1.12μA and the leakage current of 83% of the samples with the CHIH state is higher than 1.12μA. These results indicates that the CLIL state are preferable to reducing the total leakage current in majority of the samples under process fluctuations at both high and low temperatures, which is similar to the analysis of the normal one.

To better investigate the impact of the process variation on the leakage current variations of dual V_t footed dominos, we compare the parameter uncertainty (U) of dominos in different sleep states, which is listed in Table 3. Here U is given as the standard deviation (SD) of leakage divided by its average value, which is similar to the definition in Ref. [6].

Table 3 Average and leakage uncertainty of leakage current of dual V_t dominos in 65nm CMOS technology at two typical sleep temperatures

T	state	Average and leakage uncertainty (Average/U) of total leakage current (μA)					
		AND2	AND4	OR2	OR4	OR8	MUX16
110℃	CHIH	0.401/0.389	2.297/0.447	0.069/0.388	0.102/0.428	0.169/0.463	9.854/0.500
	CHIL	0.790/0.156	1.646/0.266	0.187/0.191	0.250/0.205	0.374/0.229	5.248/0.295
	CLIL	0.676/0.201	1.237/0.271	0.127/0.192	0.139/0.192	0.161/0.209	2.826/0.306
25℃	CHIH	0.353/0.421	2.126/0.462	0.061/0.421	0.092/0.453	0.156/0.480	9.351/0.507
	CHIL	0.432/0.256	1.227/0.327	0.092/0.256	0.116/0.274	0.164/0.304	2.934/0.379
	CLIL	0.338/0.265	0.854/0.359	0.065/0.251	0.075/0.252	0.097/0.280	2.195/0.373

As implied by the results from Table 3, the CHIH state is highly susceptible to the manufacturing variations compared to the other two states. And between the CHIL and CLIL states, the former is more robust to process variations in AND type dual V_t footed dominos and the latter improves the robustness of OR type dual V_t footed dominos. This implies that, although the CHIH state and the CLIL state are more effective to reduce the leakage current, the CLIL state can optimize the leakage current under the temperature and process variations.

6 Conclusions

This paper embarks on a comprehensive quantitative approach to leakage current analysis and optimization in sub-65nm dual V_t footed dominos under the effect of the temperature and process variations. It is shown that in the sub-65nm technology domain, with the increasing contribution of gate leakage current towards the total leakage current, the conventional CHIH and CHIL states are not adequate sleep setup for dual V_t footed dominos. Hence the CLIL state is advanced and the inputs and clock signals combination sleep state dependent total leakage current characteristics is examined and optimized.

HSPICE simulations based on 65nm and 45nm BSIM4 models have been performed. It is observed that the conventional CHIL state is ineffective for lowering the leakage current and the CHIH state is only effective to suppress the leakage current at high temperature other than the high fan-in dominos. Another observation is that the CLIL state reduces the leakage current in high fan-in wide dominos and most of dominos at room temperature by up to 76% depending on technology and circuit structure, compared to the CHIH state. Finally, the leakage current characteristics of the dual V_t footed dominos under the influence of process variations is assessed. It shows that the CHIH state is the most sensitive to the process variations and the CLIL state is the optimal low leakage setup considering both temperature and process variation simultaneously.

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温度和工艺参数浮动下双阈值 footed 多米诺电路的漏电流特性*

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摘要： 考虑到温度和工艺参数浮动的影响，对休眠双阈值 footed 多米诺电路的漏电流特性进行了系统的量化研究和比较，得到了不同温度下的最佳休眠状态.基于 65 和 45nm BSIM4 模型的 HSPICE 仿真表明：与业已提出的 CHIL(时钟为高，输入均为低电平)状态和 CHIH(时钟和输入均为高电平)状态相比，本文提出的 CLIL(时钟和输入均为低电平)状态更有利于减小低温下电路的漏电流和高温下的多扇入电路的漏电流.而且，分析了工艺参数的浮动对双阈值 footed 多米诺电路的漏电流特性的影响，并给出了温度和工艺参数浮动下，双阈值 footed 多米诺电路漏电流最小的休眠状态.

关键词： footed 多米诺；双阈值；漏电流；工艺参数浮动

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