# Design of a 16 gray scales 320 × 240 pixels OLED-on-silicon driving circuit*

Huang Ran(黄苒)†, Wang Xiaohui(王晓慧), Wang Wenbo(王文博),
Du Huan(杜寰), and Han Zhengsheng(韩郑生)

*(Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China)*

**Abstract:** A 320×240 pixel organic-light-emitting-diode-on-silicon (OLEDoS) driving circuit is implemented using the standard 0.5 $\mu$m CMOS process of CSMC. It gives 16 gray scales with integrated 4 bit D/A converters. A three-transistor voltage-programmed OLED pixel driver is proposed, which can realize the very small current driving required for the OLEDoS microdisplay. Both the D/A converter and the pixel driver are implemented with pMOS devices. The pass-transistor and capacitance in the OLED pixel driver can be used to sample the output of the D/A converter. An additional pMOS is added to OLED pixel driver, which is used to control the D/A converter operating only when one row is on. This can reduce the circuit's power consumption. This driving circuit can work properly in a frame frequency of 50 Hz, and the final layout of this circuit is given. The pixel area is $28.4 \times 28.4$ $\mu$m$^2$ and the display area is $10.7 \times 8.0$ mm$^2$ (the diagonal is about 13 mm). The measured pixel gray scale voltage shows that the function of the driver circuit is correct, and the power consumption of the chip is about 350 mW.

**Key words:** OLED-on-silicon; microdisplay; driving circuit; 16 gray scales; D/A converter
**DOI:** 10.1088/1674-4926/30/1/015010 **EEACC:** 1280

## 1. Introduction

Microdisplays can be used in projector and "near-eye" applications, such as rear-projection TV, head-mounted displays and camera viewfinders[1]. Organic-light-emitting-diode-on-silicon (OLEDoS) is a new microdisplay technology. OLED has many superior performances over LCD, such as lower power consumption, faster response, and larger view angle[2]. With the silicon chip and standard CMOS technology, cost can be reduced and the reliability and stability of the circuit can also be assured. So OLED-on-silicon will occupy an important position in microdisplay market.

In this paper, a $320 \times 240$ pixel OLED-on-silicon driving circuit is implemented using the standard 0.5 $\mu$m CMOS process of CSMC. The pixel area is $28.4 \times 28.4$ $\mu$m$^2$ and the display diagonal is 13 mm. With so small a pixel area, the OLED pixel current is only tens to hundreds of nanoamperes[3]. Working currents of the traditional MOS devices are always much greater than 1 $\mu$A, and their channel length needs to be increased to tens or even hundreds of micrometersto handle such low currents[4]. The traditional two-transistor voltage-programmed pixel driver[5] (Fig.2(a)) is no longer fit for OLED-on-silicon microdisplay, so a new three-transistor voltage-programmed pixel driver (Fig.2(b)) is proposed. A third pMOS transistor is paralleled with an OLED device to bypass the driving current and to make the OLED current small enough.

To implement 16 gray scales, 4 bit D/A converters using pMOS transistors[6] (Fig.2(c)) are integrated. Obviously, this will increase the circuit's power consumption, so an efficient measure has been proposed. Through reducing the operation time of each row, the working time of D/A converters can also be reduced. The details are as follows.

## 2. Design of the OLED-on-silicon driving circuit

### 2.1. System architecture

The system architecture of the OLED-on-silicon driving circuit is shown in Fig.1. The "digital control" is made with FPGA or other digital chips, which is not integrated with the driving circuit.

4 bit digital video data of one row are shifted and controlled by the signal of the "pixel clock". When video data of this row (320 pixels) are input, the signal "row clock" will store these data in latches. Then the 4 bit digital outputs

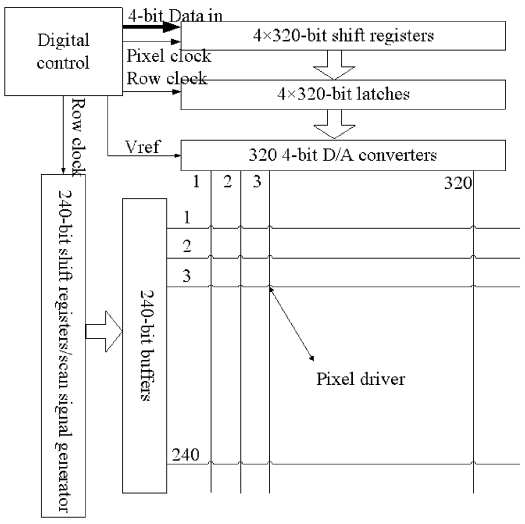


Fig.1. System architecture of the driving circuit.

* Project supported by the State Key Development Program for Basic Research of China (No. 2003CB314705).
† Corresponding author. Email: huangran@ime.ac.cn
Received 13 July 2008, revised manuscript received 14 August 2008

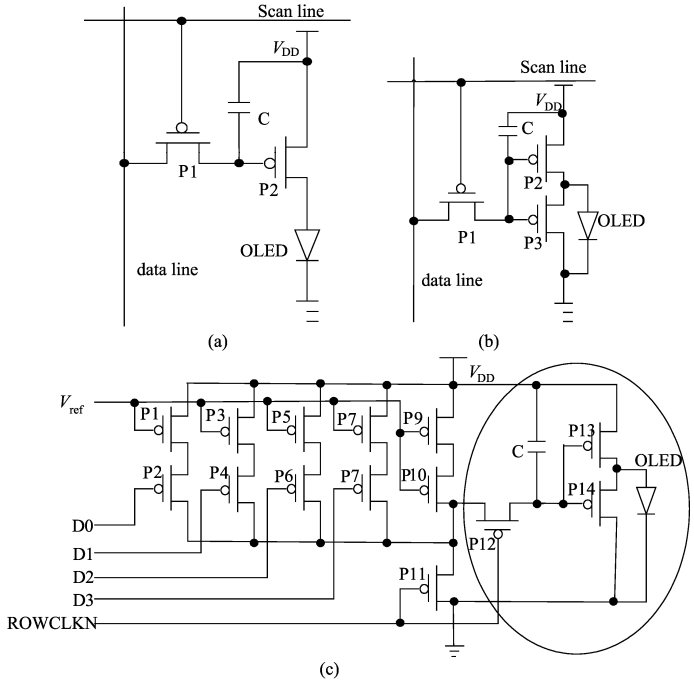


Fig.2. (a) Traditional two-transistor voltage-programmed OLED pixel driver; (b) Three-transistor voltage-programmed OLED pixel driver proposed by the author; (c) D/A converter used in this work with the pixel driver of (b).

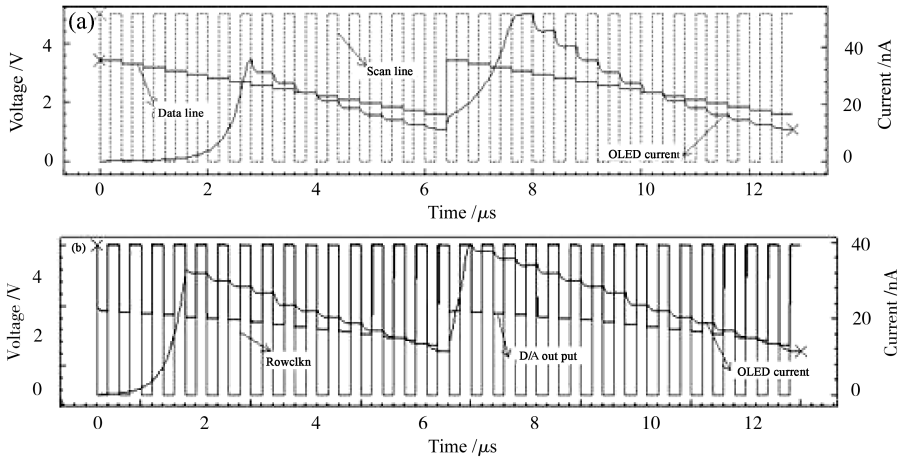


Fig.3. (a) Simulation result of the circuit in Fig.2 (b); (b) Simulation result of the circuit in Fig.2 (c).

of these latches will be transformed into analog signals. At the same time, these analog signals will be sent to the row that is on to drive the pixels of this row.

All the shifter registers, latches and buffers are implemented in 0.5 $\mu$m standard CMOS devices from CSMC. These are easy to realize, and will not be focused on. The integrated D/A converter and the measure taken to reduce the circuit's power consumption will be discussed in detail.

### 2.2. Pixel circuits and integrated D/A converters

The pixel area is 28.4 × 28.4 $\mu$m$^2$ and the OLED pixel current is only tens to hundreds nanoamperes. The traditional two-transistor voltage-programmed pixel driver (Fig.2(a)) cannot realize such a small current even $(W/L)_{P2}$ is 1.6/200 that occupy more than 30 × 30 $\mu$m$^2$ area with the 0.5 $\mu$m process. A new three-transistor voltage-programmed pixel driver (Fig.2(b)) is proposed. A third pMOS transistor is placed parallel to the OLED device to bypass the driving current and to make the OLED current small enough. Reducing $(W/L)_{P2}$ can decrease power consumption of the pixel circuits and increasing $(W/L)_{P3}$ can enlarge the range of output voltage. To satisfy the requirement of power consumption and output voltage range, the final size of the pixel circuit is $(W/L)_{P1}$= $(W/L)_{P3}$= 1.1/0.55, and $(W/L)_{P2}$ = 1.1/26.1. The simulated voltage range is 3.0911–4.4135 V.

D/A converters are analog circuits and always have high power consumption. To integrate D/A converters to digital circuits means increasing the circuits' power consumption greatly, especially for display driving circuits which always need one D/A converter for every column, so the D/A converter is not always chosen by designers. Here, because of the nonlinear characteristics of the driving current of the voltage-programmed OLED pixel circuit, nonlinear D/A converters (Fig.2 (c)) are used to improve the nonlinear characteristics. The comparison is shown in Fig.3. Here, the simplest OLED H-spice model[7] is used, which consists of a diode parallel

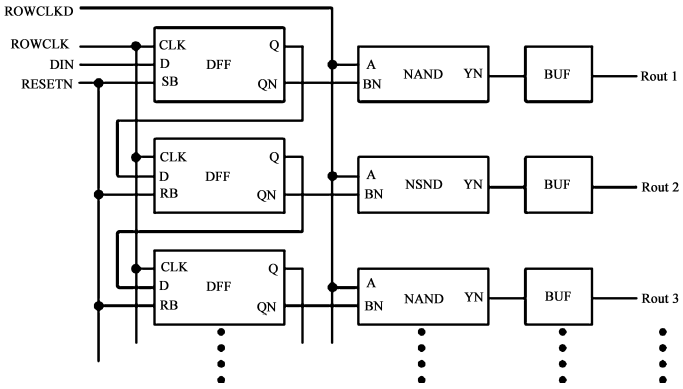


Fig.4. Row scan generator.

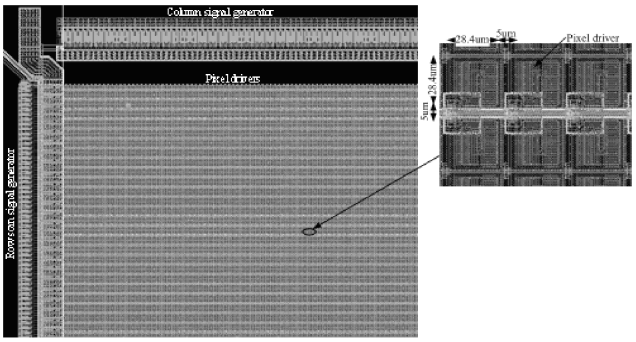


Fig.5. Part of the final layout.

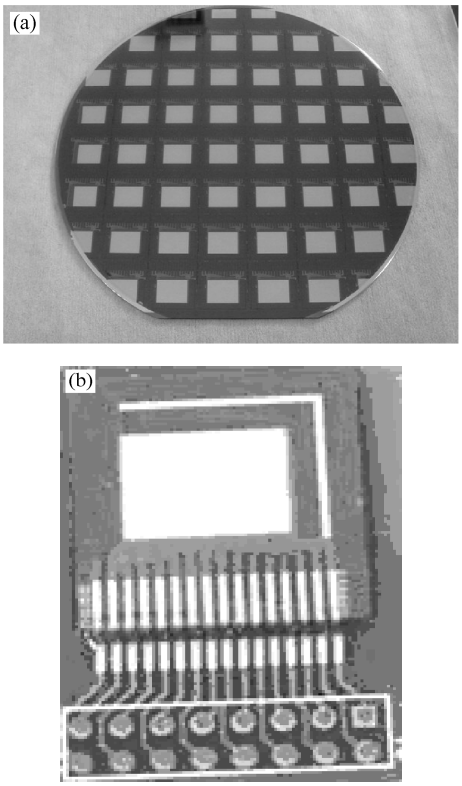


Fig.6. (a) Wafer of the OLEDoS driving circuit; (b) PCB package of the OLEDos driving circuit.

connected to a capacitor. The main H-spice model parameters of the diode are: reverse saturation current $I_s = 1.78 \times 10^{-5}$ mA/cm$^2$, emission coefficient $n = 28$, series resistance $r_s = 0$, area $= 9 \times 10^{-6}$ m$^2$, and level = 1. The paralleled capacitor $C_{OLED} = 30 \times 30\ \mu m^2 \times 25$ nF/cm$^{2[7]} = 0.225$ pF.

Figure 3 (a) shows that with the linear input (on the data line) the voltage-programmed pixel driver only has the nonlinear OLED current. While in Fig.3 (b), the nonlinear output of D/A converter rectifies the nonlinear OLED current a little.

In Fig.2 (c), the gate of transistor P11 is connected to the signal "ROWCLKN" which can control the on-off of P11 and then the on-off of the D/A converter. So through the signal "ROWCLKN" the operation time of the D/A converter can be adjusted and the circuit power consumption can be properly reduced. The on-time of the circuit should be long enough to make sure that the capacitor $C$ is charged or discharged completely.

With the frame frequency 50 Hz, the capacitor $C$ should keep the voltage level for 20 ms. So, from the formula $t = RC = VC/I$, we get $C = tI/V$. The p-type pass-transistor (Fig.2(a), (b) P1, (c) P12) always has an off-state current of hundreds of picoamperes, and the voltage level is 5 V, so the capacitor $C \approx 0.02\text{s} \times 2.5 \times 10^{-10}$ A/5 V = 1 pF. At the same time, the p-type pass-transistor has an on-state current of several milliamperes, so the capacitor $C$ can be charged from 0 to 5 V in about several nanoseconds. For the 320 × 240 pixel driver, the pixel clock is 3.84 MHz and the row clock is 12 kHz. So the routine time of one row to be chosen is about 80 μs, which is long enough for capacitor $C$ to be charged or discharged. That is why the on-time of one row can be decreased.

### 2.3. Design of the row scan signal generator

In order to reduce the on-time of one row, the row scan signals need to be a little special. The conventional scan signals generated by serials of DFFs are sent to NANDs (Fig.4), and operated by the row clock. So, the pulse width of row clock decides the on-time of one row.

In Fig.4, the signal ROWCLKD is a several nanoseconds delay signal of ROWCLK. Here the purpose is to avoid the burr problem. Though adjusting the pulse width of ROWCLK, the on-time of one row can also be adjusted. According to the maximal time of capacitor $C$ being charged or discharged, the minimal pulse width can be decided. At the same time, the operating time of the D/A converters is reduced from 80 $\mu$s to hundreds of nanoseconds, so the power consumption can be lowered considerably.

### 2.4. Final layout

Based on the design discussed above, the circuit will be fabricated using the standard 0.5 $\mu$m CMOS process of CSMC, and part of the final layout is shown in Fig.5. In this layout, the pixel area is $28.4 \times 28.4\ \mu m^2$, and the distance of the adjacent pixels is 5 $\mu$m.

Here, the gate capacitor is used as the storage capacitor $C$. With a gate oxide thickness of 125, the gate capacitance per area $C'_{ox} = \varepsilon_r \varepsilon_0 / t_{ox}^{[8]} = 3.9 \times 8.85418 \times 10^{-12}$ F/m/($125 \times 10^{-10}$m) = 2.7 fF/$\mu$m$^2$. So the capacitor in pixel driver $C \approx C'_{ox}\ WL = 2.7$ fF/$\mu$m$^2 \times 427.8\ \mu$m$^2 = 1.155$ pF, fitting to the designed value.

Because of the special requirement of display panel, the

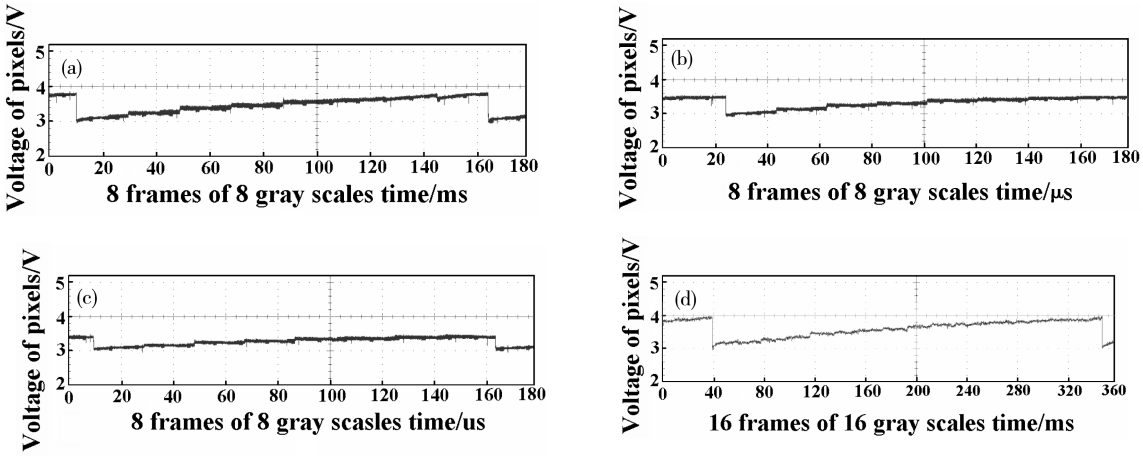


Fig.7. Test waveforms of the driving circuit pixels. (a) 8 frames of 8 scale pixel voltage with 2.0 V $V_{\rm ref}$; (b) 8 frames of 8 scale pixel voltage with 2.5 V $V_{\rm ref}$; (c) 8 frames of 8 scales pixel voltage with 3.0 V $V_{\rm ref}$; (d) 16 frames of 16 scale pixel voltage with 2.0 V $V_{\rm ref}$.

flatness of the driving IC surface is very important. The planarization process is the difficulty and will affect the results. We will focus on this in future work.

## 3. Results and discussion

The driving circuit is implemented using the standard 0.5 $\mu$m CMOS mixed signal process of CSMC. Figure 6 (a) shows the wafer of the OLEDoS driving circuit and Fig.6 (b) shows a chip with PCB package.

Inputing an eight-frames sequence with an eight gray scale signal (0000, 0010, 0100...1110) into the driving circuit with different $V_{\rm ref}$ voltages of the D/A convertor and measuring the voltage of pixels, the results in Fig.7 show that with different $V_{\rm ref}$ voltages 2.0 V (Fig.7(a)), 2.5 V (Fig.7(b)) and 3.0 V (Fig.7(c)), the voltage range is 0.83, 0.57 and 0.51 V, and the increment of the voltage decreases with the rising voltage. The measured result agrees with the simulation result. Inputting a 16 frame sequence with a 16 gray scale signal (0000, 0001,0010...1111) to the driving circuit with 2.0V $V_{\rm ref}$ voltage of D/A convertor, the pixel voltage is shown in Fig.7 (d). The waveform shows that the voltage range is from 3.08 to 3.98 V, and the gray scale response is correct. The measured power consumption of the dirving circuit is about 350 mW.

## 4. Conclusion

In this paper, a 320 × 240 pixels OLED-on-silicon driving circuit was implemented using the standard 0.5 $\mu$m CMOS process of the CSMC. 4 bit D/A converters and a three-transistor voltage-control pixel driver proposed by the author were used to realize 16 gray scales. Measures were taken to decrease the power consumption of the D/A converters. The pixel area is $28.4 \times 28.4$ $\mu$m$^2$ and the display area is $10.7 \times 8.0$ mm$^2$ (the diagonal is about 13 mm). The measured results show that this driving circuit can work properly, and the power consumption of the chip is about 350 mW.

## References

[1] Armitage D, Underwood I, Wu S T. Introduction to microdisplays. Chichester: John Wiley & Sons Ltd, 2006: 1

[2] Bardsley J N. International OLED technology roadmap. IEEE J Sel Topics Quantum Electron, 2004, 10 (1): 3

[3] Levy G B, Evans W, Ebner J, et al. An 852×600 pixel OLED-on-silicon color microdisplay using CMOS subthreshold-voltage-scaling current drivers. IEEE J Solid-State Circuits, 2002, 37 (12): 1879

[4] Ng R. Design and application of OLED drivers. Available: http://www.solomon-systech.com/pdf/IIC-China%202004_040114.pdf

[5] Aerts W F, Verlaak S, Heremans P. Design of an organic pixel addressing circuit for an active-matrix OLED display. IEEE Trans Electron Devices, 2002, 49: 2124

[6] Lee C A, Lee J D, Park B G. Design of a CMOS on-chip driver circuit for active matrix polymer electroluminescent displays. SID'03 Digest, Daegu, Korea, 2001: 330

[7] Dawson R, Shen Z, Furst D A, et al. The impact of the transient response of organic light emitting diodes on the design of active matrix OLED displays. International Electron Devices Meeting, Princeton, NJ, USA: Sarnoff Corp, 1998: 875

[8] Baker R J, Li H W, Boyce D E. CMOS circuit design, layout and simulation. New York: IEEE Press, 1997: 83