Design procedure for optimizing CMOS low noise operational amplifiers

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Abstract: This paper presents and experimentally verifies an optimized design procedure for a CMOS low noise operational amplifier. The design procedure focuses on the noise performance, which is the key requirement for low noise operational amplifiers. Based on the noise level and other specifications such as bandwidth, signal swing, slew rate, and power consumption, the device sizes and the biasing conditions are derived. In order to verify the proposed design procedure, a three-stage operational amplifier has been designed. The device parameters obtained from the proposed design procedure closely agree with the simulated results obtained by using HSPICE.

Key words: design procedure; noise; operational amplifier; optimize
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1. Introduction

CMOS operational amplifiers (opamps) are important parts in analog ICs[1]. The noise performance of opamps is one of the key requirements because it deteriorates the signal-to-noise-ratio (SNR) of circuits[2]. For applications that require high quality signals, such as professional audio equipment and precise instruments, it is necessary to minimize any kind of noise. However, a low noise performance usually comes at the price of lower speed and higher power consumption. From an application perspective, low noise opamps should have an overall optimized performance with the noise level being the most important parameter. Thus, a good design procedure is important for optimizing opamps. Analytical methods can give an insight into the design.

Several design procedures dealing with the noise performance of opamps have been presented in the literature[1, 3, 4]. These design procedures mainly aim at two-stage opamps assuming that long-channel devices are used in the circuits. Moreover, these procedures often do not start with the key specification in mind or emphasize only the relationship between a certain specification and the circuit or devices parameters. However, several new problems have to be considered when using CMOS technology with deep-submicron feature size with the goal of increasing the speed and reducing the chip size. First, often short-channel devices are used in analog circuits. However, typical long-channel noise models cannot predict the noise behavior of short-channel MOSFETs[5] very well. Using such a model has a negative impact on the accuracy of the design. Second, finding a compromise between contradicting specifications becomes more difficult as the power supply voltage decreases[6], which means we must consider how to manually calculate a design before starting a simulation in order to allow for a conclusive and timely circuit design. Hence, an effective design procedure for optimizing CMOS low noise opamps is needed.

In this work, a noise-based optimized design of a three-stage operational amplifier is discussed as a concrete example, in order to illustrate the proposed optimized design procedure starting from a key specification.

2. Topology of the circuit

For an application which requires low noise opamps with high gain, good stability, low voltage, and low power consumption, the noise performance is the key specification. To meet these design objectives while keeping a focus on the noise performance, a three-stage opamp topology was chosen. This topology uses a transconductance with capacitive feedback as a compensation technique (TCFC)[7], as shown in Fig. 1. The opamp includes three transconductance stages. The input stage is a classical folded cascade operational transconductance amplifier (OTA). The differential pair (M1 and M2) has an input transconductance g_{m1}. The second stage is a gain boosting stage. The transistor M9 provides the second-stage transconductance g_{m9}, and the transistor M12 acts as the feedback transconductance g_{m12}. The output stage is a push-pull stage. The transistor M15 acts as the output stage transconductance g_{m15}, while the transistor M14 acts as the feed-forward transconductance stage g_{m14}. C_{m1} is the Miller capacitor establishing the outer feedback loop. C_{m2} is the other feedback capacitor, which forms the internal feedback loop together with the feedback g_{m12}.

3. Circuit design and analysis

The input stage determines the noise performance of the

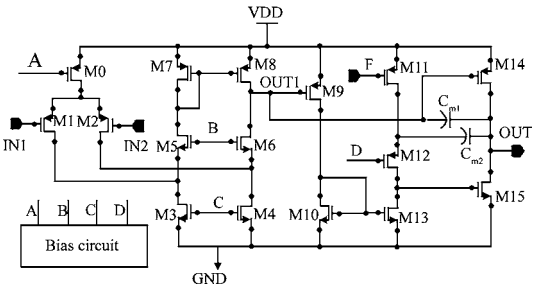

Fig. 1. Schematic of a three-stage opamp.

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overall circuit. For convenience, we assume that the noise from the second and the output stage is negligible. If the noise in each MOSFET is represented by its equivalent input voltage noise, the equivalent input-referred voltage noise for the input stage can be calculated by

$$\overline{v_{\text{in,total}}^2}(\text{V}^2/\text{Hz}) = 2\left[\overline{v_{\text{in,M1}}^2} + \alpha^2\overline{v_{\text{in,M3}}^2} + \beta^2\overline{v_{\text{in,M7}}^2}\right], \quad (1)$$

in which $\alpha = g_{\text{m3}}/g_{\text{m1}} < 1, \beta = g_{\text{m7}}/g_{\text{m1}} < 1$.

From Eq. (1), α and β should be as small as possible, and g_{m1} should be as large as possible in order to reduce the noise contribution from transistors acting as loads or current sources. This basic theory provides the theoretical foundation for optimizing low noise opamps.

3.1. Derivation of the specifications

In this paper, the proposed design procedure for the low noise opamps assumes that the following specifications are required: equivalent input-referred noise voltage ($\overline{v_{\text{in,total}}^2}$), gain-bandwidth (GBW), power consumption (P), slew rate (SR), input common-mode range (ICMR), and output swing (OS).

Since the noise performance is an important specification for low noise opamps, we first begin with noise models. The channel thermal noise and the flicker noise of MOSFETs dominate the noise performance of opamps. For design simplicity, we only consider the thermal noise in the design procedure. The flicker noise can be improved by increasing the device area.

For the design procedure, an analytical channel thermal noise model valid for both short-channel and long-channel MOSFETs will be used here. The measurement results can be fitted by a noise model given as[8]

$$\begin{aligned}
&S_{\text{id}}(\text{A}^2/\text{Hz}) = (4k_{\text{B}}T/I_{\text{DS}})\,G_{\text{d}}^2 V_{\text{deff}}\,m,\\
&m = (1 - u + \frac{u^2}{3}) + b(b - \frac{u}{2} + 1) + \frac{b^3}{u}\ln\frac{1-b}{1-u-b},\\
&G_{\text{d}} = \mu_{\text{eff}} W C_{\text{ox}} V_{\text{gseff}}/(L_{\text{elec}} + V_{\text{deff}}/E_{\text{crit}}),\\
&u = A_{\text{bulk}} V_{\text{deff}}\Big/(V_{\text{gseff}} + 2\phi_{\text{t}}),\\
&b = I_{\text{DS}}\Big/W\mu_{\text{eff}} C_{\text{ox}} V_{\text{gseff}} E_{\text{crit}},
\end{aligned} \quad (2)$$

where k_{B} is the Boltzmann constant, T is the absolute temperature, I_{DS} is the drain current, A_{bulk} is the bulk effect parameter, ϕ_{t} is the thermal voltage, L_{elec} is the electrical channel length, E_{crit} is the critical electrical field, V_{gseff} is the effective overdrive voltage[9], and V_{deff} is the effective drain voltage[9]. V_{deff} approaches V_{DS} when $V_{\text{DS}} < V_{\text{DSAT}}$, and it approaches V_{DSAT} when $V_{\text{DS}} > V_{\text{DSAT}}$[9].

The voltage noise spectrum density and the current noise spectrum density can be converted by $S_{\text{id}}(\text{A}^2/\text{Hz}) = \overline{v_{\text{in}}^2}(\text{V}^2/\text{Hz}) \cdot g_{\text{m}}^2$. Substituting Eq. (2) into Eq. (1), yields

$$\overline{v}_{\text{in,total}}^2(\text{V}^2/\text{Hz}) = 2[S_{\text{id,M1}} + S_{\text{id,M3}} + S_{\text{id,M7}}]/g_{\text{m1}}^2. \quad (3)$$

The transistors in analog ICs mostly operate under strong inversion, and the transconductance can be obtained as

$$g_{\text{m}} = \sqrt{2\mu_{\text{eff}} C_{\text{ox}}(W/L_{\text{elec}}) I_{\text{DS}}} = 2I_{\text{DS}}/V_{\text{gseff}} = G_{\text{d}}. \quad (4)$$

Using Eqs. (2) and (4), while assuming $E = V_{\text{deff}}/L_{\text{elec}}$ for saturated transistors, Equation (3) can be rewritten as

$$\overline{v}_{\text{in,total}}^2(\text{V}^2/\text{Hz}) = \frac{16k_{\text{B}}T}{g_{\text{m1}}}[m_{\text{M1}} + \alpha m_{\text{M3}} + \beta m_{\text{M7}}], \quad (5)$$

in which m_{M1}, m_{M3}, and m_{M7} correspond to the m in Eq. (2) for the transistors M1, M3, and M7, respectively. For a saturated transistor under strong inversion, b in Eq. (2) can be simplified as $b = V_{\text{gseff}}/(2L_{\text{elec}}E_{\text{crit}})$.

From Eq. (5), the noise performance of the operational amplifier is inversely proportional to g_{m1}. Hence, special care has to be taken when designing the input stage and thus g_{m1}. Furthermore, the noise spectrum density also depends on the effective overdrive voltages of M1, M3, and M7. Thus, we will relate these device parameters to the required specifications in the following derivation. For convenience, we will denote the effective overdrive voltage and the drain current for Mi as $V_{\text{gseff}i}$ and I_i, respectively. "Mi" stands for the transistors (M0–M15) in Fig. 1.

From Ref. [7], the performance parameters ω_0 and SR can be given by

$$\omega_0 = 2\pi \times \text{GBW} = A_{\text{dc}}\,|p_{\text{-3dB}}| = g_{\text{m1}}/C_{\text{m1}}, \quad (6)$$

$$\text{SR} = \min(2I_1/C_{\text{m1}}, I_{14}/C_{\text{L}}), \quad (7)$$

where ω_0 is the unity gain bandwidth, A_{dc} is the DC gain, $p_{\text{-3dB}}$ is the dominant pole, and C_{L} is load capacitance.

The opamp in Fig. 1 has a feed-forward stage g_{m14}, which forms a push-pull output stage that slews fast in both directions. Therefore, the input stage driving the Miller capacitance becomes the dominant limitation of the overall SR. The SR can be written as

$$\text{SR} = I_0/C_{\text{m1}} = 2I_1/C_{\text{m1}} = g_{\text{m1}}V_{\text{gseff1}}/C_{\text{m1}}. \quad (8)$$

From Eqs. (4) and (6),

$$V_{\text{gseff1}} = \text{SR}/\omega_0. \quad (9)$$

If we define $V_{\text{HR}}^{\text{CM}}$ as the opamp head room voltage of the input common-mode range, i.e., $V_{\text{HR}}^{\text{CM+}} = V_{\text{DD}} - V_{\text{in,CM}}^{\text{max}}$ and $V_{\text{HR}}^{\text{CM–}} = V_{\text{in,CM}}^{\text{min}} - \text{GND}$, it can be shown that

$$\begin{aligned}
V_{\text{HR}}^{\text{CM+}} &= V_{\text{gseff0}} + V_{\text{gseff1}} + \left|V_{\text{TH,P}}\right|,\\
V_{\text{HR}}^{\text{CM–}} &= V_{\text{gseff3}} - \left|V_{\text{TH,P}}\right| + V_{\text{TH,N}},
\end{aligned} \quad (10)$$

in which $V_{\text{TH,P}}$ and $V_{\text{TH,N}}$ represent the threshold voltages of the PMOS and NMOS, respectively. In the same way, we define $V_{\text{HR}}^{\text{out}}$ as the head room voltage of the output voltage swing, i.e.,

$$V_{\text{HR}}^{\text{out+}} = V_{\text{DD}} - V_{\text{out}}^{\text{Max}},\ V_{\text{HR}}^{\text{out-}} = V_{\text{out}}^{\text{Min}} - \text{GND}.$$

The following relations can be obtained:

$$\begin{aligned}
V_{\text{HR}}^{\text{out+}} &= V_{\text{gseff14}},\\
V_{\text{HR}}^{\text{out–}} &= V_{\text{gseff15}}.
\end{aligned} \quad (11)$$

For minimizing the offset, accurate matching must be guaranteed. Thus we set

$$\begin{aligned} V_{\text{gseff7}} &= V_{\text{gseff9}} = V_{\text{gseff14}} = V_{\text{HR}}^{\text{out+}}, \\ V_{\text{gseff10}} &= V_{\text{gseff13}} = V_{\text{gseff15}} = V_{\text{HR}}^{\text{out–}}. \end{aligned} \tag{12}$$

To avoid the slewing effect in high-speed circuits with large signal levels, the drain current I_3 of M3 should be larger than I_0. If we assume that $I_3 = I_0 = 2I_1$, then $I_7 = I_3 - I_1 = I_1$. Thus, using Eqs. (2), (7), (8) and (10), α and β can be expressed by the required specifications as

$$\begin{aligned} \alpha &= \frac{2 \cdot \text{SR}}{\omega_0(V_{\text{HR}}^{\text{CM–}} + \left|V_{\text{TH,P}}\right| - V_{\text{TH,N}})}, \\ \beta &= \text{SR}/(\omega_0 V_{\text{HR}}^{\text{out+}}). \end{aligned} \tag{13}$$

This is different from the presumed values for α and β in Ref. [3].

Up to now, the effective overdrive voltages for all transistors have been related to the required specifications. The drain currents I_3 and I_7 depend on $I_1 = (g_{\text{m1}} V_{\text{gseff1}})/2$. Thus, g_{m1} should firstly be calculated according to the required specifications. Therefore, we will first determine the device sizes and biasing conditions starting from g_{m1} in section 3.2.

3.2. Design procedure

Based on the aforementioned analysis, we will design the device sizes and biasing conditions by the following steps:

Step 1: Calculate the key variable g_{m1} based on the required noise performance. From Eq. (3),

$$g_{\text{m1}} = \frac{16 k_{\text{B}} T}{\overline{v_{\text{in,thermal}}^2}}(m_{\text{M1}} + \alpha m_{\text{M3}} + \beta m_{\text{M7}}). \tag{14}$$

The obtained g_{m1} from Eq. (12) should be the minimum value for ensuring the noise performance. Relaxing the noise requirement allows for more margins in the design.

Step 2: Calculate C_{m1}.

From Eq. (6),

$$C_{\text{m1}} = g_{\text{m1}}/\omega_0. \tag{15}$$

Step 3: Calculate the drain currents I_1, I_3, I_7 and I_0.

$$\begin{aligned} I_1 &= \frac{g_{\text{m1}} V_{\text{gseff1}}}{2} = \frac{g_{\text{m1}}}{2}\frac{\text{SR}}{\omega_0}, \\ I_3 &= \frac{\alpha g_{\text{m1}} V_{\text{gseff3}}}{2} = \frac{\alpha g_{\text{m1}}}{2}(V_{\text{HR}}^{\text{CM–}} + \left|V_{\text{TH,P}}\right| - V_{\text{TH,N}}), \\ I_7 &= \frac{\beta g_{\text{m1}} V_{\text{gseff7}}}{2} = \frac{\beta g_{\text{m1}}}{2} V_{\text{HR}}^{\text{out+}}, \\ I_0 &= 2I_1. \end{aligned} \tag{16}$$

As a result, $(W/L)_1$, $(W/L)_3$, $(W/L)_7$ and $(W/L)_0$ can be calculated using the square law of drain currents, in which we express the effective mobilities as $\mu_{\text{eff,P}}$ and $\mu_{\text{eff,N}}$ for the PMOS and the NMOS, respectively.

$$\begin{aligned} (W/L)_1 &= \frac{g_{\text{m1}}}{\mu_{\text{eff,P}} C_{\text{ox}}(\text{SR}/\omega_0)}, \\ (W/L)_3 &= \frac{\alpha g_{\text{m1}}}{\mu_{\text{eff,N}} C_{\text{ox}}(V_{\text{HR}}^{\text{CM–}} + \left|V_{\text{TH,P}}\right| - V_{\text{TH,N}})}, \\ (W/L)_7 &= \frac{\beta g_{\text{m1}}}{\mu_{\text{eff,P}} C_{\text{ox}} V_{\text{HR}}^{\text{out+}}}, \\ (W/L)_0 &= \frac{2 g_{\text{m1}} \text{SR}/\omega_0}{\mu_{\text{eff,P}} C_{\text{ox}}(V_{\text{HR}}^{\text{CM+}} - \text{SR}/\omega_0 - \left|V_{\text{TH,P}}\right|)^2}. \end{aligned} \tag{17}$$

Step 4: Calculate $(W/L)_{14}$ and $(W/L)_{15}$.

From Eqs. (7) and (11), we assume $I_{14} = 4.5\text{SR}C_{\text{L}}$, then

$$\begin{aligned} (W/L)_{14} &= \frac{4.5\text{SR}C_{\text{L}}}{\mu_{\text{eff,P}} C_{\text{ox}}(V_{\text{HR}}^{\text{out+}})^2/2}, \\ (W/L)_{15} &= \frac{4.5\text{SR}C_{\text{L}}}{\mu_{\text{eff,N}} C_{\text{ox}}(V_{\text{HR}}^{\text{out–}})^2/2}. \end{aligned} \tag{18}$$

Step 5: Calculate $(W/L)_9$, $(W/L)_{10}$ and $(W/L)_{13}$.

The quiescent power consumption of the opamp shown in Fig. 1 can be expressed as

$$P = (I_0 + 2I_7 + I_9 + I_{13} + I_{14})V_{\text{DD}}. \tag{19}$$

If we assume that $I_9 = 2I_{13}$, the width-to-length ratios of M9, M10 and M13 can be written as

$$\begin{aligned} (W/L)_9 &= \frac{(2/3)(P/V_{\text{DD}} - I_0 - 2I_7 - I_{14})}{\mu_{\text{eff,P}} C_{\text{ox}}(V_{\text{HR}}^{\text{out+}})^2/2} \\ (W/L)_{10} &= \frac{(2/3)(P/V_{\text{DD}} - I_0 - 2I_7 - I_{14})}{\mu_{\text{eff,N}} C_{\text{ox}}(V_{\text{HR}}^{\text{out–}})^2/2} \\ (W/L)_{13} &= (W/L)_{10}/2. \end{aligned} \tag{20}$$

Step 6: Decide on $(W/L)_5$, $(W/L)_{11}$, $(W/L)_{12}$ and C_{m2}.

The drain current of M11 or M12 is equivalent to that of M13, and the drain current of M5 is equivalent to that of M7. The bias voltages F, D, and B for M11, M12, and M5 can be adjusted by the bias circuit. Thus $(W/L)_{11}$, $(W/L)_{12}$, and $(W/L)_5$ can be chosen freely. For the stability of the opamp, it is necessary that $C_{\text{m2}} \gg C_2$, $g_{\text{m9}}/C_2 \gg 2\pi\text{GBW}$, and $C_L \gg C_{\text{m1}}$, where C_2 is a lumped parasitic capacitance.

3.3. Extension of the design procedure

The design procedure described in section 3.2 aims at low noise opamps, e.g., opamps for which the noise performance is considered to be the key specification. In fact, the design procedure can be extended to designs using the other specification, such as bandwidth or slew rate, as the key parameter depending on the requirements of the application. For example, for an opamp which needs to drive a large load capacitance C_{L}, I_{14}/C_{L} in Eq. (9) might become the dominant limitation of the SR. As a result, I_{14} becomes the key design variable, and thus should be calculated first. Moreover, the design procedure can also be extended to other opamp structures. However, this might require modifying the given equations based on small-signal frequency response analysis. For example, for a basic

Table 1. Expected specifications and constraints for our opamp.

Electrical parameters	Expected
Supply voltage (V)	1.8
Load capacitance C_L(pF)	5
GBW (MHz)	80
Power consumption (mW)	< 1.2
Slew rate (V/μs)	> 12
Input noise (nV/$\sqrt{\text{Hz}}$) @ 10 MHz	35
DC gain: A_{dc}(dB)	> 100
Phase margin ($^\circ$)	> 45
Input common range (V)	0–1.265
Outout voltage swing (V)	0.3–1.6

Table 2. Simulated design parameters of the opamp in Fig. 1.

Device parameter	From Eq. (21)	From Eq. (14)	Simulated by HSPICE
g_{m1}	1.396×10^{-5}	1.9×10^{-3}	1.489×10^{-3}
g_{m3}	6.759×10^{-6}	9.352×10^{-4}	1.063×10^{-3}
g_{m7}	1.667×10^{-6}	2.307×10^{-4}	2.219×10^{-4}
g_{m9}	1.8×10^{-3}	1.3×10^{-3}	9.876×10^{-4}
g_{m14}	1.8×10^{-3}	1.8×10^{-3}	1.841×10^{-3}
g_{m15}	2.7×10^{-3}	2.7×10^{-3}	2.564×10^{-3}
C_{m1}(pF)	0.02161	3.8449	3

two-stage CMOS opamp composed of seven transistors, Equation (14) becomes simpler because the third term can be removed. In theory, the design procedure can be adapted for other design objectives or other opamp topologies.

In addition, the design procedure is not only valid for deep-submicron CMOS technologies, but also can be applied to long-channel CMOS technologies. This is due to the fact that the noise model (2) can predict the noise behaviors of both short and long-channel devices[8]. Thus, our work makes it possible to use both short and long-channel transistors in analog circuits, which will improve the flexibility of choosing the CMOS technology for an opamp design.

The validity of the design procedure is proved by comparing the design objectives and measured results in section 4.

4. Experimental results

4.1. Simulated results

The chosen specifications for our opamp are shown in Table 1. From the aforementioned analysis, the transconductances of the devices are directly related to the required specifications of the opamp. The transconductances of the devices calculated from Eq. (3) are given in Table 2. For comparison, the transconductances were also calculated using the long-channel noise model, given by

$$g_{m1} = \frac{8k_B T\gamma}{v^2_{\text{in,thermal}}}(1+\alpha+\beta), \quad \gamma = 2/3. \tag{21}$$

It is obvious from Table 2, that the noise model for long-channel devices (Eq. (21)) is not valid for deep-submicron CMOS technology. The parameters calculated from Eq. (14) are very close to the parameters simulated by HSPICE. This indicates that the proposed design procedure is valid, and the analytical noise model proposed in our previous work[8] improves the design accuracy. For the application, device sizes and biasing conditions can be calculated from the transconductances of the devices and the effective overdrive voltages.

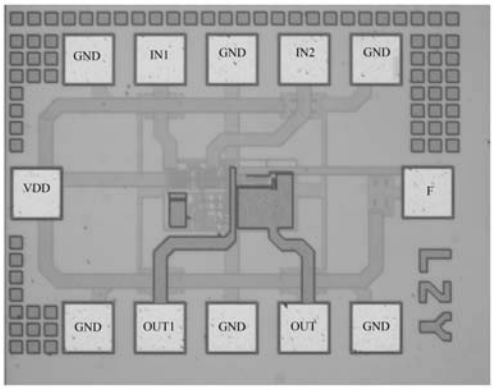

Fig. 2. Microphotograph of the implemented opamp.

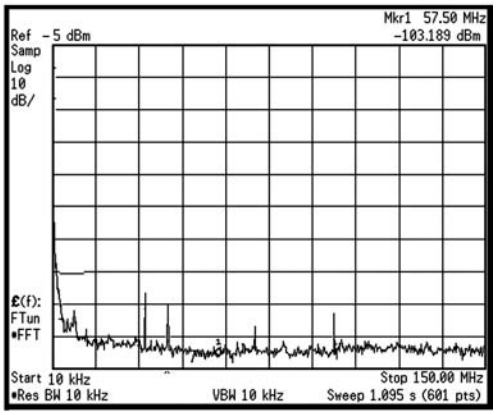

Fig. 3. Measured output noise spectrum density of the opamp.

4.2. Measured results

The opamp was fabricated in a standard 0.18 μm CMOS process. A microphotograph of the fabricated amplifier is shown in Fig. 2. The active area for the opamp is about 0.0214 mm^2.

The opamp was measured using a frequency spectrum analyzer (Agilent E4440A) and an oscilloscope (Tektronix TDS2014B). The measured noise spectrum density was converted into dBm by FFT analysis, as shown in Fig. 3. Data given in dBm, as measured by a frequency spectrum analyzer, can be converted into the frequency spectrum density (V/$\sqrt{\text{Hz}}$)[10] by

$$S_{\text{id}}(\text{V}/\sqrt{\text{Hz}}) = \frac{\sqrt{(10^{N[\text{dBm}]/10})(1\text{mW})R}}{\sqrt{K_n \text{RBW}}}, \tag{22}$$

where RBW is the resolution bandwidth, R is the source resistance, K_n is the coefficient used to convert resolution bandwidth to resolution noise bandwidth, i.e., K_n is 1.056 for FFT analysis. Given in Fig. 3 is the output noise spectrum density.

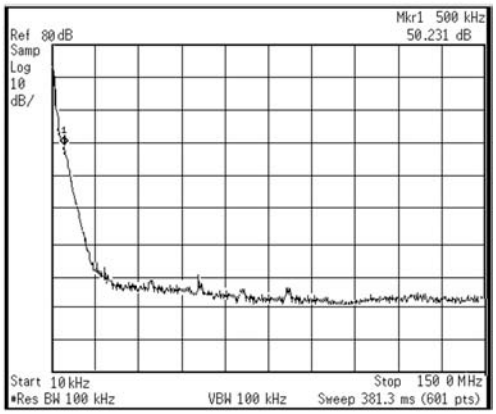

Fig. 4. Measured AC gain of the opamp versus frequency.

By dividing the output noise spectrum density by the AC gain, the equivalent input-referred noise can be obtained. The measured AC gain, is shown in Fig. 4.

The measured and simulated results are summarized in Table 3. Both results closely meet the required specifications. The discrepancy of the measured and simulated results might result from parasitic effects. The simulated noise contribution from the second stage and the output stage to the input-referred noise are 5.9×10^{-10} and $2.24 \times 10^{-14}\,\mathrm{V}/\sqrt{\mathrm{Hz}}$, respectively. This justifies the assumption of ignoring the noise from the second stage and the output stages. The measured input noise spectrum density is slightly higher than the expected input noise spectrum density, which could be the result of substrate coupling and flicker noise.

5. Conclusion

A tradeoff design procedure based on noise considerations for optimizing low noise operational amplifiers has been presented. The modeled and measured results confirm that the proposed design procedure is valid. Device sizes and biasing conditions obtained from hand calculations are very useful in terms of a conclusive and timely circuit design. The design procedure makes it possible to use both short and long-channel devices in analog circuits. Moreover, the procedure can be extended to other key specifications or opamp topologies. The design procedure can be integrated into an analog computer aided design tool, which could pave the way for an easier design of operational amplifiers.

Table 3. Measured and simulated results of our CMOS opamp.

Electrical parameters	Simulation results by HSPICE	Measured results
GBW (MHz)	86.7	79.4
Power consumption (mW)	1.12	1.27
Slew rate (V/μs) (+/–)	14.6/12.4	11/8
Equivalent input noise (nV/$\sqrt{\mathrm{Hz}}$) @10 MHz	32.67	37.16
DC gain: A_{dc} (dB)	114	108
Gain (dB)@10 kHz	82.8	76.8
Phase margin ($^\circ$)	51.2	—
Input common range (V)	0–1.44	0–1.25
Output voltage swing (V)	0–1.80	0.35–1.7

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