Design of an ultra-low-power digital processor for passive UHF RFID tags

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Abstract: A new architecture of digital processors for passive UHF radio-frequency identification tags is proposed. This architecture is based on ISO/IEC 18000-6C and targeted at ultra-low power consumption. By applying methods like system-level power management, global clock gating and low voltage implementation, the total power of the design is reduced to a few microwatts. In addition, an innovative way for the design of a true RNG is presented, which contributes to both low power and secure data transaction. The digital processor is verified by an integrated FPGA platform and implemented by the Synopsys design kit for ASIC flows. The design fits different CMOS technologies and has been taped out using the 2P4M 0.35 μm process of Chartered Semiconductor.

Key words: UHF RFID; ultra-low power; power management; TRNG
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1. Introduction

Applying RFID (radio-frequency identification) tags becomes increasingly more popular today, including areas such as supply chain management, access control to buildings, public transportation, airport baggage management, civil and military logistics. ISO/IEC 18000-6C is a protocol focused on UHF RFID for air interface communications at 860–960 MHz[1]. According to this protocol, an interrogator transmits information by modulating an RF signal in the 860 to 960 MHz frequency range, while a tag receives both information and operating energy from this RF signal. In order to send information back to an interrogator, a tag responds by modulating the reflection coefficient of its antenna.

During the communication between a tag and an interrogator, the tag is passive, meaning that it receives all its operating energy from the interrogator's RF waveform[2]. So it is important that an UHF RFID system works at ultra-low power in addition to the requirements of long operating range, high data rate, and low cost[3].

Generally, a passive UHF tag consists of four blocks: external antenna, analog front-end, digital processor, and EEPROM for memory, among which the digital processor accounts for more than 35% of the power that a tag consumes[4]. Therefore, an effective way to get a low-power tag is by designing an ultra-low-power digital processor.

In this paper, a new architecture for a digital processor is proposed, and several innovative approaches to realize ultra-low power consumption are presented.

2. Power analysis and architecture of the digital processor

The power dissipated in a CMOS circuit falls into two categories, namely static power and dynamic power, among which the latter accounts for more than 75% of the power consumption for both 0.18 μm and 0.35 μm technologies. Therefore, dynamic power, which is related to switching activities, is the dominant power for a design[5]. According to Synopsys' power analysis guideline[6], the dynamic power of a CMOS circuit is given by

$$P_{\text{dynamic}} = 0.5\alpha C_{\text{L}} V_{\text{dd}}^2 f, \tag{1}$$

where α represents the switching activities of the circuit, C_{L} is the circuit's total load capacitance, V_{dd} represents the voltage applied to the circuit, and f is the average frequency of the circuit when it runs.

In order to achieve ultra-low power consumption in our design of the digital processor, any module is shut down instantly when it becomes idle. At both algorithm level and

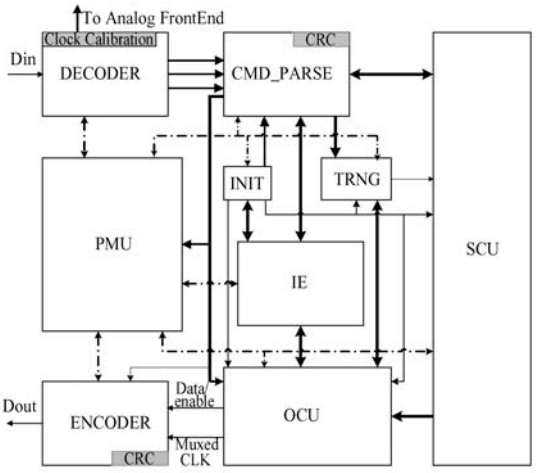

Fig. 1. Architecture of the digital processor. DECODER: PIE decoder unit; CMD_PARSE: command parse unit; PMU: power management unit; INIT: initiation unit; TRNG: true random number generator; SCU: state control unit; IE: interface to EEPROM; ENCODER: unit for encoding; OCU: output control unit.

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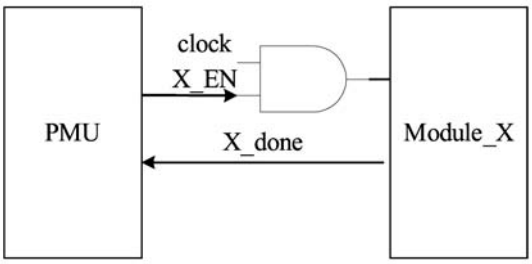

Fig. 2. Operation model of the PMU.

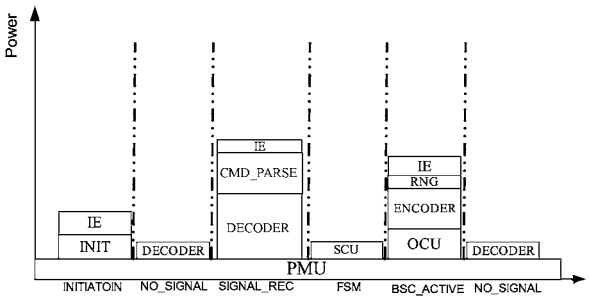

Fig. 3. Power management of the digital processor at system level.

register transfer level, techniques like clock gating and Gray Code FSM encoding are used to reduce both α and C_{L}. Additionally, by realizing various designs with different frequency characteristics, the relationship between decoding accuracy, operating speed and power is well balanced[7]. For the design, we choose CMOS transistors with low threshold voltage, thus reducing V_{dd} for digital circuits from 3.3 to 1.6 V. Due to these optimizations from system level to transistor level, this design has a low power consumption. The architecture for the design is given in Fig. 1.

3. Innovations

3.1. System level power management and global clock gating

In a digital circuit, the largest portion of power is consumed when the clocks rise and fall, resulting from the charging and discharging of load capacitances[8]. So our main concern is to avoid clock transitions inside any module when it becomes idle. This is the purpose of the power management unit (PMU).

Under any state of a tag, a mutual handshake signals between the PMU and any other module causes the PMU to allow or disallow clock transitions inside a respective module. Thus each module in this architecture runs without extra power dissipation caused by clock transitions. Figure 2 shows how this method works.

Figure 3 illustrates the power consumption of the whole system when a PMU is used. As can be seen, each module runs only when it is needed.

In addition to power management at system level, clock gating is automatically applied to the entire circuit when using the Synopsys Design Compiler. Figure 4 gives a comparison showing how this technique reduces the activity of the circuit. As seen in Fig. 4(a), the flip-flop receiving the clock dissipates

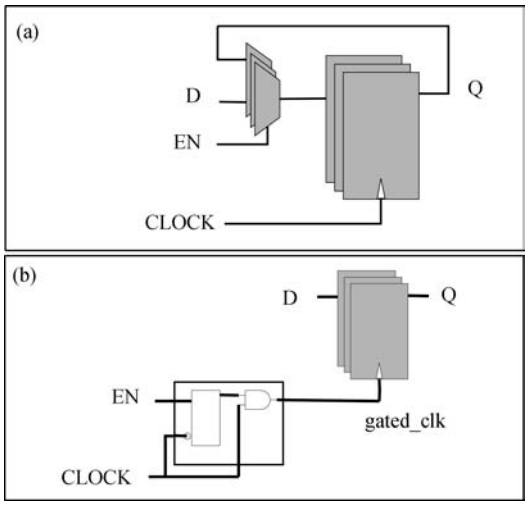

Fig. 4. Reduction of activity by clock gating: (a) Circuit with high activity; (b) Circuit with low activity.

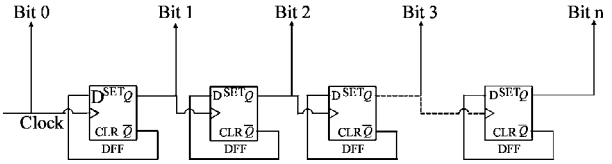

Fig. 5. Structure of the ripple counter.

some dynamic power even if the input and output remain constant. However, by applying the Design Compiler to identifying circuits where clock gating can be inserted without changing the function of the logic, clocks are turned off when they are not necessary. Thus we get an efficient approach to achieve low power consumption, as illustrated in Fig. 4(b).

3.2. Ripple counter

Traditionally, a counter is designed in either a serial carry model or a carry-look-ahead model. In both models, the clock nets are connected to every flip-flop. However, the charging and discharging of the load capacitances due to clock transitions consumes a considerable amount of power. Therefore, this method needs to be optimized in order to be applied to a passive circuit. Hence, a new model called ripple counter is adopted to realize a low-power counter. The counter is shown in Fig. 5.

In a ripple counter, the main clock with the highest frequency is applied only to the input CP of the first flip-flop, the input CP of the second flip-flop is driven by the output Q of the first flip-flop, and so on. With this structure, the power dissipation is effectively reduced due to the lower activity of the circuit.

3.3. A true RNG with low power

According to the protocol, a random number generator (RNG) is needed for generating any 16-bits random number, or RN16, as a handle or a cover-code during password transactions. Instead of generating pseudo-random numbers from an all-digital circuit, we proposed to use a TRUE RNG (TRNG), which incorporates parts from both the analog front-end and the digital processor of a tag. The

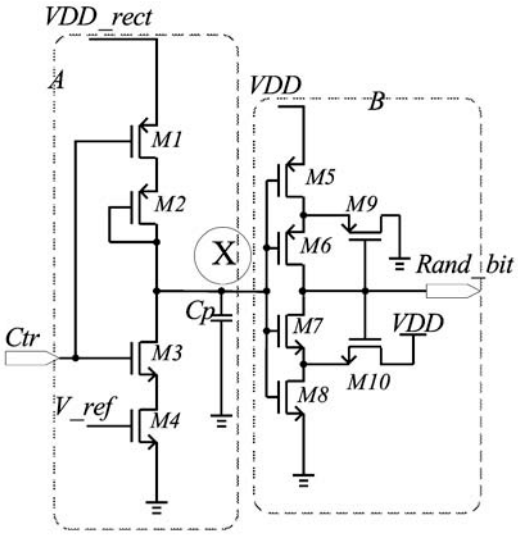

Fig. 6. Analog part of the TRNG.

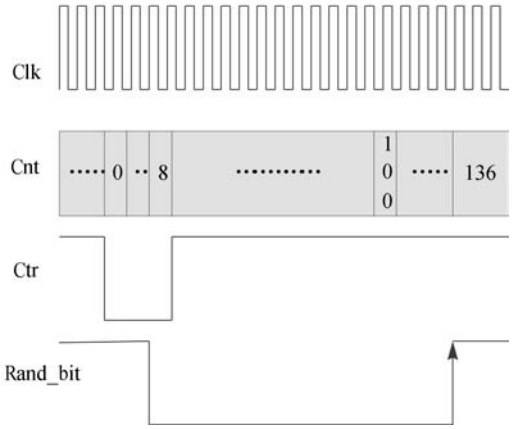

Fig. 7. Operation of the TRNG.

power a tag may acquire at any time and location is a variable, and the energy conversion efficiency of the power management circuit varies with the operation of the digital processor. Correspondingly, the output voltage of the energy conversion circuit, $V_{\mathrm{DD\_rect}}$, varies with time. Our TRNG design is based on the noise of $V_{\mathrm{DD\_rect}}$, as illustrated in Fig. 6. The analog part of the TRNG is composed of two parts: part A being a noise source and part B being a Schmitt trigger. When C_{tr} is kept low, the capacitance C_{p} will be charged to $V_{\mathrm{DD\_rect}}$. When C_{tr} transitions to a high level, C_{p} will be discharged through M3 and M4. Because of the fluctuation of $V_{\mathrm{DD\_rect}}$, the time for C_{p} to be discharged varies. By controlling C_{tr} via the digital processor, we can get a negative pulse with stochastic length from the signal Rand_bit. A true random number is obtained by counting the negative pulse, as shown in Fig. 7.

3.4. Applying lower voltage to the digital processor

As mentioned in section 2, using transistors with low V_{th} is an efficient way to reduce the power dissipation because these transistors work at lower supply voltage. So instead of the standard cells working at 3.3 V, our design uses transistors with lower V_{th}, which can successfully operate at 1.6 V. As estimated by a Nanosim simulation, this method leads to a total current consumption as low as 13.3 μA for a 0.35 μm process and 5.16 μA for a 0.18 μm process.

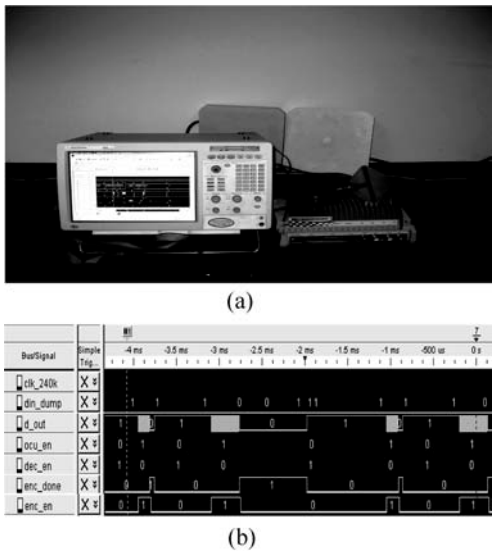

Fig. 8. FPGA verification: (a) FPGA verification platform; (b) Waveforms measured during the FPGA verification.

4. Verification and chip realization

4.1. Verification

Under various articles of the protocol, the design and verification of the digital processor at RTL level is completed by a combination of Cadence NCVerilog and Mentor Debussy. Code coverage is 100%, and function coverage is 99%.

Prior to the implementation of an ASIC flow, the functionality of the design is verified by using an FPGA platform consisting of a SPEEDWAY reader from Impinj and a programmable Cyclone EP1C chip from Altera. A photo of this FPGA platform and its corresponding waveforms are given in Fig. 8. The verification of the design with an FPGA prior to tapeout contributes significantly to a successful realization of the chip.

4.2. ASIC implementation

After the successful FPGA verification, the ASIC flow of this design requires the usage of a Design Compiler to transform the RTL level design into gate level standard cells from a specific foundry. Then, static timing analysis (STA) is done using PrimeTime to make sure all timing constraints are met. For the next step, the digital processor is optimized with regard to its power consumption based on power values calculated by both PrimePower and Nanosim[9]. At last, Astro is applied for the floorplan, place, CTS, and route, and Mentor Calibre for DRC and LVS. The chip has been taped out through the 2P4M 0.35 μm process of Chartered Semiconductor. A micrograph of the chip is shown in Fig. 9.

5. Conclusions

In this paper, a new architecture for a passive UHF RFID digital processor is presented, and several innovative and effective methods are developed to achieve ultra-low power

Table 1. Comparison of power consumption and design performance.

IP Owner		Masui[10]	Abrial[8]	Usami[11]	Fukumizu[12]	This paper	This paper
Release time/Test method		1999	2001	2004	2004	Simulation	Real chip
Process (μm)		0.8	0.25	0.18	0.18	0.18	0.35
Characteristics	Decoding frequency (MHz)	< 1.92	< 1.92	< 1.92	< 1.92	1.92	1.92
	CRC	Yes	No	No	Yes	Yes	Yes
	Memory	EERPOM	EERPOM	No	EERPOM	MTP	EERPOM
	Anti-collision algorithm	Yes	Yes	No	Yes	Yes	Yes
	TRNG	No	No	No	No	Yes	Yes
Power		< 2 mW*	0.8 mW	1.5 mW*	23.4 μW*	6.78 μW	18.6 μW

Note: * indicates the total power consumed by a tag.

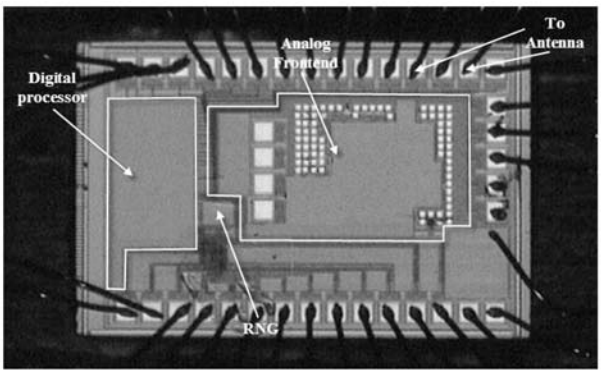

Fig. 9. Micrograph of the RFID tag chip.

consumption. These methods include clock gating at system level, a ripple counter, and a low operating voltage. In addition, an innovative way to realize the TRNG is proposed. This TRNG has the advantages of both low power consumption and efficient data processing. The design is verified by an integrated FPGA platform and implemented through a formal ASIC flow using the Synopsys design kit. Compared with the power consumptions given by Refs. [8, 10–12] and our simulation results for a 0.18 μm process, our design exhibits ultra-low power consumption. In addition, the power consumption will be optimized further with more advanced technology, as shown in Table 1.

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