Design of anti-jamming current-sensing circuit for current-mode buck regulator*

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Abstract: A novel anti-jamming integrated CMOS current-sensing circuit for current-mode buck regulators is presented. Based on the widely-used traditional current-sensing structure, anti-jamming performance is improved significantly by adding on-chip capacitors and one-shot circuit. Also the transient response is faster through the introduction of current offset. The circuit is concise, simple to implement and suits for SoC applications with single power supply. A dual-output current-mode DC-DC buck converter with proposed structure has been fabricated with a 0.5 μm CMOS process for validation. In the 2.5–5.5 V input range, the two channels work steadily in the load current range of 0–600 mA. And the measured maximum efficiency is up to 96%.

Key words: buck regulators; current-mode control; current-sensing circuit; anti-jamming
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1. Introduction

In today's consumer market, power management ICs especially switching regulators, are widely used in battery-operated portable electronic devices such as cellular phones, personal digital assistants (PDAs), MP4 players and digital still cameras. Industry has been paying more attention on the size and efficiency of power regulators[1,2]. For voltage conversion performed by highly integrated regulators with individual loads, the design of anti-jamming analog building blocks including current-sensing circuit thus becomes challenging and important research since the bounces in the supply and ground are critical in monolithic systems.

In switch-mode power regulators, current-mode pulse width-modulation (PWM) control schemes are widely used in industry due to the advantages of automatic over-current protection, better closed-loop stability and faster dynamic responses[3]. The output of the error amplifier, artificial compensation ramp and the sensed inductor current signal will pass through the modulator and the digital control block to define the duty cycle and avoid subharmonic oscillation. So as a particularly important block for PWM control, the current-sensing circuit not only determines the peak current of regulator but also affects the stability of feedback loop[4].

Therefore, an anti-jamming integrated CMOS current-sensing circuit for current-mode buck regulators is presented in this paper. The proposed circuit provides solutions to the jamming problem of traditional current-sensing schemes. Also the transient response speed is optimized. A monolithic dual-output current-mode DC–DC buck converter with proposed structure has been fabricated with a 0.5 μm CMOS process for validation. Measurement result shows that the proposed anti-jamming current-sensing circuit has good performance. In the 2.5–5.5 V input range, both the two channels work steadily in the load current range of 0–600 mA simultaneously. It has a good transient response and the measured maximum efficiency is up to 96%.

2. Traditional current-sensing circuit

Efficiency degradation, problems on full integration and complicated circuit implementation are the familiar difficulties and problems on circuit realization of current-sensing function. A lot of different current-sensing techniques such as series sensing resistor, sensing transformer and even sensing scheme with integrators have been published or developed[4–6]. Each of these methods suffers from some major disadvantages which limit their applications in switching power regulators design[7]. Different methods should be chosen by the designer in the consideration of the application environment.

In the buck regulator design, only the rising slope of the inductor current is sensed and required in the feedback loop as it contains the supply information. Figure 1 shows an accurate integrated current-sensing scheme which is most widely-used. MP and MN are power switches integrated on-chip. L and C are the off-chip inductor and capacitor of the DC–DC buck regulator. MS are the matched PMOS transistor with aspect ratio much smaller than that of MP. M1–M6 act as a common gate amplifier[8,9] which enforces the same voltage at nodes B and C. Inductor current $I_{\rm L}$ is sensed and scaled to $I_{\rm SEN}$. The positive input of PWM comparator $V_{\rm ADD}$ is given as

$$V_{\rm ADD} = I_{\rm SEN}R_3 + I_{\rm SLOPE}R_3 + I_{\rm DC}R_3. \quad (1)$$

The first item stands for the voltage generated by the sense current flowing through M3. The second item denotes the slope

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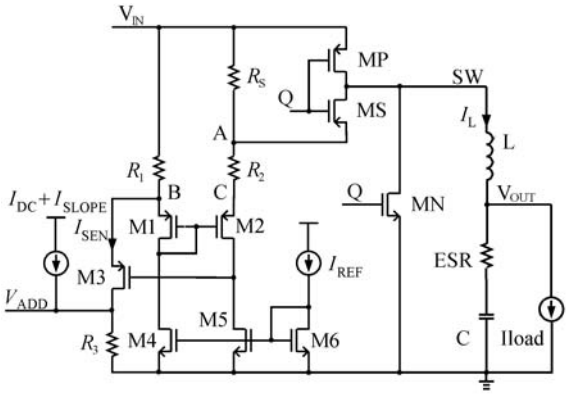

Fig. 1. Traditional current-sensing circuit.

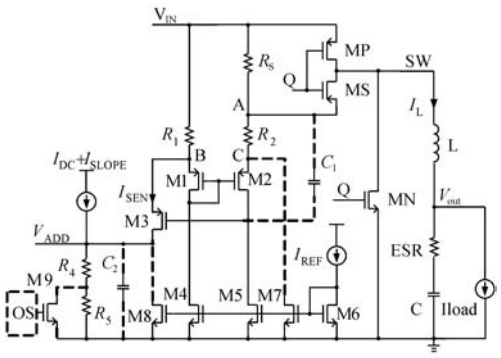

Fig. 2. Schematic of proposed anti-jamming current-sensing circuit.

compensation ramp voltage which changes with the duty cycle and is used to avoid subharmonic oscillation. The third item refers to the fixed DC voltage applied to the PWM comparator for a suitable DC operating point[4].

The principle of operation will be described in detail in Section 3. There are two main disadvantages in the circuit shown in Fig. 1. First of all is the low response speed. The inductor current rises from zero every cycle when the chip enters discontinuous-conduction mode (DCM). But when MP is off, $I_{\rm SEN} \approx 0$. When MP is on, the common gate amplifier needs a little time to enter the normal operation state. The sense ratio would be unreal in this period. Second, the jamming problem is serious when there is a glitch or bounce in $V_{\rm IN}$. The source voltage of M3 can responds quickly to the change of $V_{\rm IN}$ due to the resistive way of R_1. But the gate voltage of M3 cannot responds simultaneously because of its high impedance to GND. Thus the sense current and $V_{\rm ADD}$ will dithers greatly, which will trigger the logic circuit to shut down MP. The duty cycle would not be fixed and loop would be unstable. So the layout should be very carefully done in the multi-output DC–DC regulators with single supply input. Otherwise the channels would be unstable due to the poor anti-jamming current-sensing circuit.

3. Proposed anti-jamming current-sensing circuit

An anti-jamming current-sensing circuit is proposed to get rid of the above two disadvantages. The detailed schematic is shown in Fig. 2. The dashed lines show the optimization to improve the performance. MP and MN consist of many transistors in parallel to improve the efficiency. For a PMOS transistor MX operated in triode region, the on-resistance can be obtained as

$$R_{\rm MX} \approx \frac{L}{\mu_{\rm P} C_{\rm OX} W (V_{\rm SG} - |V_{\rm TH}|)}, \tag{2}$$

where $\mu_{\rm P}$, $C_{\rm OX}$, W, L, $V_{\rm SG}$, $V_{\rm TH}$ stands for the effective channel mobility, gate oxide capacitance per unit area, channel width and length of a MOSFET transistor, source-gate voltage, threshold voltage, respectively. The designed on-resistance of power switches is about 0.3 Ω with $V_{\rm IN} = 3.6$ V at room temperature. $I_{\rm REF}$ is the temperature and supply independent current reference. M1, M2 operate in the saturation region, and M4–M8 form current mirror. $(W/L)_{\rm M1,2} = 50\ \mu$m/2 μm, $(W/L)_{\rm M3,9} = 3\ \mu$m/0.5 μm, $(W/L)_{\rm M4,5} = 80\ \mu$m/5 μm, $(W/L)_{\rm M6,7,8} = 10\ \mu$m/5 μm. For common gate structure, the source voltages of M1 and M2, $V_{\rm B}$ and $V_{\rm C}$, are equal. Feedback loop is formed by M3. When $V_{\rm A}$ drops, $V_{\rm C}$ and the gate voltage of M3 will drop. Then $I_{\rm SEN}$ increases and $V_{\rm B}$ drops until new balance is achieved. M7 introduces offset to the common gate amplifier.

During the regulator off-state, both MP and MS turn off with Q tied to $V_{\rm IN}$. Inductor current falls linearly with the slope of $-V_{\rm OUT}/L$. There is no need to sense current during this period. $V_{\rm B}$ and $V_{\rm C}$ can be expressed as

$$V_{\rm B} = V_{\rm IN} - (8I_{\rm REF} + I_{\rm SEN})R_1, \tag{3}$$

$$V_{\rm C} = V_{\rm IN} - 9I_{\rm REF}(R_{\rm S} + R_2). \tag{4}$$

Considering $R_{\rm S} \ll R_1 = R_2$ and $V_{\rm B} = V_{\rm C}$, $I_{\rm SEN}$ is given by

$$I_{\rm SEN} = \frac{9I_{\rm REF}R_{\rm S}}{R_1} + I_{\rm REF} \approx I_{\rm REF}. \tag{5}$$

During the regulator on-state, both MP and MS turn on with Q tied to ground. Inductor current rises linearly with the slope of $(V_{\rm IN} - V_{\rm OUT})/L$. There is a current flowing from node A to the inductor of the power stage. Because the aspect ratio of MS is much smaller than that of MP, then according to Eq. (2) the current through MS is so small that any effect it has on the operation of the regulator can be ignored. $V_{\rm A}$, $V_{\rm B}$ and $V_{\rm C}$ can be expressed as

$$V_{\rm A} \approx V_{\rm IN} - \frac{R_{\rm MP}R_{\rm S}}{R_{\rm MS} + R_{\rm S}} I_{\rm L}, \tag{6}$$

$$V_{\rm B} = V_{\rm IN} - (8I_{\rm REF} + I_{\rm SEN})R_1, \tag{7}$$

$$V_{\rm C} = V_{\rm A} - 9I_{\rm REF}R_2. \tag{8}$$

Considering $R_1 = R_2$ and $V_{\rm B} = V_{\rm C}$, $I_{\rm SEN}$ is given by

$$I_{\rm SEN} = \frac{R_{\rm MP}R_{\rm S}}{(R_{\rm MS} + R_{\rm S})R_1} I_{\rm L} + I_{\rm REF}. \tag{9}$$

From Eqs. (5) and (9) we can see that no matter MP turns on or off, M3 operates normally and $I_{\rm SEN}$ is not zero because of the introduction of M7. The feedback loop of common gate amplifier operates full-time during the whole cycle. The response speed of current-sensing is improved, which helps the sense ratio to recover quickly when inductor current rises from zero.

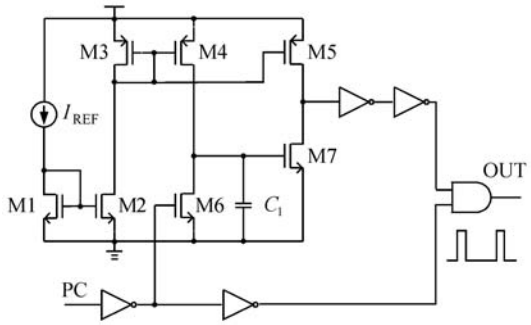

Fig. 3. Schematic of one-shot circuit.

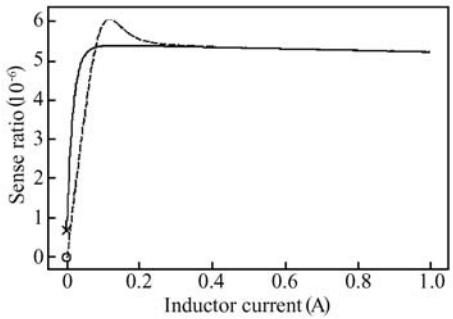

Fig. 4. Simulation result of response speed.

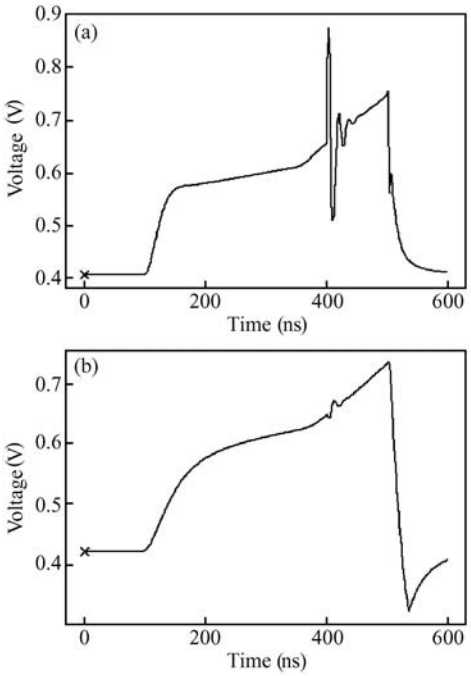

Fig. 5. Simulation result of anti-jamming performance: (a) Traditional current-sensing circuit; (b) Proposed current-sensing circuit.

Also the ripple of inductor current and output voltage would be reduced in DCM. In order to maintain the peak current limit, the voltage of V_{ADD} should be fixed and M8 is added to counteract the additional current of I_{REF}.

Generally speaking, V_{ADD} which compares with the output of error amplifier should be a continuous and strictly increasing function. But the glitch of V_{IN} will easily affect the sense current and V_{ADD} with the traditional circuit of Fig. 1, which would trigger the PWM comparator. In order to enhance the anti-jamming performance, C_1 is added between the gate of M3 and node A, which helps the gate of M3 to respond quickly to the change of V_{IN}. C_2 is added between the drain of M3 and ground, which helps to stable V_{ADD}. Also at the same time there is a disadvantage of doing so. When MP turns off, V_{ADD} falls down slowly due to the existence of C_2. One-shot circuit is specially designed to solve this problem. Figure 3 shows the detailed schematic. $(W/L)_{M1,2,3} = 10\ \mu m/5\ \mu m$, $(W/L)_{M4} = 50\ \mu m/5\ \mu m$, $(W/L)_{M5} = 20\ \mu m/5\ \mu m$, $(W/L)_{M6} = 1.5\ \mu m/0.5\ \mu m$, $(W/L)_{M7} = 10\ \mu m/1\ \mu m$. PC is the gate drive signal of MP. OUT is a clock signal with about 30 ns pulse width. When PC is high, MP turns off and C_1 is charged by I_{REF}. M7 turns on when the voltage across C_1 reaches the threshold. OUT changes from high to low. When PC is low, MP turns on and C_1 is discharged. When OUT is high, M9 in Fig. 2 turns on. Because R_3 in Fig. 1 is split to R_4 ad R_5, discharge speed of C_2 is accelerated. Of course the exactly value of R_4 and R_5 should be considered according to the simulation falling speed of V_{ADD}.

4. Results and discussion

A monolithic dual-output current mode buck regulator with proposed anti-jamming current-sensing circuit has been implemented in Magnachip CMOS 0.5 μm technology. The comparison simulation results of traditional current-sensing circuit and proposed method with $V_{IN} = 3.6$ V are shown in Figs. 4 and 5. The curve of sense ratio versus inductor current is shown in Fig. 4. Dashed line and real line indicate the transient result with the circuit of Figs. 1 and 2, individually. The response speed is improved significantly. The real line shows that sense ratio is stabilized when inductor current reaches about 60 mA, which is much faster than the dashed line. Simulation result of anti-jamming performance is plotted in Fig. 5. Figure 5(a) shows the waveform of V_{ADD} with traditional current-sensing circuit. V_{ADD} dithers greatly when there is a glitch in V_{IN}, which will trigger the PWM comparator and turn off MP. Thus the duty ratio in this cycle would be smaller than designed and loop would be unstable. Figure 5(b) shows significant performance improvement. V_{ADD} dithers a little for the glitch of V_{IN}. Even the glitch happens at the moment that MP is designed to turn off, the duty cycle would only be affected less than 3%.

Table 1. Performance summary of the presented DC-DC converter.

Parameter	Value
Input voltage range	2.5–5.5 V
Inductor(off-chip)	2.2 μH
Input capacitor(off-chip)	10 μF
Output capacitor(off-chip)	10 μF
Switching frequency	1.5 MHz
Max output current	600 mA
Output voltage ripple	10 mV
Efficiency	96% (MAX)
High side switch on resistance	0.28 Ω
Low side switch on resistance	0.30 Ω

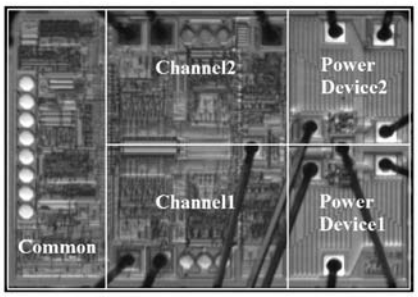

Fig. 6. Micrograph of the achieved DC-DC converter.

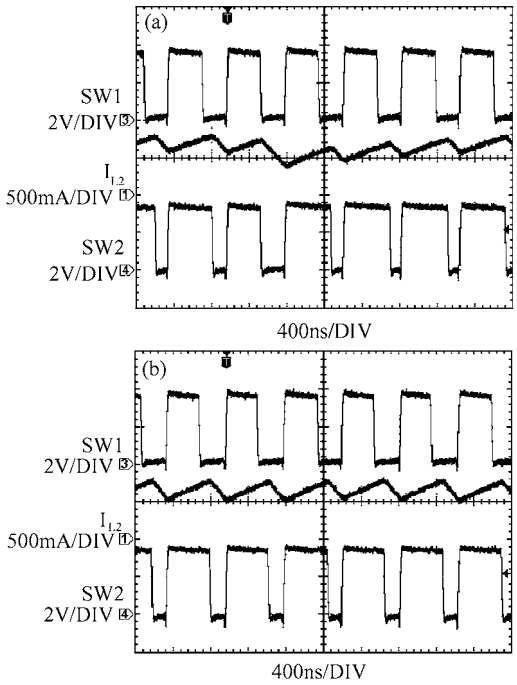

Fig. 7. Measured waveforms of I_L and SWs: (a) With traditional current-sensing circuit; (b) With proposed current-sensing circuit. V_{IN} = 3.6 V, V_{OUT1} = 1.8 V, V_{OUT2} = 2.4 V, I_{LOAD1} = I_{LOAD2} = 600 mA.

Figure 6 shows the micrograph of presented regulator. The size of the whole chip is 1245 × 1850 μm^2. It is composed by common blocks, two individual control blocks and power devices. Common blocks consist of bandgap voltage reference, current reference and oscillator. The current-sensing circuit, soft-start circuit and compensation network[10] are integrated on-chip, which reduces the complexity of the design and saves the PCB space. The performance of the two channels is shown in Table 1. The 2.5 to 5.5 V input voltage range makes it ideally suited for single Li-ion battery-powered applications. Low-dropout operation extends battery life in portable systems. Switching frequency is internally set at 1.5 MHz, allowing the use of small surface mount inductors and capacitors. Also the synchronous switch increases efficiency and eliminates the need for an external Schottky diode. The steady state has been tested with X5R ceramic capacitors under (−40 °C, 85 °C). Other circuits to be the same, the chips with traditional current-sensing circuit and proposed anti-jamming current-sensing circuit have been tested. Figure 7 shows the measured waveforms under the condition of V_{IN} = 3.6 V,

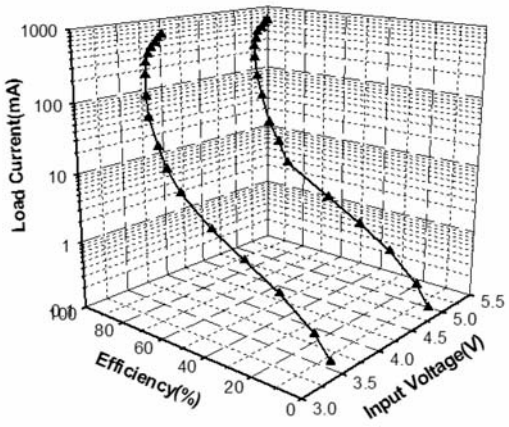

Fig. 8. Measured efficiency curves.

V_{OUT1} = 1.8 V, V_{OUT2} = 2.4 V, and I_{LOAD1} = I_{LOAD2} = 600 mA. I_{L2} is the inductor current measured with Tektronix TCP202 active probe. SW1,2 is the switch pin which connects to the inductor. Figure 7(a) shows that the two channels can not work stable and channel2 maybe shutdown by the channel1 because of the switching noise in the common V_{IN}. Figure 7(b) shows that anti-jamming method restrains the two channels' oscillation successfully. Also the measurement results indicate that the regulator with proposed circuit regulates properly for different duty cycles without any oscillation. The measured efficiency is shown in Fig. 8 with the input voltage of 3.6, 5 V and the output voltage of 1.8 V. With internal synchronous rectification technique, the efficiency is above 80% for load currents between 10 and 600 mA. And the maximum efficiency is up to 96%.

5. Conclusion

A novel anti-jamming current-sensing circuit for CMOS buck power regulators is introduced in this paper. The principle of operation has been presented. And the proposed circuit has been applied to a dual-output current-mode buck regulator. The performance improvement is proven and verified by simulation and experimental results. The concise circuit can be applied to some other SoC applications.

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