Effects of pattern characteristics on copper CMP

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Abstract: Copper chemical mechanical polishing (CMP) is influenced by geometric characteristics such as line width and pattern density, as well as by the more obvious parameters such as slurry chemistry, pad type, polishing pressure and rotational speed. Variations in the copper thickness across each die and across the wafer can impact the circuit performance and reduce the yield. In this paper, we propose a modeling method to simulate the polishing behavior as a function of layout pattern factors. Under the same process conditions, the pattern density, the line width and the line spacing have a strong influence on copper dishing, dielectric erosion and topography. The test results showed: the wider the copper line or the spacing, the higher the copper dishing; the higher the density, the higher the dielectric erosion; the dishing and erosion increase slowly as a function of increasing density and go into saturation when the density is more than 0.7.

Key words: copper chemical mechanical polishing; line width; line spacing; density; copper dishing; dielectric erosion

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1. Introduction

Copper chemical mechanical polishing (CMP) is very effective at reducing the feature level or the local step height and achieves global planarization[1, 2]. However, CMP planarization is influenced by geometric characteristics such as line width and pattern density. It is known, that various degrees of copper dishing and dielectric erosion occur at different densities and metal line widths. Figure 1 shows a CMP simulation result on a full chip, which indicates different surface heights at various places of the chip due to dishing and erosion at different metal feature sizes and densities[3]. Dishing is defined as the difference between the height of the copper in the trench and the height of the dielectric surrounding the copper trench in question. Erosion on the other hand, is defined as the difference between the dielectric thickness before CMP and after CMP.

Dishing and erosion on a given metal level could lead to cumulative non-uniformity on higher metal levels[4], which might cause integration, yield, and manufacturing problems. As critical dimensions shrink aggressively to ever smaller nodes, interconnect delay, reliability, and manufacturability are becoming major issues in ultra-large-scale integrated circuit (ULSI) design and fabrication[5]. There is an urgent need to understand the effects of pattern characteristics on dishing, erosion and topography.

To reduce interconnect thickness variations, dishing and erosion must be minimized, but this requires an understanding of the layout and process dependencies involved in copper CMP, and a process model to accurately predict the dishing and erosion. The fundamental mechanisms of the micro-wear of the CMP process are not well understood even though there are so many published papers about CMP modeling. In the light of Jiang's research[6, 7], there are four types of approaches for CMP models: the purely fluid mechanical approach, the fluid dynamics lubrication approach, the contact mechanics approach, and the viscous flow approach. Using the results of the CMP modeling research of the Massachusetts Institute of Technology (MIT), Cadence developed a CMP predictor that can be used for technology below 65 nm. Cooperating with the Berkeley CMP research team, Synopsys is now developing and optimizing their CMP predictor. Mentor Graphics, Magma and TSMC have also developed CMP predictors to do design for manufacturability (DFM) research including model-based design layout optimization and dummy fill for density uniformity. Based on the Preston equation, MITs density-step-height model and the contact mechanics model, we developed a CMP predictor. Some researches report on pattern structure effects[8, 9], but there is no systemic study available on the influence of density, line width and line spacing. In this paper, we focus on the influence of the layout density, the line width and the line spacing on dishing, erosion and copper line thickness. Using our CMP model, we test many combinations and gain some quantitative conclusions, which will be helpful for designers and manufacturing engineers.

2. CMP process and modeling

Copper CMP involves the simultaneous polishing of multiple materials: copper, dielectric and barrier[10]. It is necessary to clear the overburden copper and remove the barrier on top of the dielectric spaces separating the copper interconnect lines. Nowadays, a three-step polishing process is widely used in front-ends, as shown in Fig. 2. The first step uses a high copper removal rate (typically above 600 nm/min) to remove a large amount of the overburden copper without completely

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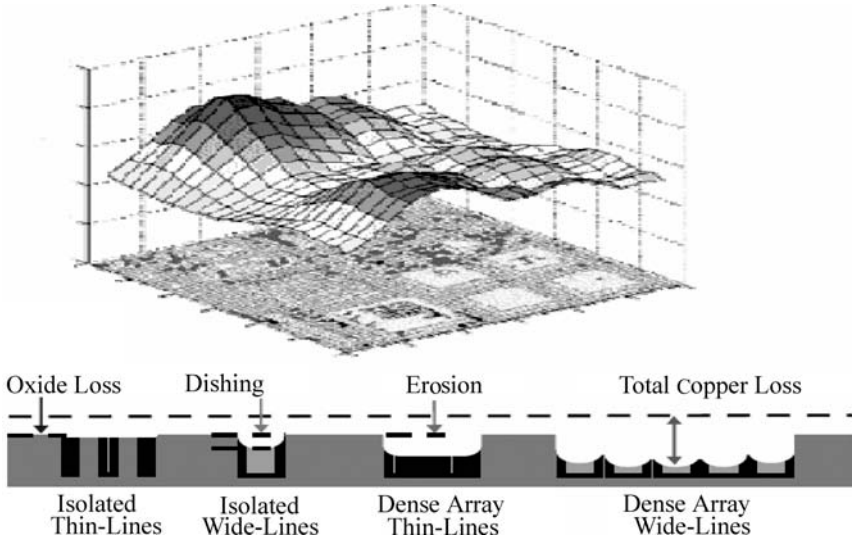

Fig. 1. Thickness and topography variation caused by CMP process[3].

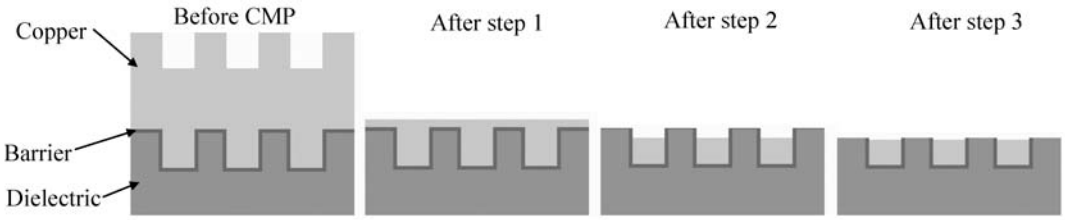

Fig. 2. Three stages in copper CMP processes.

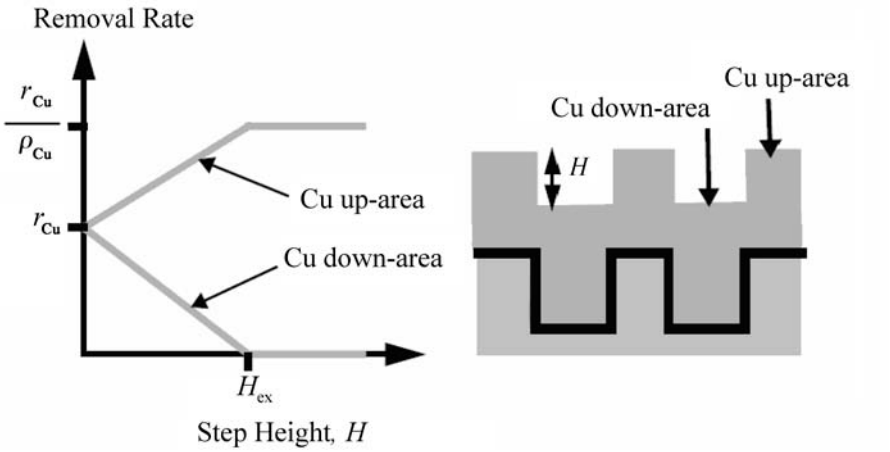

Fig. 3. First step removal rate diagram.

clearing it. The second step is intended to clear all overburden copper residue across the wafer, while achieving lower dishing and erosion as compared to the first step. In this step, a low-removal-rate copper process is used. The third step uses a different polish process setting, a different type of slurry, and maybe a different type of pad. The process has low removal rates for copper, barrier and dielectric[5].

All the models proposed for copper CMP are based on Preston's glass polishing model[11]. According to the model, the polish rate at any position on the wafer is given by

$$\mathrm{RR} = KPV, \tag{1}$$

where RR is the material removal rate, K the Preston coefficient, P the polish pressure, and V the relative speed between the platen and the carrier. The chemical contributions are lumped in Preston's coefficient.

Based on the Preston model, MIT developed the density-step-height model[5, 12, 13]. For the first step, the pad first touches the up-area of the wafer surface and the average pressure is thus P/ρ_{cu}, where ρ_{cu} is the copper pattern density. The up-area removal rate is $r_{\mathrm{cu}}/\rho_{\mathrm{cu}}$ and the down-area is zero, where r_{cu} is the blanket copper removal rate. As polishing progresses, the step height H decreases as illustrated in Fig. 3. When the step height becomes less than the critical step height H_{ex}, the pad touches the down-area surface and the pressure exerted on the down-area becomes non-zero. By Hooke's law, this non-zero down-area pressure increases linearly as the step-height decreases, while the up-area pressure decreases linearly as the step-height decreases. Step height reduction continues until the step height is eliminated and the

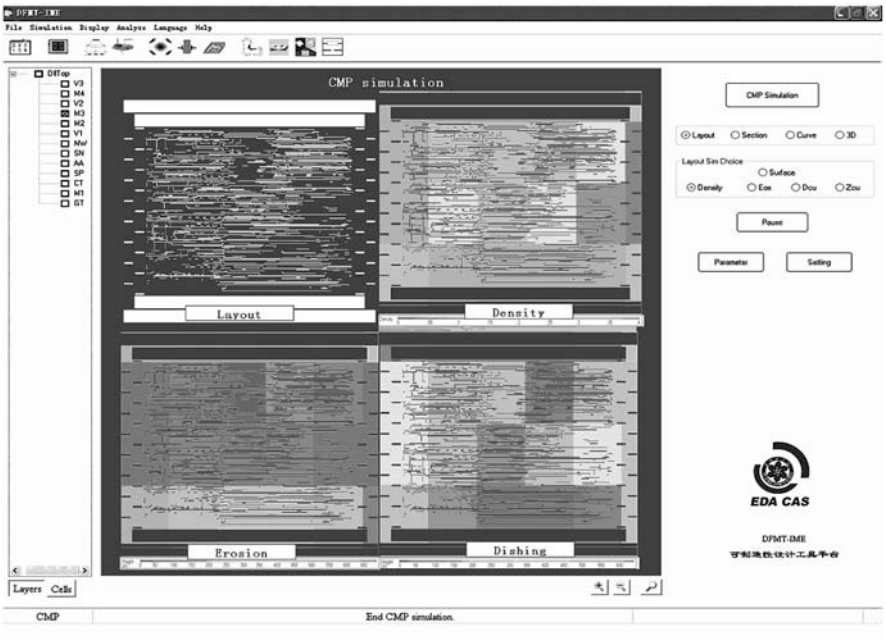

Fig. 4. Copper CMP process simulator.

copper surface is flat. The up-area copper removal rate decreases from r_{cu}/ρ_{cu} to r_{cu} and the down-area removal rate increases from zero to r_{cu}. Understanding the up-area and down-area removal rate, the wafer topography will be achieved using this semi-experiential modeling. The second and third steps are handled in the same way, but there are different materials involved.

However, the density-step-height model fails to take die scale height variations introduced by the electroplating process into account. Contact mechanics[14–17] can accommodate the long range initial thickness variation caused by copper electroplating, and also accounts for the evolution of the surface topography as polishing progresses. If the pad is treated as a massive elastic body and the wafer as a rigid body, then the pad displacement W and the contact pressure P are related as given by

$$W(x,y) = \frac{1-v^2}{\pi E}\iint_A \frac{P(\xi,\eta)}{\sqrt{(x-\xi)^2+(y-\eta)^2}}\mathrm{d}\xi\mathrm{d}\eta, \quad (2)$$

where v is the Poisson ratio and E is the elasticity of the pad. If the displacement is known, the contact pressure P can be computed and vice-versa. Once the pressure has been computed, it can then be substituted into the wear law to compute the material removal rate.

Building on the MIT density-step-height model and the contact mechanics model, the EDA Center of Chinese Academy of Sciences has developed a copper CMP simulation software. Figure 4 shows a screenshot of the implementation of the copper CMP model with a graphical user interface. For the copper CMP simulator, the input is design layout information and the output includes information on copper thickness, dishing, erosion, etc. This simulator will enable users to input layout and process information, and predict the surface topography during manufacturing.

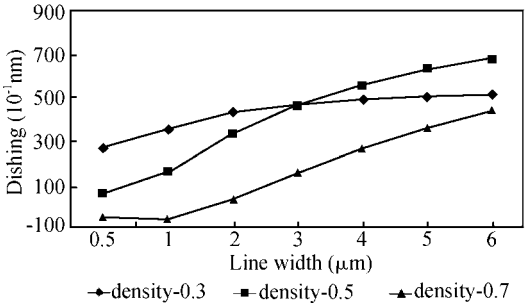

Fig. 5. Copper dishing versus line width.

3. Effects of pattern characteristics

It has been reported that the performance of CMP, most notably the effect on wafer non-uniformities such as dishing and erosion, is highly dependent upon the pattern characteristics[18]. Pattern characteristics known to affect CMP include pattern uniformity, line width, line spacing and pattern density (defined as the ratio of the linewidth to the pitch, where pitch is the distance between the centers of neighboring lines). These effects are at least in part due to the resulting non-uniformities in pressure[19,20]. Using a special process and equipment, we designed pattern characteristic combination tests. The used CMP polishing tool was an AMAT Reflexion. The MetaPulse 300 Π from Rudolph can measure copper thicknesses with good accuracy. An Atomic Force Microscope from Veeco was used to measure surface dishing and erosion. Using density, line width or line spacing as the x axis and thickness, dishing or erosion data as the y axis, a series of 2D curves were computed. Finally, we get some important conclusions from process model simulations.

Firstly, we investigated the effects of three different pattern densities and seven different line widths. For a fixed pattern density, an increasing line width leads to increased dishing and a decreasing copper thickness, as illustrated in Figs. 5

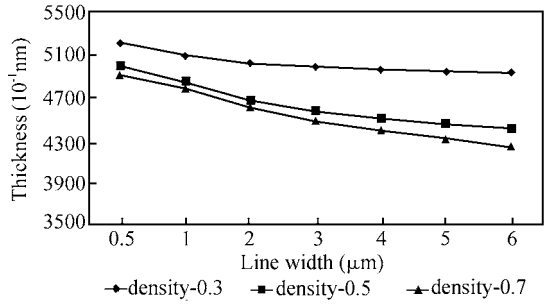

Fig. 6. Copper thickness versus line width.

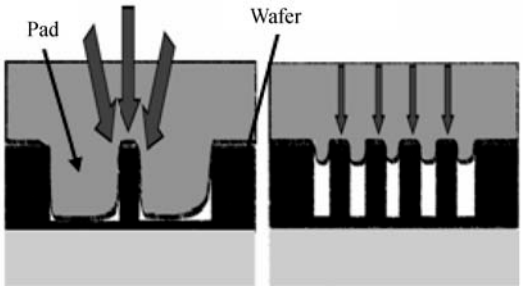

Fig. 7. Effect of the pattern on dishing with a compliant pad[8].

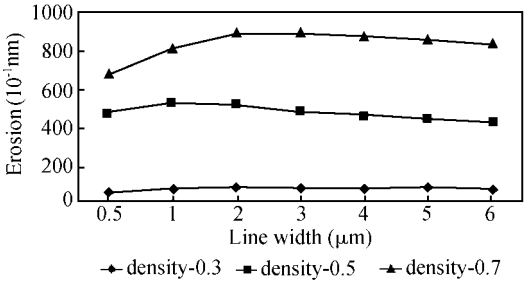

Fig. 8. Dielectric erosion versus line width.

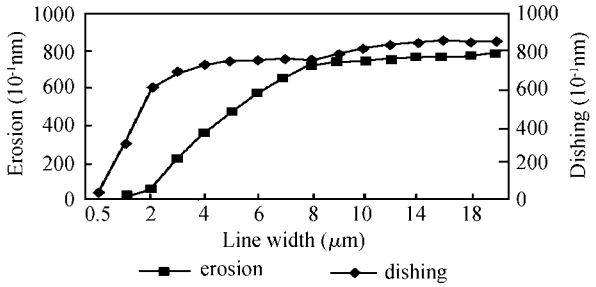

Fig. 9. Dishing and erosion versus line width.

and 6. As the line width increases, pad asperity easily touches the copper in the trenches, as depicted schematically in Fig. 7. Thus, as the line width increases, the dishing increases and the thickness decreases. Given the same line width, the erosion increases with increasing pattern density, as shown in Fig. 8. As Figure 7 shows, the effective pressure on the dielectric will increase with increasing pattern densities, which enhances the effect of the slurry on the dielectric and assists in mechanical abrasion. These effects account for the increase in erosion with increasing patter density.

Secondly, for a given line spacing, the dishing increases with the line width, as Figure 9 shows. Experimental data shows that as the line width increases, the slope of the dishing as a function of line width decreases. A saturation is reached

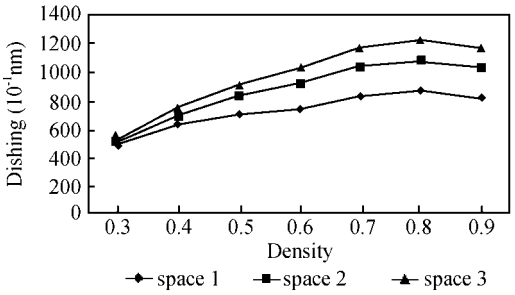

Fig. 10. Dishing versus density.

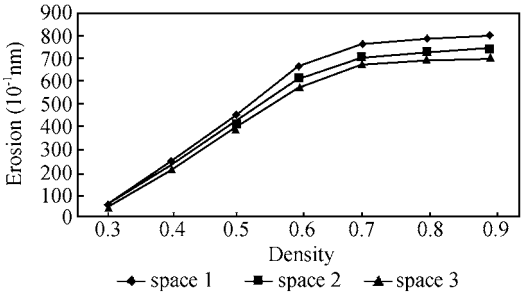

Fig. 11. Erosion versus density.

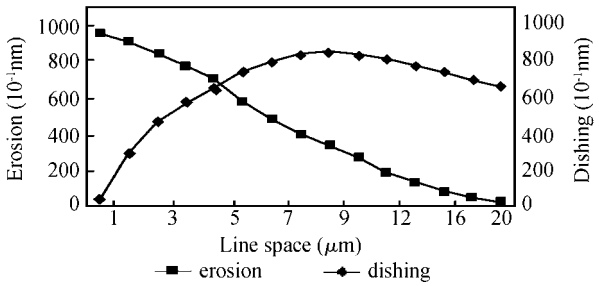

Fig. 12. Dishing and erosion versus line spacing.

as the line width increases to a certain level. The same holds true for the erosion. It first increases as a function of the line width and later levels off. The test results show that the dishing and erosion go into saturation when the density is higher than 0.7, as shown in Figs. 10 and 11.

In addition, for conventional copper CMP processes, as Figure 12 shows, the wider the line spacing surrounding a given line, the higher the dishing of that line and the lower the dielectric erosion. As the line spacing increases, the dishing rate with respect to the line spacing decreases less steeply, and the erosion decreases with increasing line spacing, because high line spacing means low dielectric pressure, and thus low dielectric material removal rate.

4. Summary and next steps

In this paper, we analyze the copper CMP process and some effects involved with it, namely copper dishing, dielectric erosion and copper line thickness variation. A process model is introduced, which is used to test the influence of pattern characteristics on dishing, erosion and topography variation. Under the same process conditions, the test results show: the wider the copper line or the line spacing, the higher the copper dishing; the higher the density, the higher the dielec-

tric erosion; dishing and erosion goes into saturation when the density reaches 0.7.

In a next step, we will study die-level and wafer-level effects on dishing, erosion and copper line thickness. Then a dummy fill will be designed to improve the pattern uniformity and to minimize pattern effects.

References

[1] Wu L, Yan C. An analytical model for step height reduction in CMP with different pattern densities. J Electrochem Soc, 2007, 154(7): H596

[2] Zantye P B, Kumar A, Sikder A K. Chemical mechanical planarization for microelectronics applications. Mater Sci Eng, 2004, 45(3–6): 89

[3] Rodriguez N, Song L, Shroff S, et al. Hotspot prevention using CMP model in design implementation flow. 9th International Symposium on Quality Electronic Design, 2008: 365

[4] Park T, Tugbawa T, Boning D, et al. Multi-level pattern effects in copper CMP. Electrochemical Society Proceedings of the Third International Symposium on Chemical Mechanical Planarization in IC Device Manufacturing, 1999, 99(37): 94

[5] Gbondo-Tugbawa T E. Chip-scale modeling of pattern dependencies in copper chemical mechanical polishing processes. PhD Thesis, Massachusetts Institute of Technology, 2002

[6] Jiang J Z, Zhao Y W, Wang Y G, et al. A chemical mechanical polishing model based on the viscous flow of the amorphous layer. WEAR, 2008, 265(7/8): 992

[7] Chen R L, Luo J B, Guo D, et al. Phase transformation during silica cluster impact on crystal silicon substrate studied by molecular dynamics simulation. Nuclear Instruments & Methods in Physics Research Section B-Beam Interactions with Materials and Atoms, 2008, 266(14): 3231

[8] Wang L, Doyle F M. Known effects of pattern characteristics on copper CMP and future directions. Proceedings of the 9th International Chemical-Mechanical Planarization (CMP) for ULSI Multilevel Interconnections, 2004

[9] Stavreva Z, Zeidler D, Plotner M, et al. Chemical mechanical polishing of copper for multilevel metallization. Appl Surf Sci, 1995, 91: 192

[10] Gotkis Y, Schey D, Alamgir S, et al. Cu CMP with orbital technology: summary of the experience. Advanced Process Development, 1998: 364

[11] Preston F W. The theory and design of plate glass polishing machines. Glass Technology, 1927, 11: 214

[12] Cai H. Modeling of pattern dependencies in the fabrication of multilevel copper metallization. PhD Thesis, Massachusetts Institute of Technology, 2007

[13] Xie X. Physical understanding and modeling of chemical mechanical planarization in dielectric materials. PhD Thesis, Massachusetts Institute of Technology, 2007

[14] Vlassak J J. A contact-mechanics based model for dishing and erosion in chemical-mechanical polishing. Materials Research Society, 2001: 671

[15] Vlassak J J. A model for chemical–mechanical polishing of a material surface based on contact mechanics. Journal of the Mechanics and Physics of Solids, 2004, 52: 847

[16] Park T H. Characterization and modeling of pattern dependencies in copper interconnects for integrated circuits. PhD Thesis, Massachusetts Institute of Technology, 2002

[17] Tugbawa T, Park T, Lee B, et al. Modeling of pattern dependencies for multi-level copper chemical-mechanical polishing processes. Materials Research Society (MRS) Spring Meeting, 2001

[18] Zeidler D, Stavreva Z, Plotner M, et al. Characterization of Cu chemical mechanical polishing by electrochemical investigations. Microelectron Eng, 1997, 33: 259

[19] Pan J T, Li P, Wijekoon K, et al. Copper CMP integration and time dependent pattern effect. Proceedings of the International Interconnect Technology Conference, 1999: 164

[20] Lai J Y, Saka N, Chun J H. Evolution of copper-oxide damascene structures in chemical mechanical polishing Ⅱ: contact mechanics modeling. J Electrochem Soc, 2002, 149(1): G41