A single-inductor dual-output switching converter with average current mode control

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Abstract: An integrated single-inductor dual-output (SIDO) switching DC–DC converter is presented. The outputs are specified with 1.2 V / 400 mA and 1.8 V / 200 mA. A decoupling small signal model is proposed to analyze the multi-loop system and to design the on-chip compensators. An average current control mode is introduced with lossless, continuous current detection. The converter has been fabricated in a 0.25 μm 2P4M CMOS process. The power efficiency is 86% at a total output power of 840 mW while the output ripples are about 40 mV at an oscillator frequency of 600 kHz.

Key words: DC–DC converter; single-inductor multiple-output; average current mode control; on-chip current detection

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1. Introduction

Portable applications usually need different supply voltages for different functional modules to minimize power consumption. The conventional way to generate N regulated output voltages is to use N independent converters. However, a more interesting and efficient solution is to use one converter with a single inductor to generate multiple outputs, which reduces the external components and saves cost and space.

In recent years, there have been several kinds of single-inductor multiple-output (SIMO) switching converters reported. The converters in Refs. [1, 2] make use of time-multiplexing control, which can be seen as a combination of two independent discontinuous conduction modes (DCM). There is a freewheeling state of inductor current when distributing energy from one channel to the other, which causes two channels independent of each other to suppress the cross regulation. But these converters suffer from very large current ripples and dissipate energy during the freewheeling state. The converter in Ref. [3] employs ordered power-distributive control which has a main channel for compensation and other subchannels controlled just by comparators. This simplifies the control loop, but has a higher ripple and is only suited for small load currents. The solution in Ref. [4] adopts digital control for a separate regulation of common-mode and differential-mode output voltages. The cross regulation problem is partially compensated by sophisticated control schemes. However, due to the limitations of digital control, the dynamic performance of the converter is not satisfactory.

This paper presents the analysis and design of an average current mode controlled SIDO buck converter. Compared with other designs, this SIDO converter maintains the advantages of continuous conduction mode (CCM) and also achieves fast load response. The system architecture and control sequence are introduced. A decoupling small signal model is proposed and the system stability is investigated. Circuit implementation is addressed. The measurement results confirm the system design.

2. Architecture of SIDO buck converter

A conventional buck converter consists of two power switches and one inductor, which provide efficient power conversion. In a SIDO buck converter, the function of dual outputs is realized by adding another two switches at the output node of the inductor[5]. As shown in Fig. 1, there are four power transistors in the converter: two input switches S1 and S2, which regulate the total energy, and two output switches S3 and S4, which are used to share the energy in the inductor.

The control sequence is shown in Fig. 2. According to the switches' states, each period can be divided into three phases. Assuming the ripples and equivalent series resistors (ESRs) of the output capacitors are negligible, the power stage can be described by piecewise linear differential equations. By the time-averaging method, the equations are expressed as[4]:

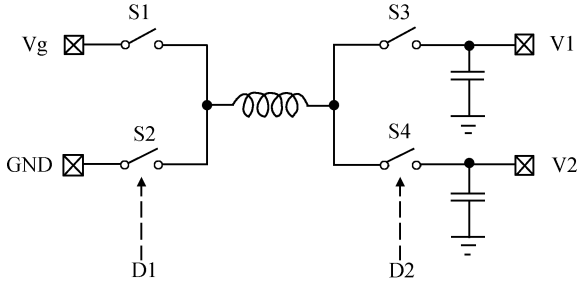

Fig. 1. Power stage structure of a SIDO buck converter.

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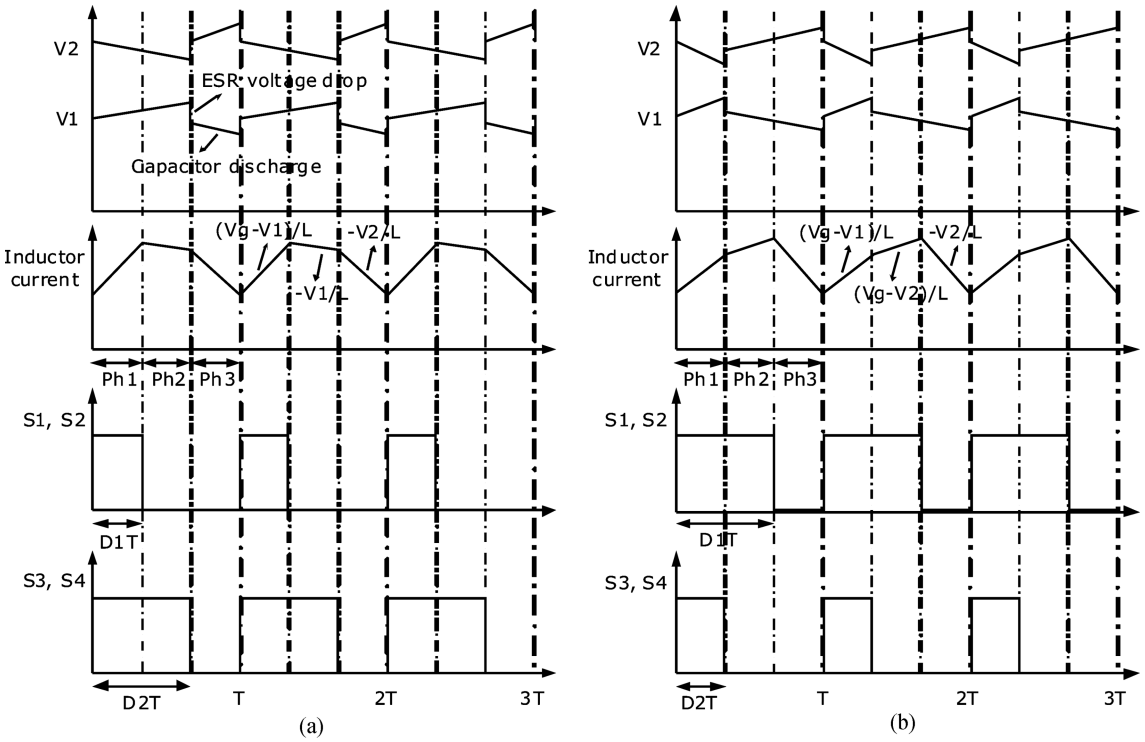

Fig. 2. Waveforms of output voltage ripples and inductor current with control signals: (a) $D_1 < D_2$; (b) $D_1 > D_2$.

$$\begin{aligned} C_1\frac{\mathrm{d}}{\mathrm{d}t}v_1 &= i_\mathrm{L}d_2 - \frac{v_1}{R_1},\\ C_2\frac{\mathrm{d}}{\mathrm{d}t}v_2 &= i_\mathrm{L}(1-d_2) - \frac{v_2}{R_2},\\ L\frac{\mathrm{d}}{\mathrm{d}t}i_\mathrm{L} &= v_\mathrm{g}d_1 - v_1d_2 - v_2(1-d_2). \end{aligned} \tag{1}$$

In steady state, $\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} v_1 & v_2 & i_\mathrm{L}\end{bmatrix}^T = 0$.

So, the steady-state variables can be solved from Eq. (1). D_1 is independent of load current, which is similar to of the situation in a conventional buck converter, while D_2 is only related to the ratio of the two load currents.

There are two situations according to the relation of D_1 and D_2. The slope of inductor current in Phase 2 is different in these two situations, which is labeled in Fig. 2. However, both control sequences can be unified into the description of Eq. (1), which means that they have the same behavior model. It will be analyzed below that the control loops of D_1 and D_2 can be regarded as independent of each other.

The waveforms of the steady-state inductor current and output voltage ripples in CCM are also depicted in Fig. 2. The ripples of SIDO output voltages mainly consist of two parts: the charge and discharge of capacitors and the voltage drop on the ESR of the capacitor. If the current ripple of the inductor is neglected, the output ripples in CCM can be estimated as:

$$V_\mathrm{ripple1} = \Delta V_\mathrm{C1} + \Delta V_\mathrm{ESR1} = \frac{I_1(1-D_2)T}{C_1} + I_\mathrm{L}R_\mathrm{ESR1}, \tag{2}$$

$$V_\mathrm{ripple2} = \Delta V_\mathrm{C2} + \Delta V_\mathrm{ESR2} = \frac{I_2D_2T}{C_2} + I_\mathrm{L}R_\mathrm{ESR2}. \tag{3}$$

So, the steady-state voltage ripples depend on the discharge time and inductor current when switching S3 and S4. DCM and pseudo-CCM control in Refs. [1, 2] have longer discharging time and higher peak current, and thus have much larger ripples. However, due to the efficient usage of inductor current, which means there is no freewheel or idle state of inductor current, the control method shown in Fig. 2 has the advantages of low ripple and ability to sustain large load currents.

Voltage mode control is widely used in switching converters. It is simple, but requires large compensation components which are difficult for on-chip implementation[1]. Average current mode control exhibits the following important benefits[6]: (i) fast response which can partly suppress the cross regulation problem; (ii) easy compensation which can be realized by on-chip capacitors. Figure 3 illustrates the architecture of a SIDO converter with average current mode control.

In the SIDO converter system, there are two main control loops: the common-mode loop, which regulates the total energy by control signal D_1, and the differential-mode loop, which determines the distribution of inductor current between two output channels by control signal D_2. The common-mode and differential-mode voltages are defined as[4]:

$$\begin{aligned} V_\mathrm{CM} &= m_1V_1 + m_2V_2,\\ V_\mathrm{DM} &= m_1V_1 - m_2V_2, \end{aligned} \tag{4}$$

where m_1 and m_2 are the feedback coefficients.

The converter is designed for an output load of 400 mA at 1.2 V on the first channel and 200 mA at 1.8 V on the second with an input voltage ranging from 2.8 to 5 V. The off-chip inductor is 4.7 μH and the filter capacitors are 22 μF. All compensation components are integrated on-chip.

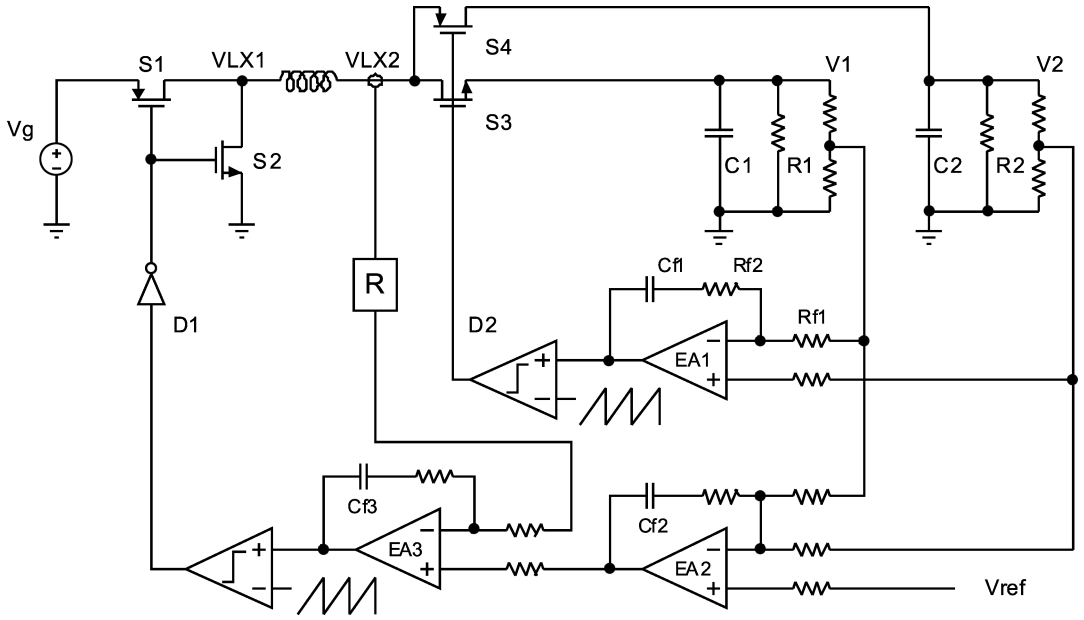

Fig. 3. System architecture of the average current mode controlled SIDO buck converter.

3. System design of the SIDO buck converter

The SIDO converter demonstrates attractive advantages at the expense of more complicated system design. From Fig. 3, the converter works as a multi-loop feedback system so that the stability and dynamic response are the key problems. In this section the small signal model of the SIDO power stage is given. Based on the proposed decoupling model, the procedure for the compensator design is derived.

3.1. Small signal model

Based on Eq. (1), let $x = X + \widetilde{x}$, where x, X and $\widetilde{x}$ are the average variable, steady state value and the small signal perturbation, respectively. Assuming the ripples and ESRs are negligible, the small signal behavior of the power stage can be described as:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix}\widetilde{v_1}\\ \widetilde{v_2}\\ \widetilde{i_\mathrm{L}}\end{bmatrix} = \begin{bmatrix} -\dfrac{1}{R_1C_1} & 0 & \dfrac{D_2}{C_1}\\ 0 & -\dfrac{1}{R_2C_2} & \dfrac{1-D_2}{C_2}\\ -\dfrac{D_2}{L} & -\dfrac{1-D_2}{L} & 0\end{bmatrix}\begin{bmatrix}\widetilde{v_1}\\ \widetilde{v_2}\\ \widetilde{i_\mathrm{L}}\end{bmatrix} + \begin{bmatrix} 0 & \dfrac{I_\mathrm{L}}{C_1}\\ 0 & -\dfrac{I_\mathrm{L}}{C_2}\\ \dfrac{V_\mathrm{g}}{L} & \dfrac{V_2-V_1}{L}\end{bmatrix}\begin{bmatrix}\widetilde{d_1}\\ \widetilde{d_2}\end{bmatrix}, \tag{5a}$$

$$\begin{bmatrix}\widetilde{v_\mathrm{CM}}\\ \widetilde{v_\mathrm{DM}}\\ \widetilde{i_\mathrm{L}}\end{bmatrix} = \begin{bmatrix} m_1 & m_2 & 0\\ m_1 & -m_2 & 0\\ 0 & 0 & 1\end{bmatrix}\begin{bmatrix}\widetilde{v_1}\\ \widetilde{v_2}\\ \widetilde{i_\mathrm{L}}\end{bmatrix}. \tag{5b}$$

According to Eq. (5), the corresponding AC small signal model of SIDO power stage can be obtained (without considering the variation of input voltage). It is shown in Fig. 4 that the averaged switching operation of S3 and S4 can be modeled as two transformers.

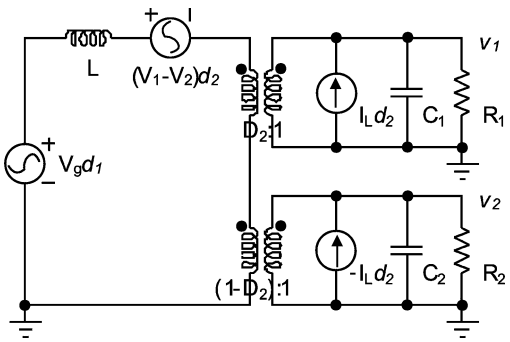

Fig. 4. AC small signal model of the SIDO power stage.

The SIDO converter in Fig. 3 is a multi-loop system which has several cross-regulated items. However, it is feasible to decompose the system into several single-loop subsystems to solve the stability problem[4]. Detailed analysis on the differential-mode and common-mode sub-systems will be derived.

3.2. Differential-mode sub-system

When the common-mode loop is closed, the inductor behaves as a current source because of the average current mode control. Therefore, the approximated transfer function from $\widetilde{d_2}$ to $\widetilde{v_\mathrm{DM}}$ can be expressed as:

$$F_\mathrm{DM}(s) = I_\mathrm{L}\left(\frac{m_1R_1}{1+sR_1C_1} + \frac{m_2R_2}{1+sR_2C_2}\right). \tag{6}$$

Equation (6) gives us the valuable information that the power stage of the differential mode works as a first-order system whose dominant pole "p_0" is related to the output capacitors and resistors. Based on this, the compensation of EA1 can be designed accordingly. Assuming the error amplifier is ideal with infinite gain, the transfer function of the proportional

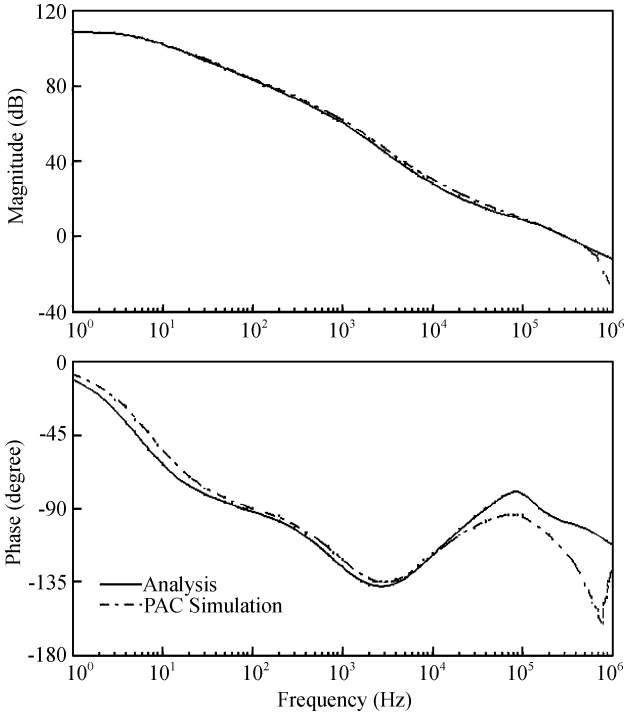

Fig. 5. Bode plots of the differential-mode sub-system.

integral compensator is

$$G_{\mathrm{EA1}}(s) = -\frac{1 + sR_{\mathrm{f2}}C_{\mathrm{f1}}}{sR_{\mathrm{f1}}C_{\mathrm{f1}}}, \tag{7}$$

which has a pole "$p_1 = 0$" and a zero "$z_1 = 1/R_{\mathrm{f2}}C_{\mathrm{f1}}$". Because of the limited area for on-chip capacitors and resistors, z_1 is higher than p_0. For two poles at low frequency and zero compensation, large loop gain is needed to make the crossover frequency f_{c} much higher than z_1:

$$z_1 \ll 2\pi f_{\mathrm{c}} \rightarrow R_{\mathrm{f2}} \approx 1\,\mathrm{M\Omega},\ \ C_{\mathrm{f1}} \approx 10\ \mathrm{pF}. \tag{8}$$

The change of load resistors has little influence on the stability of the differential-mode loop. On the other hand, the maximum loop gain at the switching frequency is limited by the ramp slope of the sawtooth waveform to avoid sub-harmonic oscillation problems[6].

$$|G_{\mathrm{EA1}}(s)|_{\omega=2\pi f_{\mathrm{s}}} < V_{\mathrm{saw}} f_{\mathrm{s}} \frac{C}{(m_1 + m_2)I_1}, \tag{9}$$

where f_{s} is the switching frequency and V_{saw} is the voltage of the sawtooth waveform. Equation (9) decides the value of $R_{\mathrm{f2}}/R_{\mathrm{f1}}$.

A bode plot of the periodic AC (PAC) simulation in Spectre is shown by the dashed line in Fig. 5 (when $V_{\mathrm{g}} = 4\,\mathrm{V}$, $R_1 = 3\ \Omega$, $R_2 = 9\ \Omega$), which demonstrates a phase margin of 85° and a crossover frequency of 145 kHz. From the bode plot, it is informed that the loop gain is important for stability and response.

3.3. Common-mode sub-system

When the differential-mode loop is closed, according to the state space equation (5) and small signal model in Fig. 4,

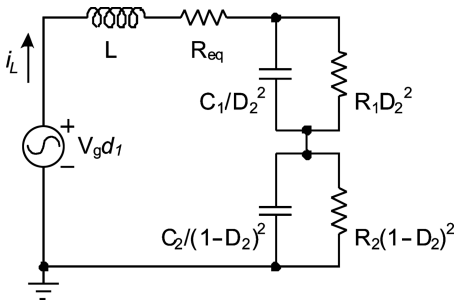

Fig. 6. AC decoupling model of the common-mode power stage.

the approximated transfer function from $\widetilde{d_1}$ to $\widetilde{i_{\mathrm{L}}}$ and $\widetilde{v_{\mathrm{CM}}}$ is given by:

$$F_{\mathrm{CMi}}(s) = \frac{V_{\mathrm{g}}}{sL + \dfrac{(D_2)^2 R_1}{1 + sR_1C_1} + \dfrac{(1 - D_2)^2 R_2}{1 + sR_2C_2} + R_{\mathrm{eq}}}, \tag{10}$$

$$F_{\mathrm{CMv}}(s) = \left[\frac{m_1(D_2)^2 R_1}{1 + sR_1C_1} + \frac{m_2(1 - D_2)^2 R_2}{1 + sR_2C_2}\right] F_{\mathrm{CMi}}(s), \tag{11}$$

with $R_{\mathrm{eq}} \approx \frac{V_2 - V_1}{I_{\mathrm{L}}}\left(D_2 - \frac{m_2}{m_1 + m_2}\right)$.

Equations (10) and (11) show that the power stage of the common-mode sub-system behaves as a normal buck converter with the resonance frequency $w = \sqrt{[D_2^2 + (1 - D_2)^2]/LC}$. The closed-loop effect of the differential mode acts as an extra series resistor R_{eq}. The equivalent model is illustrated in Fig. 6.

Based on this conclusion, the compensation of the common-mode sub-system can be designed. Average current mode control is adopted to achieve good dynamic performance. The design of current mode control has been studied extensively in the literature[6, 7]. There are also two control loops in the sub-system: the current loop and the voltage loop. The configurations of these two loops have been discussed in Ref. [8]. The inductor behaves as a current source in current mode control. Thus the compensation of the voltage loop is similar to that of the differential-mode loop ($C_{\mathrm{f2}} \approx 10$ pF), whose dominate pole in the power stage is related to the filter capacitors and load resistors.

Figure 7 gives the outer loop simulation of the common-mode sub-system with current loop closed, which shows a phase margin of 52° and a crossover frequency of 120 kHz (when $V_{\mathrm{g}} = 4\,\mathrm{V}$, $R_1 = 3\,\Omega$, $R_2 = 9\,\Omega$). Due to the current mode control, the system stability is insensitive to changes in load[8].

4. Circuit implementation

Average current mode control has the advantage of good stability and fast response, but it needs the information of the inductor current. Existing on-chip current detection techniques include using a series sensing resistor or mirror transistor[9]. However, they undergo problems of power loss, only half a side of inductor current, and inaccurate match on layout. Here a lossless, continuous, filter-based current detection method[10] is used. As shown in Fig. 8, the inductor current is sensed by filtering the voltage across the inductor.

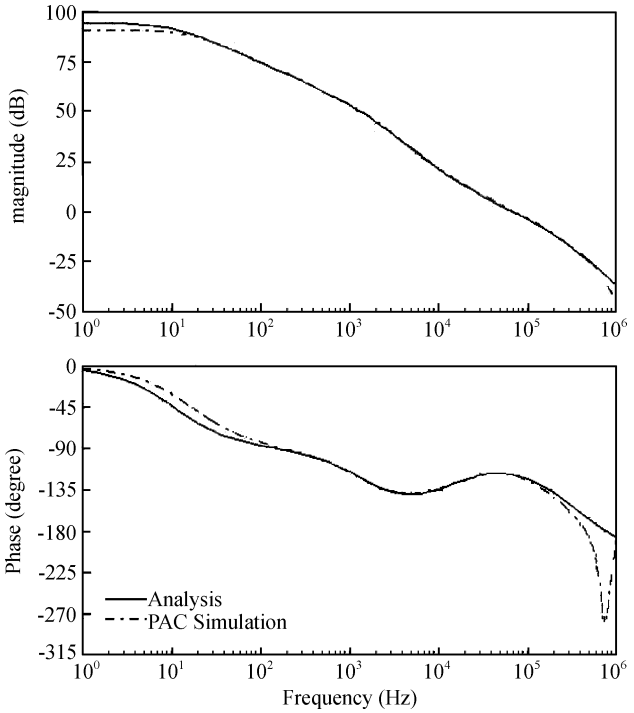

Fig. 7. Bode plots of the common-mode sub-system.

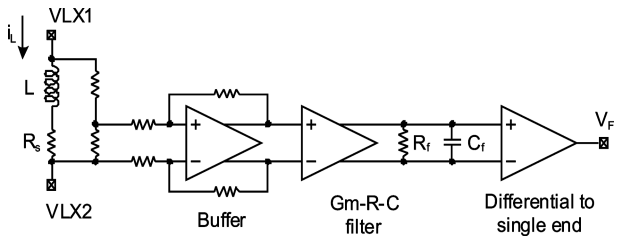

Fig. 8. Diagram of a filter-based inductor current detector.

So, the output of this current detector can be expressed as:

$$V_{\mathrm{F}}(s) = V_{\mathrm{L}}(s)H(s) = I_{\mathrm{L}}(s)(sL + R_{\mathrm{s}})\frac{g_{\mathrm{m}}R_{\mathrm{f}}}{1 + sR_{\mathrm{f}}C_{\mathrm{f}}}K. \qquad (12)$$

Actually it is not necessary to make the pole of the filter exactly equal to the zero of the inductor because the current loop only affects the system stability at high frequency[8]. Thus, Equation (12) can be written as:

$$V_{\mathrm{F}}(s)|_{\mathrm{f}\uparrow} = I_{\mathrm{L}}(s)\frac{g_{\mathrm{m}}L}{C_{\mathrm{f}}}K. \qquad (13)$$

Therefore, the filter is feasible for on-chip implementation (C_{f} = 5 pF). In the SIDO converter, both sides of the inductor have switches, which gives rise to a large common mode noise at the input of the filter. The differential g_{m} opamp in Fig. 9 is used to suppress this noise[11]. The transconductance g_{m} is adjusted by transistors M3 and M4, which work as linear resistors.

A four-input-terminal two-stage opamp is used for differential-to-single-end conversion. The schematic is given in Fig. 10, which has high input impedance, and it is easy to adjust the gain and common mode voltage.

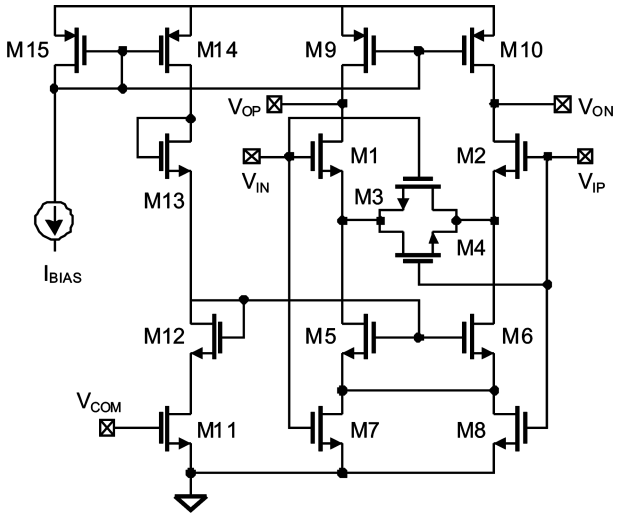

Fig. 9. Schematic of the full-differential g_{m} opamp.

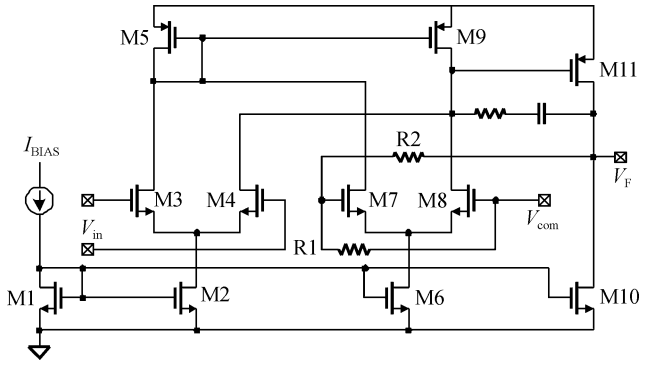

Fig. 10. Schematic of a differential-to-single-end conversion circuit.

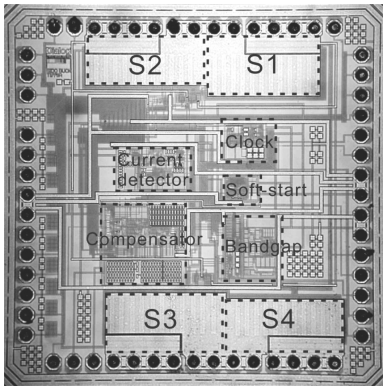

Fig. 11. Die micrograph of the SIDO chip.

5. Measurement results

The SIDO converter was fabricated on a 0.25 μm 2P4M CMOS process. The die micrograph is shown in Fig. 11. The chip area is 2.2 × 2.2 mm^2 with all pads.

Figure 12 depicts the soft start process with the input voltage 4 V and load currents I_1 = 400 mA, I_2 = 200 mA. The output voltages ramp up smoothly in about 250 μs. Both output voltages are stable with V_1 = 1.2 V and V_2 = 1.8 V.

Figure 13 shows the detailed waveform of the ripples of two outputs, which correlates well with that from the analysis. The ripples are about 40 mV at a frequency of 600 kHz. It can be clearly seen that large glitches occur at the transition between output switches S3 and S4. The discontinuous current

Table 1. Performance comparison of SIDO switching converters.

Parameter	Ma[1]	Ma[2]	Trevisan[3]	Bonizzoni[4]	This work
Process	0.5 μm 1P3M	0.5 μm 1P3M	FPGA	0.35 μm 1P3M	0.25 μm 2P4M
Inductor (μH)	1	1	5	22	4.7
Capacitors (μF)	33/40	33	10	35	22
Oscillator (MHz)	1	1	0.5	1	0.6
Efficiency (max)	88%	89%	N/A	93%	95%
Output voltage (V)	3.0/3.6	2.5/3.0	0.9–1.5	1.2–Vbat	1.2/1.8
Load current (max) (mA)	75/75	120/100	500/500	200 (total)	400/200
Output ripple (mV)	35/30	20/25	60/50	31/24	40/40
Control method	Voltage mode	Voltage mode	Digital PWM	Voltage mode	Current mode

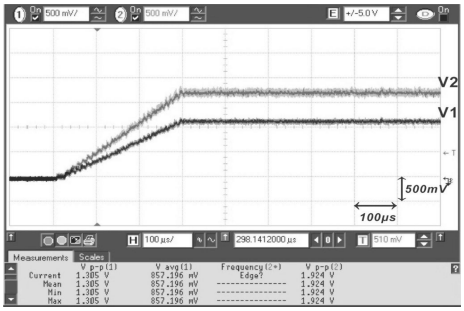

Fig. 12. Output voltages of the soft start test.

Fig. 13. Ripples of two output voltages.

Fig. 14. Load response: I_1 = 400 mA, I_2 = 200 mA $\longrightarrow$ 0.1 mA.

on the filter capacitor is the root cause of these glitches.

The converter efficiency at full load is 86%. The performance comparison of the SIDO switching converters is summarized in Table 1. Considering the output ripples are related to load currents, this SIDO converter shows the advantages of low ripple and fast response.

6. Conclusion

This paper presents an average current mode controlled SIDO buck converter. The system stability was investigated and the decoupling analysis of this multi-loop system was proposed. A lossless, continuous filter-based current detector was used. Measurements on a test chip demonstrated low ripple, fast response and high efficiency. The SIDO converter is suitable for cost-effective power management of portable electronics.

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