Improved dual-channel 4H-SiC MESFETs with high doped n-type surface layers and step-gate structure*

Deng Xiaochuan(邓小川)†, Zhang Bo(张波), Li Zhaoji(李肇基), and Zhang Yourun(张有润)

(State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu 610054, China)

Abstract: An improved dual-channel 4H-SiC MESFET with high doped n-type surface layer and step-gate structure is proposed, and the static and dynamic electrical performances are analyzed. A high doped n-type surface layer is applied to obtain a low source parasitic series resistance, while the step-gate structure is utilized to reduce the gate capacitance by the elimination of the depletion layer extension near the gate edge, thereby improving the RF characteristics and still maintaining a high breakdown voltage and a large drain current in comparison with the published SiC MESFETs with a dual-channel layer. Detailed numerical simulations demonstrate that the gate-to-drain capacitance, the gate-to-source capacitance, and the source parasitic series resistance of the proposed structure are about 4%, 7%, and 18% smaller than those of the dual-channel structure, which is responsible for 1.4 and 6 GHz improvements in the cut-off frequency and the maximum oscillation frequency.

Key words: high doped surface layer; step-gate; 4H-SiC MESFETs
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1. Introduction

Silicon carbide (SiC) based metal semiconductor field effect transistors (MESFETs) are considered to be excellent candidates for high power, high frequency, and high temperature applications in commercial and military communication due to their superior properties, such as high electron saturation velocity, high critical electric field, and high thermal conductivity[1,2]. Today, a large number of SiC MESFET structures have been reported for a wide range of applications. Among them, MESFETs with a buried-gate to suppress the trapping induced instabilities and to provide high drain current are the most widely analyzed and manufactured for power applications[3,4]. However, both experimental and simulation results show that the drain-source breakdown voltage of buried-gate transistors is lower than that of conventional channel recessed structures. Andersson *et al.* presented a SiC MESFET structure with the application of the buried-gate and field-plate techniques to increase the breakdown voltage and to reduce the high frequency dispersion in high power applications[5]. The gate field plate amplifies the charge interaction between the drain and gate terminals, thus increasing the gate-to-drain capacitance, decreasing the saturation current, and significantly degrading the gain characteristics[6]. Recently, SiC MESFETs with a dual-channel layer, that can alleviate the above mentioned drawbacks, have been proposed, which are found to have an improved performance compared to conventional single channel layer devices by using the lower doped upper-channel layer and the higher doped lower-channel layer to improve the breakdown voltage and the channel current[7]. However, the lower doped channel layer will lead to an increase of the parasitic series resistance in the gate-source region, which reduces the cut-off frequency and the maximum oscillation frequency.

In this paper, an improved dual-channel 4H-SiC MESFET with a high doped n-type surface layer and a step-gate structure is investigated using the 2D device simulation program ATLAS. The proposed structure improves RF characteristics, such as the cut-off frequency and the maximum oscillation frequency, but still maintains a high breakdown voltage and a high drain current. In this configuration, a high doped n-type surface layer is employed to obtain a low source parasitic series resistance. Also, the step-gate structure is adopted to decrease the gate-to-drain capacitance and the gate-to-source capacitance by the elimination of the depletion layer extension near the gate edge. The DC and RF performances of the proposed 4H-SiC MESFETs have been studied in detail, and the simulation results are compared with those obtained from the dual-channel layer structure.

2. Device structure and physical model

Cross-sectional views of the proposed and the dual-channel 4H-SiC MESFETs are shown in Fig. 1. To compare the characteristics of the proposed structure with the dual-channel structure, the basic parameters of the structure, except

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† Corresponding author. Email: xcdeng@uestc.edu.cn
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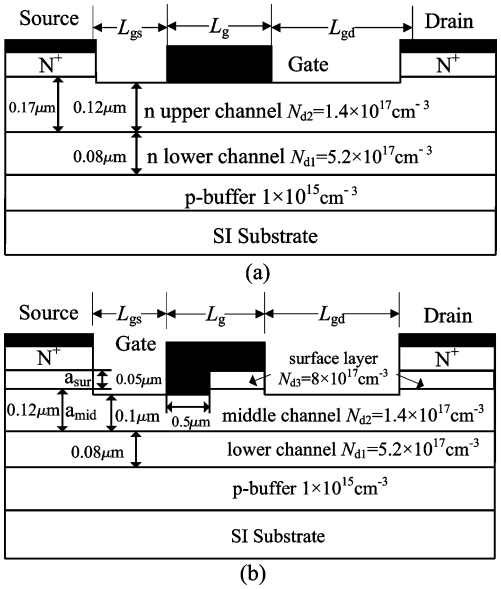

Fig. 1. Schematic cross-sections of (a) the dual-channel 4H-SiC MESFETs and (b) the proposed MESFETs.

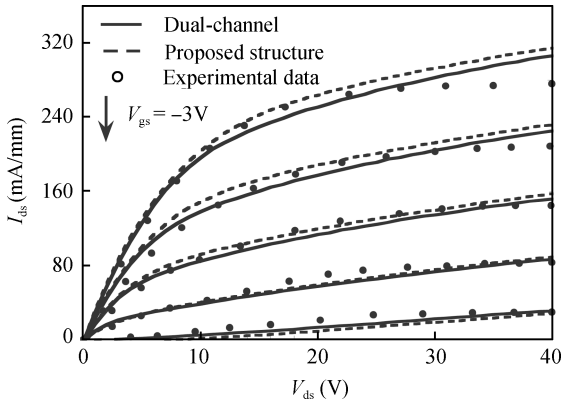

Fig. 2. Comparison of *I*–*V* characteristics for the SiC MESFETs.

for the n-type active layer and the gate configuration, are left unchanged and can be described as follows. A vanadium-doped semi-insulating wafer with a buffer/channel/cap epi stack is used. The buffer and cap layers are p-doped (1×10^{15} cm^{-3}) and n-doped (1×10^{19} cm^{-3}) with thicknesses of 0.5 and 0.2 μm, respectively. The gate length L_g is 1 μm, and both the gate-source and the gate-drain spacing, L_{gs} and L_{gd}, are 0.5 and 1.5 μm. The gate width is 50 μm, and a temperature of 300 K is employed by default in the simulations. The doping concentration and the thickness of the lower-channel layer for the dual-channel structure are 5.2×10^{17} cm^{-3} and 0.08 μm, and the doping concentration and the thickness of the upper-channel layer are 1.4×10^{17} cm^{-3} and 0.17 μm. To allow a meaningful comparison, the channel thickness and the doping concentration of the proposed MESFETs are determined to have the same pinch-off voltage as that of the dual-channel MESFETs. The proposed structure consists of an n-doped layer (N_{d1} = 5.2×10^{17} cm^{-3}, N_{d2} = 1.4×10^{17} cm^{-3}, and N_{d3} = 8×10^{17} cm^{-3}) with thicknesses of 0.08, 0.12 (a_{mid}), and 0.05 μm (a_{sur}), respectively. The recessed/step-gate region can be realized by inductively coupled plasma etching.

The 2D numerical device characteristics are realized with Atlas from Silvaco. The details of the model and the simulation method are presented elsewhere[8]. In addition to basic Poisson and the drift/diffusion equations, the different physical models used simultaneously in Silvaco are SRH (Shockley-Read-Hall) and Auger for generation and recombination, Analytic and Fldmob for mobility, Incomplete for incomplete ionization of dopants, and, finally, Impact Selb for impact ionization. These mobility models will take into account carrier velocity saturation, carrier-carrier scattering (with high doping), carrier diffusion at interface, and vertical electric field influence. The low-field mobility dependence on the temperature and doping concentration has been described by the 4H-SiC specific model proposed by Roschke *et al.*[9, 10], and the Caughey–Thomas high-field mobility model is obtained from full-band Monte Carlo simulations of bulk 4H-SiC[11].

3. Simulation results and discussion

3.1. DC characteristics

Figure 2 shows the simulated and experimental drain current–voltage (I_{ds}–V_{ds}) characteristics under the gate bias (V_{gs}) varied from 0 to −12 V in steps of −3 V. It should be noted that the simulated results of the dual-channel MESFETs are in good agreement with the experimental data except for a few small discrepancies at a large drain bias, when the gate bias is set to zero[7]. The discrepancy is mainly due to neglecting the thermal effects in our simulations[12]. As seen from the figure, I_{ds} of the proposed structure is almost the same as that of the dual-channel structure at various V_{gs}. It can also be seen that I_{ds} of the proposed structure is slightly larger than that of the dual-channel structure when the gate bias is over –9 V; however, I_{ds} of the proposed structure shows the opposite behavior when the gate bias is below –9 V. This is related to the step-gate of the improved structure, which has lower and upper gates, i.e., a thinner (0.18 μm) and a thicker (0.25 μm) part of the channel. The thicker channel allows for a higher drain saturation current and lower source and drain impedances, whereas the thinner channel ensures that the channel can be effectively controlled by the gate bias. The drain current is dominated by the upper gate, i.e., the thicker channel, under high gate bias, which leads to the fact that I_{ds} of the proposed structure is slightly larger than that of the dual-channel structure. As V_{gs} is reduced, the influence of the upper gate increases, which results in the opposite behavior.

The simulated breakdown voltage characteristic of the improved SiC MESFETs structure with a breakdown voltage of 142 V is illustrated in Fig. 3 and compared to the results of the dual-channel SiC MESFETs from simulations, which is consistent with the experimental results for the dual-channel structure. It is found that the breakdown characteristic of the proposed structure is almost the same as that of the dual-channel structure. This is due to the fact that both the proposed

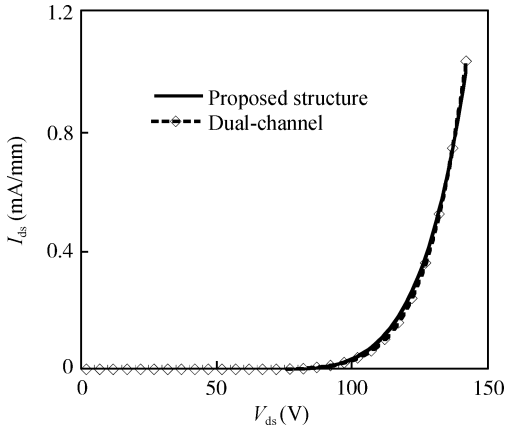

Fig. 3. Simulated three-terminal breakdown characteristics.

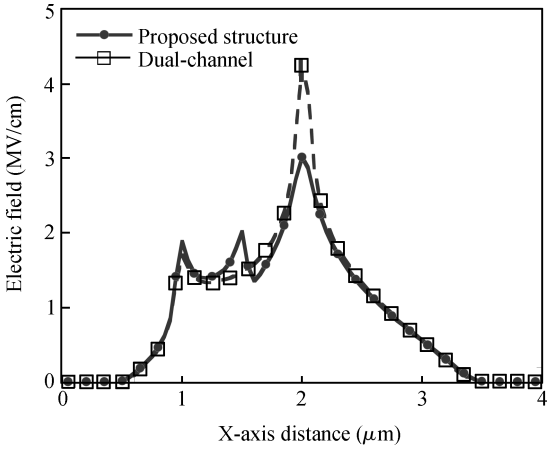

Fig. 4. Simulated electric field distribution under the gate (100 from the bottom) at the breakdown.

device and the dual-channel device utilize the lower doped channel layer to sustain a high breakdown voltage.

In Fig. 4, a comparison of the electric field distribution in the channel region under the gate for the dual-channel MESFETs and the proposed MESFETs at the breakdown is shown, which is used to understand the cause of the behavior described in Fig. 3. The simulation results show that the dual-channel structure has two electric field peaks, which occur near the drain and source side gate edge. The high, sharp electric field peak at the gate edge toward the drain side results in the breakdown of the device. For the proposed structure, it should be noted that the electric field has three important peaks, i.e., one at the source side gate edge, another at the drain side gate edge, and the third at the bottom edge of step-gate toward the drain side. The high electric field peak at the bottom edge of the gate towards the drain side is suppressed by the extension of the gate metal on the surface, which acts like a field plate resulting in a gradual field distribution. As indicated by the electric field distribution given in the figure, it is obvious that both the proposed device and the dual-channel device utilize the lower doped channel layer to sustain a high breakdown voltage. Therefore, the breakdown characteristic of the proposed SiC MESFETs is found to be very similar to that of the dual-channel MESFETs.

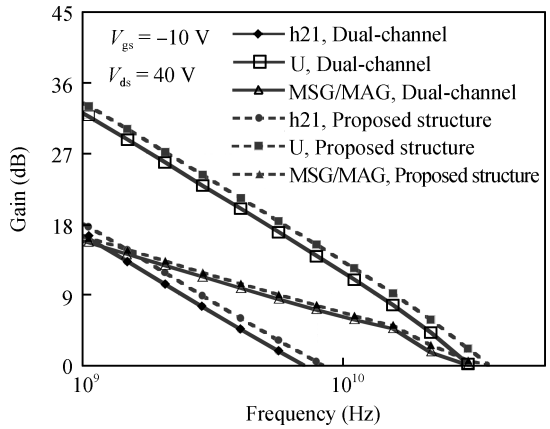

Fig. 5. Simulated small-signal high frequency characteristics of a 4H-SiC.

3.2. Small signal characteristics

Small-signal characteristics for a 4H-SiC MESFET with a high doped n-type surface layer, an step-gate structure, and the dual-channel structure are estimated by a S-parameter simulation from 800 MHz to 80 GHz. Values of the parasitic elements for the equivalent circuit are extracted using the Dambrine method[13]. Figure 5 shows the frequency dependence of the small signal current gain h_{21}, the maximum stable gain (MSG), the maximum available gain (MAG), and the unilateral power gain (U) simulated under bias conditions of $V_{gs} = -10$ V and $V_{ds} = 40$ V. The results show that the cut-off frequency f_T (defined as the frequency at which the current gain is equal to 1) and the maximum oscillation frequency f_{max} (defined as the frequency at which the unilateral power gain is unity) of the proposed structure are 8.5 and 37 GHz, respectively. On the other hand, for the dual-channel structure, f_T and f_{max} are 7.1 and 31 GHz, respectively. The increase in f_T and f_{max} is attributed to the reduction in the feedback capacitance and the parasitic series resistance compared to the dual-channel layer MESFETs.

Figure 6(a) demonstrates the frequency dependence of the gate-to-drain capacitance (C_{gd}) and the gate-to-source capacitance (C_{gs}) extracted from S-parameters. The bias conditions of $V_{gs} = -10$ V and $V_{ds} = 40$ V are considered in our simulations. Figure 6(b) shows a comparison of the source parasitic series resistance (R_s) between the proposed and the dual-channel MESFETs with the application of the pinched cold-FET techniques[14]. For the proposed structure, the feedback gate capacitance and the parasitic series resistance are decreased compared to that of the dual-channel structure, which is responsible for an approximately 20% improvement in f_T and 19% improvement in f_{max}. The reduction in C_{gd} and C_{gs} is due to the fact that the recess regions between the gate-source and gate-drain electrodes reduce the depletion layer extension at the edge of the gate effectively, whereas the decrease in R_s is attributed to the relatively high doping concentration of the surface layer. It is known that, in the intrinsic FET, the cut-off frequency and the maximum oscillation frequency are given as

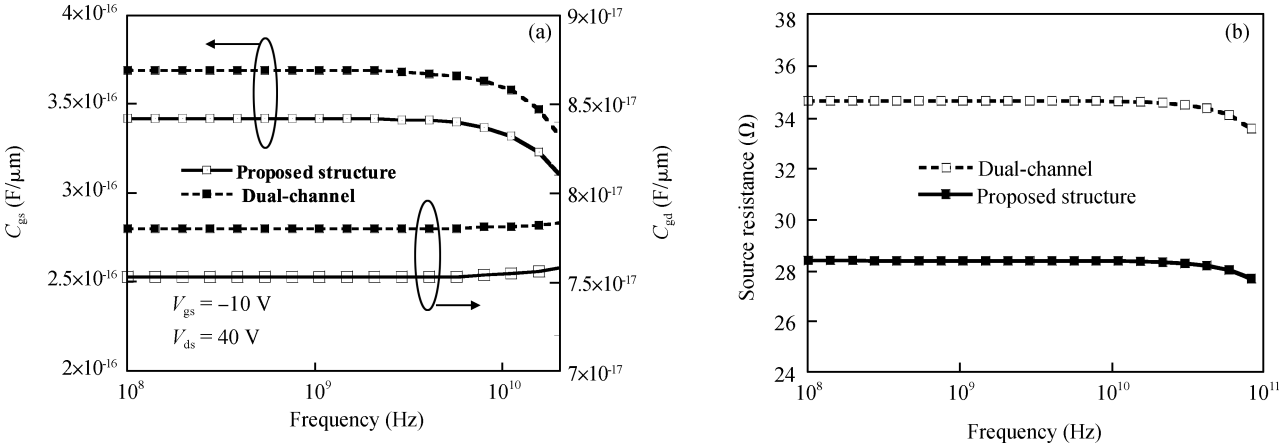

Fig. 6. Change of the extracted small-signal equivalent circuit parameters as a function of the frequency: (a) Input capacitance; (b) Source parasitic series resistance.

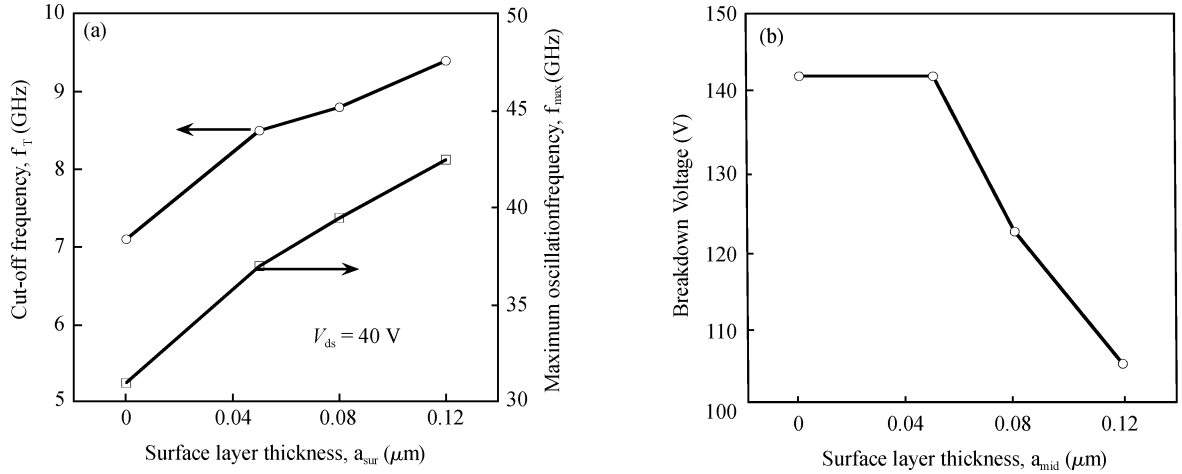

Fig. 7. (a) f_T and f_{max} and (b) simulated off-state breakdown voltage as a function of surface layer thickness.

follows[15].

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)}, \tag{1}$$

$$f_{max} \approx \frac{f_T}{2\sqrt{r_1 + f_T\tau_3}}, \tag{2}$$

where

$$r_1 = \frac{R_g + R_i + R_s}{R_{ds}}, \qquad \tau_3 \equiv 2\pi R_g C_{gd}, \tag{3}$$

where g_m is the transconductance, R_g is the gate resistance, and R_i and R_{ds} are the input and output resistances under the gate. As inferred from Eq. (1), the decrease of C_{gs} and C_{gd} has important effects on the cut-off frequency of the SiC MESFETs, which leads to an increase of f_T. The behavior of f_{max}, as shown in Fig. 5, can be interpreted using Eqs. (2) and (3). In fact, the proposed structure will decrease the total input capacitance and the parasitic series resistance compared to the dual-channel structure. Therefore, the values of f_T and f_{max} increase from 7.1 to 8.5 GHz and 31 to 37 GHz, respectively.

3.3. Surface layer thickness influence

Figures 7(a) and 7(b) shows the surface layer thickness dependence of the cut-off frequency, the maximum oscillation frequency, and the breakdown voltage. In this analysis, a_{sur} is varied while keeping $a_{sur} + a_{mid} = 0.17$ μm. As can be seen from the figure, with the increase of the surface layer thickness from 0 to 0.12 μm, the values of f_T and f_{max} increase from 7.1 and 31 to 9.4 and 42.5 GHz, respectively, whereas the value of the breakdown voltage decreases from 142 to 105 V. The improvement of f_T and f_{max} is due to the decrease of the gate-to-source capacitance and the increase of the transconductance. On the other hand, the decrease of the breakdown voltages is due to the fact that the increase of the surface layer thickness under the step gate reduces the effects of the extension of the gate metal on the surface.

4. Conclusion

In this work, the electrical performances of a newly developed dual-channel 4H-SiC MESFET with a high doped n-type surface layer and a step-gate structure are studied in detail by physical simulations. The improvement of the RF performances is achieved for the proposed structure, which yet has a similar saturation drain current and similar breakdown characteristics. The cut-off frequency and the maximum oscillation frequency of the proposed MESFETs are 8.5 and 37 GHz, respectively, compared with 7.1 and 31 GHz for the

dual-channel MESFETs. This change is attributed to the elimination of the depletion layer extension near the gate edge and the low source parasitic series resistance. As compared to the dual-channel MESFETs, the proposed MESFETs show an approximately 4% and 7% decrease in the gate-to-drain capacitance and the gate-to-source capacitance at $V_{gs} = -10$ V and $V_{ds} = 40$ V, while the source parasitic series resistance reduces from 34.6 to 28.3 Ω. Therefore, the improved dual-channel 4H-SiC MESFET with a high doped n-type surface layer and a step-gate structure has a superior DC and RF performance compared to the similar device based on the dual-channel structure.

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