W-plug via electromigration in CMOS process*

Zhao Wenbin(赵文彬)[1,2,†], Chen Haifeng(陈海峰)[2], Xiao Zhiqiang(肖志强)[2], Li Leilei(李蕾蕾)[1], and Yu Zongguang(于宗光)[1,2]

(1 School of Microelectronics, Xidian University, Xi'an 710071, China)

(2 No.58 Institute, China Electronic Technology Group Corporation, Wuxi 214035, China)

Abstract: We analyze the failure mechanism of W-plug via electromigration made in a 0.5-μm CMOS SPTM process. Failure occurs at the top or bottom of a W-plug via. We design a series of via chains, whose size ranges from 0.35 to 0.55 μm. The structure for the via electromigration test is a long via chain, and the layer in the via is Ti/TiN/W/TiN. Using a self-heated resistor to raise the temperature of the via chain allows the structure to be stressed at lower current densities, which does not cause significant joule heating in the plugs. This reduces the interaction between the plug and the plug contact resistance and the time-to-failure for the via chain. The lifetime of a W-plug via electromigration is on the order of 3×10^7 s, i.e., far below the lifetime of metal electromigration. The study on W-plug via electromigraion in this paper is beneficial for wafer level reliability monitoring of the ultra-deep submicron CMOS multilayer metal interconnect process.

Key words: W-plug; self-heated; electromigration; lifetime
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1. Introduction

With the development of the semiconductor manufacturing industry, multilayer interconnect structures have been developed and widely used[1−5]. One such structure is illustrated in Fig. 1. A W-plug is used in both contacts and vias, resulting in good planarity. At the bottom of the contact, $TiSi_2$ is used to form a good electrical contact to the Si. In contacts and vias, TiN surrounds the tungsten, thus increasing the adhesion to the oxide. It also acts as a barrier for WF_6 originating from the underlying material during tungsten deposition. The global interconnect structure in this paper is Ti/TiN/Al(Si-Cu)/TiN. Cu in the Al suppresses electromigration and hillock formation. Ti improves the grain texture of the Al for better electromigration protection and promotes adhesion. TiN is used as a barrier between the Al and the Ti in order to limit $TiAl_3$ formation. The Ti/TiN and TiN layers on the bottom and the top of each interconnect provide an electrical shunt in case of void formation in the Al. TiN on the top also acts as an antireflective layer for lithography[1,5]. Many variations of this structure are used by different manufacturers. These variations especially involve in the exact makeup and the order of materials in the interconnect stack. But the basic idea of using multilayer planar structures is very common[2,3].

Metallization structures are also receiving increased attention because of failure and reliability issues. Failure has a variety of causes: stress-induced void formation in interconnect lines; hillock growth; unwanted chemical reactions and interdiffusion between layers; dopant diffusion and segregation; excessive roughening of films; corrosion; electromigration; and others[4]. In this paper, using accelerated lifetime tests, we study the W-plug contacts/vias electromigration characteristic and monitor the early electromigration failures of the contacts/vias.

2. Failure mechanism of W-plug via electromigration

Very high test temperatures can be used for via chain tests because there is no electromigration in tungsten at temperatures less than approximately 1800 °C (i.e., the recrystallization temperature of tungsten). A W-plug via fails under an electromigration stress due to the accumulation of vacancies flowing in the Al lines at the interface between the plug and the Al line. These vacancies can form a very thin line of voids along this interface and cause an open in the via. Currently, most processes prevent this problem by forming refractory metal layers above and below the Al metal lines. This produces a W-to-Ti/TiN interface, rather than a W-to-Al interface. Since the Ti or Ti/TiN layer contacts the Al along its entire surface, the formation of a string of thin voids between the Ti or Ti/TiN and the Al lines will not produce an open via[1,5].

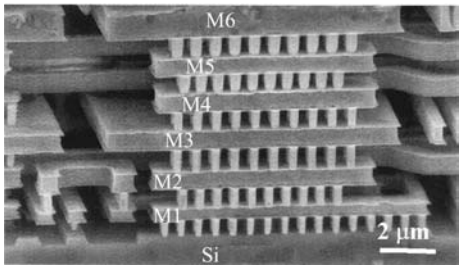

Fig. 1. SEM picture of a 6-layer metal stack.

* Project supported by the Series Program for Electronic Component and Device Spectrum.
† Corresponding author. Email: justinzhaowb@sina.com
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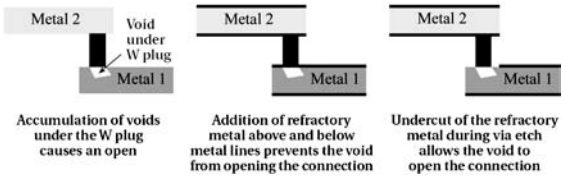

Fig. 2. W-plug via electromigration failure modes.

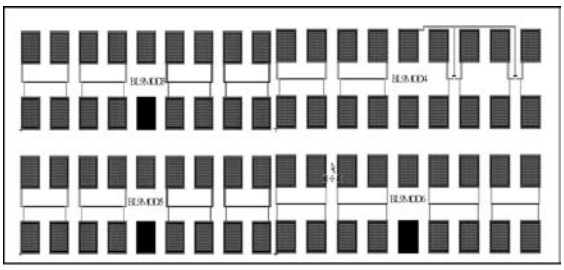

Fig. 3. Layout of the contacts/vias of the electromigration test structure.

Unfortunately, most etchants used to open the interior layer dielectric (ILD) layers to form a via hole have poor selectivity between oxide and the Ti or Ti/TiN layers on top of the lower metal line. This produces a tendency to remove the refractory metal layer off the top of the Al metal lines at the via openings. A reliable via can still be constructed, as long as the etch rate of the Ti or Ti/TiN layer is slower than that of the ILD. Under this case, a narrow ring of the refractory material should be exposed around the edge of the via opening. This will allow for a contact between the W-plug and the refractory metal on the surface of the Al metal line and provides a reliable contact. However, if the etch rate of the Ti or Ti/N metal layer on top of the Al metal lines is faster than the lateral etch rate of the ILD, then the refractory metal layer on top of the Al lines will be undercut around the edges of the via opening. This will prevent the formation of a contact between the W-plug and the refractory metal layer on top of the lower metal layer and lead to early electromigration failures of the vias (Fig. 2).

This is the most common via electromigration failure mechanism for W-plug vias. Therefore, it should be clear that electromigration tests performed at temperatures sufficient to cause significant rates of bulk electromigration in the Al lines will still allow the detection of a lack of W-to-refractory metal layers at any via. The number of vacancies required to cause an open in the via will be significantly less when the barrier metal over the metal 1 does not contact the W-plug. The sensitivity of the via chain to an over-etched refractory metal can be detected as easily with bulk migration in the Al as with grain boundary migration in Al. The use of higher temperatures will simply reduce the measurement time.

3. Test structure design

We designed series of via 1 (Metal 1 to Metal 2), via 2 (Metal 2 to Metal 3) chains, whose size ranges from 0.35 to 0.55 μm, step 0.1 μm. Such a layout structure is illustrated in Fig. 3. For example, for Block 9 Model 5 (BL9MOD5), we design contact electromigration chains: chains with 50 contacts,

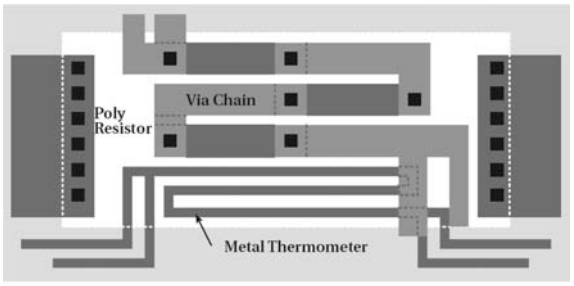

Fig. 4. W-plug via test structure using a self-heated poly resistor.

(A) Structure 1: Metal 3 to Metal 2; ovl Metal 3 / Via 2 = DR (Design Rule);

(B) Structure 2: Metal 3 to Metal 2; ovl Metal 3 / Via 2 = DR – 0.1 μm;

(C) Structure 3: Metal 3 to Metal 1; ovl Metal 3 / Via 2 = DR; ovl Metal 2/ V ia = DR;

(D) Structure 4: Metal 3 to Metal 1; ovl Metal 3 / Via 2 = DR – 0.1 μm; ovl Metal 2 / Via = DR – 0.1 μm.

The test structure for the via electromigration test is a long via chain (Fig. 4), and the layer in the via is Ti(20 nm)/TiN(60 nm)/W(600 nm)/TiN(80 nm)/Al(800 nm)/TiN. There are three important aspects of the structure:

(1) The self-heated resistor (poly resistor). The use of tungsten (W) plug vias introduces one more variable in the design of suitable test structures. The resistivity of the W-plug can be up to seven times higher than that of an Al-plug[5]. Therefore, for the same current density, the power dissipated in the W-plug will be up to seven times higher. This would cause significant joule heating at much lower current densities and introduce an increased thermal gradient in the line. Thus, it is often impossible to achieve a reasonable stress using an isothermal or SWEAT test. Variations in plug resistivity will influence the test results much more than these variations will influence the rate of electromigration under lower current stresses. This interaction effect requires that the via test structure includes a self-heated resistor. A self-heated resistor is most commonly formed by a poly resistor placed under the via chain. The poly resistor is designed to ensure that current can be forced through the resistor. Power dissipated in this resistor will heat the via chain placed on top of it[6].

(2) Metal thermometer. A metal 1 "thermometer" will measure the temperature of the metal over the heater. Feedback from this thermometer will be used to adjust the power forced into the heater resistor to achieve any specified temperature. There must be some form of feedback to provide an accurate measure of the temperature achieved by the heater. Generally, a serpentine metal line is used for the "thermometer". The thermal coefficient of resistance (TCR) of any metal is process independent. Therefore, a measurement of the change in the resistance of the metal thermometer will provide an accurate measure for the temperature of the metal line. This can provide the feedback to allow the adjustment of the current forced through the self-heated resistor to achieve any desired stress temperature.

(3) Via chain. The length of the chain should be compat-

Table 1. Time to failure for W-plug via electromigration.

No	T (K)	T_f (s)	No	T (K)	T_f (s)	No	T (K)	T_f (s)
1	420	126	1	400	386	1	380	1220
2	420	164	2	400	760	2	380	1900
3	420	148	3	400	500	3	380	1606
4	420	188	4	400	600	4	380	1960
5	420	486	5	400	506	5	380	7406
6	420	260	6	400	564	6	380	1168
7	420	304	7	400	544	7	380	1480
8	420	244	8	400	548	8	380	804
9	420	248	9	400	482	9	380	5940
10	420	286	10	400	526	10	380	1802

ible with the available space and the power supply available for the test. The cross-sectional area of the metal 1 segment, the metal 2 segment, and the vias should be about equal, because the time-to-failure for the metal line is the time required to diffuse vacancies, initially distributed throughout the metal line, into a void large enough to open the line or via. Except in extreme cases, there are not enough vacancies in the via itself to open the via. Therefore, it is necessary to collect vacancies from the connecting metal lines to form the void required to open the via. That means, the collection rate for the void is limited by the lowest current density in the chain. If wide metal lines are used to connect the vias, the lifetime of the vias would be extremely long[3].

4. Test and analysis

The reliability of interconnects is measured by electrical tests. Common causes for the failure of interconnect lines are void and hillock formation, either due to stresses on the lines or due to electromigration. Stress-induced voids can be detected simply by measuring the electrical resistance of the line. An open in the circuit would indicate a line-spanning void. When shunt layers, such as TiN, are used, a void, which spans the entire Al layer, would not cause an open in the circuit since current could still flow through the shunt line. In this case, a failure would lead to a certain increase in the line resistance on the order of 20%. Stress-induced hillocks, which crack overlaying dielectric layers and contact adjacent interconnect layers, can be detected by short circuits. Failure due to electromigration-current-induced voids and hillock formation is measured using accelerated lifetime tests[3].

It would take too long to monitor the failure of interconnects due to electromigration under normal circuit operating conditions. Therefore, tests are done at elevated temperatures and higher-than-normal current levels, so-called accelerated lifetime tests. In these tests, the temperature acceleration is given by[3]

$$A_T = \exp[(E_a/0.00008625)(1/T_{use} - 1/T_{test})], \quad (1)$$

where A_T is the temperature acceleration, T_{use} is the normal operating temperature (K), and T_{test} is the test temperature (K).

The current acceleration is given by[3]

$$A_J = (J_{test}/J_{use})^n, \quad (2)$$

where A_J is the temperature acceleration, J_{use} is the normal operating current (A/cm^2), J_{test} is the test current (A/cm^2), and n is typically close to 2.

Increased current densities (about 1×10^6 to 2×10^6 A/cm^2) are forced through an interconnect line at elevated temperatures (380–420 °C). The voltage is monitored by taps to this line, and the resistance is measured. An open circuit, or even a partially open circuit, indicating void formation due to electromigration, is, thus, detected by an increase in the resistance. A second line adjacent to the line under test is monitored as well. A short circuit to this line indicates hillock formation and extrusion. Again, a certain percentage change in resistance (on the order of 20%) defines a line failure. The time to failure for a number of lines is determined and statistically analyzed. This is done by plotting the cumulative percentage of lines that have failed versus time in a logarithmic plot. The median time to failure (MTTF) has been found to follow the general relationship[3]:

$$\mathrm{MTTF} = AJ^{-n}\exp\frac{E_A}{kT}, \quad (3)$$

where J is the current density, n is typically close to 2 while values ranging from 1 to 3 have been reported, and A is a constant, which depends on the film structure (grain size, etc.) and the processing. E_A is the activation energy for electromigration and is often associated with Al grain boundary diffusion. Its value ranges from 0.5 to 0.8 eV. k is the Boltzmann constant, and T is the temperature. Once the exact values for this expression have been determined experimentally at elevated temperatures and currents for the particular structure and process, one can extrapolate down to the normal operating conditions to determine how long the interconnects are functional before a failure occurs. This, of course, assumes that the failure occurs by the same mechanisms at lower temperatures and current densities, which may not always be the case.

We did our tests on the via structure shown in Fig. 3. Table 1 is the time to failure of a W-plug via at three different temperatures. The via size is 0.5 μm. It is necessary to use up

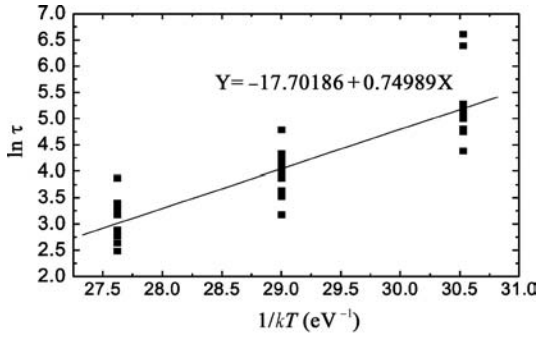

Fig. 5. Plot of $\ln\tau$–T for W-plug via electromigration.

Table 2. Lifetime of W-plug via electromigration at 420 K.

No	T_f (s)	A_T	A_J	Total acceleration	Lifetime (s)
1	126	3730	33	123090	1.6×10^7
2	164	3730	33	123090	2.0×10^7
3	148	3730	33	123090	1.8×10^7
4	188	3730	33	123090	2.3×10^7
5	486	3730	33	123090	6.0×10^7
6	260	3730	33	123090	3.2×10^7
7	304	3730	33	123090	3.7×10^7
8	244	3730	33	123090	3.0×10^7
9	248	3730	33	123090	3.1×10^7
10	286	3730	33	123090	3.5×10^7

to 1×10^6 A/cm^2 in this structure in order to produce a short in the circuit.

Figure 5 gives the relationship between the logarithm of the time-to-failure and $1/kT$. From this plot, we can estimate E_A to be about 0.75 eV by using Eq. (3).

Then we can calculate the temperature acceleration, the current acceleration and the total acceleration at 420 K, and, thus, obtain the lifetime of a W-plug via. Table 2 is the lifetime of the W-plug via of each sample.

The lifetime of the W-plug via electromigration is on the order of 3×10^7 s, but the lifetime of metal electromigration is on the order of 1×10^9 s. The via structure incorporates metal lines of a significant length being subject to a high current density and a high temperature stress. Thus, the via test time cannot be longer than the test duration of the metal lines. The metal line lifetime always poses an upper limit to the duration of the test structure. Therefore, this structure is only of useful if the vias limit the lifetime of the structure. In addition, the cross-sectional area of the metal 1 segment, the metal 2 segment, and the vias should be about equal. If wide metal lines are used to connect the vias, the lifetime of the vias would be extremely long.

The fast wafer level reliability (WLR) tests provide a significant advantage for enabling the test of large samples from a semiconductor FAB. In this case, large samples do not simply mean large numbers of semiconductor devices. These tests are designed to fit into the scribe lanes of a production semiconductor wafer. Structures arranged like this allow for rapid testing of the variation in reliability across a wafer, the variation between wafers in a lot, and the variation between different wafer lots. Each of these sources of variation can be quantified and inspected on a daily basis using WLR test techniques.

5. Conclusion

According to the electromigration standard of JEDEC, we design a series of a long via chain W-plug via test structure. The layer in the via is Ti/TiN/W/TiN. The via test structure is designed to have a constant current density and temperature distribution throughout the structure. Therefore, failures at locations other than the vias are not unexpected for this structure for the standard "stepped Al vias." However, failure at the top or bottom of a W-plug via is expected, because there is no electromigration in the tungsten via itself. Hence, vacancies will accumulate at the interface between the Al and the refractory metal in the current path. In this paper, we report the test of W-plug via eletromigration. The extrapolated lifetime is on the order of 3×10^7 s. If wide metal lines are used to connect the vias, the lifetime of the vias is longer. If we apply a low temperature or a lower current density stress, the measure time for via electromigration would be extremely long. The study on W-plug via electromigration reported in this paper is beneficial for the wafer level reliability monitoring of the ultra-deep submicron CMOS multilayer metal interconnect process.

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