A universal programmable driving circuit for spatial light modulators*

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Abstract: A universal programmable multi-quantum-well (MQW) spatial light modulator (SLM) driving circuit is developed. With a twice scanning, it can generate programmable signals to drive a non-linear MQW SLM by using a software preprocessing unit. By adjusting the switching network of the driving circuit, this circuit can reduce the switching noise and improve the output precision. The chip test results show that the driving voltage can swing from 0 to V_{DD}, and its resolution could be close to 256 with a pixel area of only 65×65 μm^2.

Key words: spatial light modulator; programmable; driving circuit
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1. Introduction

Spatial light modulators (SLMs) are the pivotal component of many optical information systems. Semiconductor SLMs based on the quantum-confined Stark effect (QCSE) can reach a much higher modulation speed than SLMs using other techniques, such as liquid crystals and micro-mirrors. Therefore, it is very attractive for applications when speed is a critical parameter. Apart from this, the multi-quantum-well (MQW) SLM has distinct advantages over any other SLMs, including a high contrast ratio, multi-level modulation, and low power.

However, the driving circuit usually limits the speed of a MQW SLM. Up to now, a 256-level resolution driving circuit using 0.25-μm CMOS technique is only developed by Lenslet Company[1]. The features of a SLM include a faster switching speed, which is as fast as ps, a low light-power and switch-power consumption, long time stability at room temperature, and a good integration compatibility with other optoelectronic devices and electronic circuits. There are four major bottlenecks of a MQW SLM driving circuit: nonlinearity between the driving voltage and the MQW SLM reflectivity, the response speed gap between the SLM (ps) and the CMOS circuit (ns), the full-swing voltage output, which are basic properties for a MQW SLM driving circuit, and the limits of the SLM pixel are because of its flip-chip bonding with MQW SLMs[2].

In order to resolve the problems mentioned above, a new driving circuit has been developed in this paper. Photoelectric controlling signals are generated by using a software preprocessing unit for different reflectance spectra and modulation grayscales. A new method, which does a rough-scan followed by a fine-scan is developed to reduce the pixel size effectively and takes the place of the method of one-step-scan. The new switched-capacitor integral[3–5] circuit is designed to eliminate the various noises caused by MOS switch and to improve the output precision.

2. Principle and structure of the driving circuit

The block diagram of the driving circuit is shown in Fig. 1. The software preprocessing unit is the unit on the outside of the chip, which is used to do preprocessing for a variety of reflectance spectra of the MQW SLM. The chip is composed of an array of driving circuit pixels and external control circuits.

The MQW SLM array is flip-chip bounded to the driving circuit array, and each modulator pixel has its own driving circuit pixel. The external control circuit controls the work state of the pixel unit. The working principles are described in the following text.

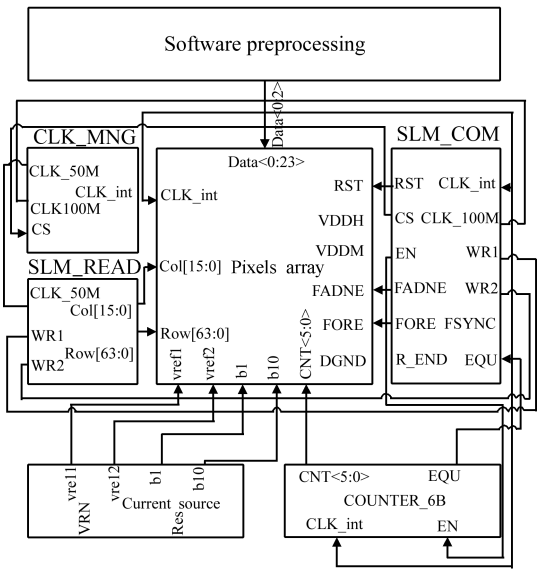

Fig. 1. Block diagram of the driving circuit with a 64×64-pixel array.

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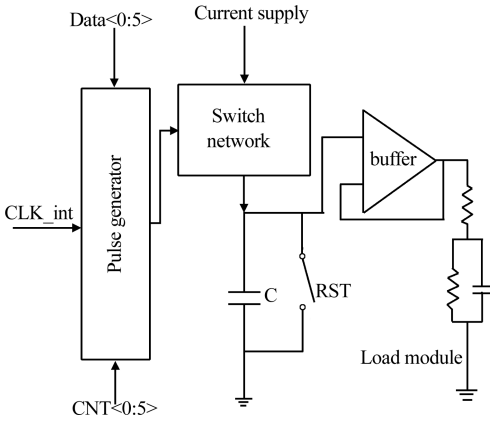

Fig. 2. Driving circuit pixel.

2.1. Array of driving circuit pixels

The array is composed of 64 × 64 pixels; each modulator unit has its own driving circuit, whose structure is shown in Fig. 2. A pulse generator generates a switch-control signal, which is a pulse-width-modulation (PWM) signal to control the integral circuit. The switch network is a new method for controlling the precision of the output current. The process compares data <0:5> sent from the software preprocessing unit with CNT <0:5> sent from the counter. When the counter starts working, the switch turns on, the current source begins charging the integral-capacitor and the integral process begins to work. When the CNT <0:5> equals data <0:5>, the switch turns off, the current source stops charging the integral-capacitor, and the integral process is stopped, too. The value of data <0:5> determines the integral-time and integral-voltage while the buffer maintains the pixel value to be displayed.

The structure adopting a switched-capacitor integral circuit satisfies the requirements of low-power. The new switching network eliminates the switch noise caused by switching transistors of the traditional switch and improves the integral-precision. The new method of a rough-scan followed by a fine-scan, not only realizes the high scanning speed and high resolution, but also reduces the pixel size effectively.

2.2. Software preprocessing unit

The software preprocessing unit is initialized before the driving circuit works for the first time. First, the characteristic parameter of the MQW SLM non-linear reflectance spectrum is tested. Second, the MQW SLM non-linear reflectance spectrum is fitted. Then, according to the MQW SLM grayscale resolution, the driving voltage provided by the driving circuit is calculated. Finally, the driving voltage value is translated into binary digital codes, which are stored in a RAM in accordance with the integral circuit parameters. It could work on different modulators and realize different modulation grayscales that make the driving circuit become more equal. Its design process is shown in Fig. 3.

2.3. External control circuit

The external control circuit includes five modules:

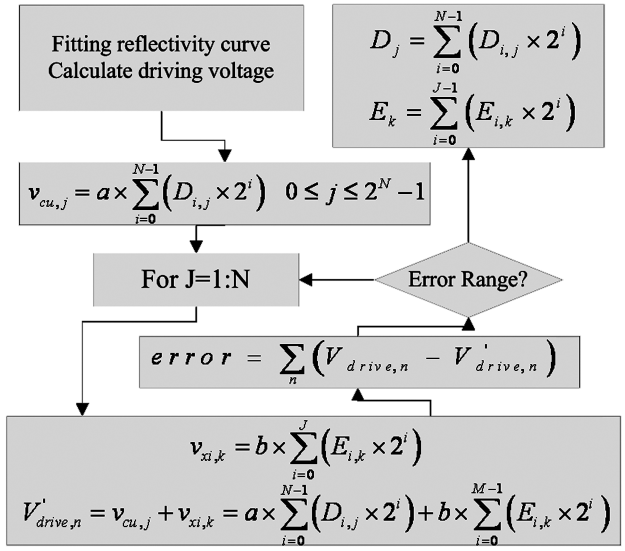

Fig. 3. Flow chart of the software preprocessing unit.

CLK_MNG, SLM_READ, SLM_ COM, the current source, and COUNTER_6B.

(1) CLK_MNG generates clock signals used for the two-step-scan integral. There are three inputs: CLK_50 MHz, CLK_100 MHz, and CS, where CS is the strobe signal of the clock. For CS = 1, the first integral starts, and CLK_int = 6.25 MHz. For CS = 0, the second integral starts, and CLK_int = 100 MHz.

(2) SLM_READ generates a row/column address signal. In the beginning of each frame, reference data is assigned to the row/column address strobe unit. The reference data, provided by the software preprocessing unit, is 6-bit wide for each pixel through a 24-bit wide data bus.

(3) SLM_COM generates control-signals and state-signals used by the pixel unit and the external control circuit.

(4) The current source is a band-gap current reference. It provides a constant current to all pixels, which use a current mirror to obtain the reference current.

(5) COUNTER_6B is a 6-finger-counter. The signal EN sent from the SLM_COM unit determines when the COUNTER_6B begins to work. CLK_int determines the frequency of a work clock. In a frame, 0 to full is counted twice. During the counting, the real-time counter data is sent to all the pixels; a state-signal is send to SLM_COM when the counting ends.

3. Chip test and analysis

The photo of a chip with 64 × 64 pixels is shown in Fig. 4. The area of each pixel is 65 × 65 μm^2, which could meet the flip-chip requirements of the MQW SLM.

The work principle of the driving circuit is:

$$U = \frac{I\times \mathrm{CLK}_1}{C} + \frac{I\times \mathrm{CLK}_2}{C}, \tag{1}$$

where CLK_1 is the rough-scan clock, CLK_2 is the fine-scan clock, the integrating current I = 500 nA, and the integrating

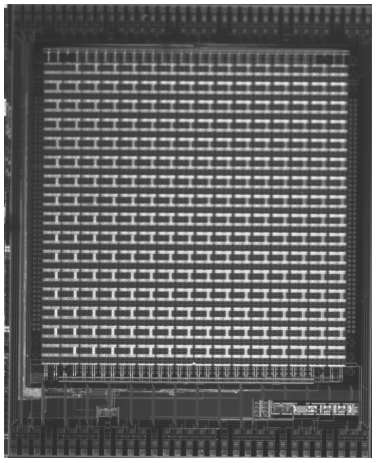

Fig. 4. Chip picture.

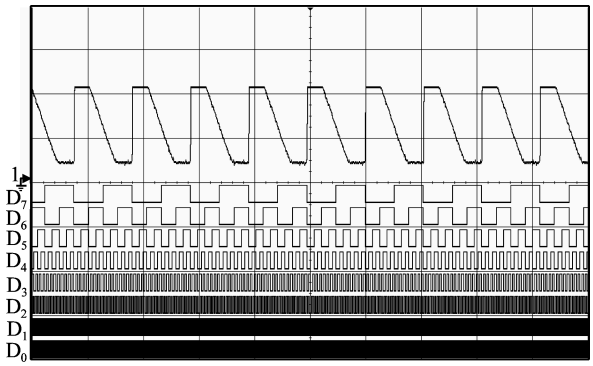

Fig. 5. The driving voltage decreases linearly when the data increases.

capacitance is C = 500 fF. During the one-step-scan, CLK_2 = 0.

3.1. One-step-scan mode

The method of one-step-scan and discharge integral is tested. The frequency of CLK_1 is 10 MHz. The input data is 6-bit wide. The driving voltage of the driving circuit is:

$$U = V_{DD} - V_{in} = V_{DD} - \frac{It}{C}. \quad (2)$$

According to Eq. (2), the supply source V_{DD}, the integrating current I, and the integrating capacitance C are all constant; so the driving voltage U is a linear function of the charging or the discharging time t, where t is the width of the pulse signal generated by the input data. As a result, the U is a linear function of the input data. When the input data is tiny, the driving voltage stays at V_{DD}. While the input data is increasing, V_{in} is also increasing, and the driving voltage decreases to 0 V. So the driving voltage swings from 0 to V_{DD}. On the condition of V_{DD} = 3.3 V, the value of the integrating voltage is 100 mV, and the resolution of the driving voltage is 32. When the data increases by 1, the driving voltage decreases from 100 mV to 0. The faster the clock is, the smaller the driving voltage integrated in one clock is, and the higher the driving voltage resolution will be.

In Fig. 5, the top curve is the output voltage, and the lower curves are input data bits. As analyzed above, the driving voltage is reducing linearly while the input data is increasing linearly when the range of the output voltage is 0–3.3 V.

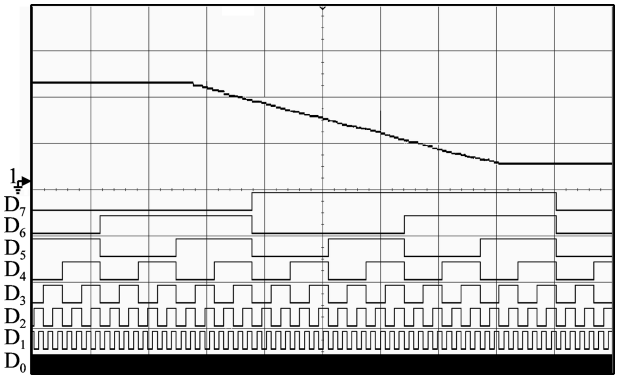

Fig. 6. Grayscale change of the driving voltage when the data increases.

Table 1. Driving voltage comparison between theoretical values and experimental results.

Theoretical value (V)	0.1	0.5	0.9	1.3	1.7
Experimental result (V)	0.104	0.502	0.901	1.301	1.700
Theoretical value (V)	2.1	2.3	2.7	3	3.3
Experimental result (V)	2.009	2.302	2.696	3.005	3.300

The curves in Fig. 6 are one period results of Fig. 5. During the period, the input data increases from 0 to a maximum, the driving voltage has a 32-level grayscale. There are some experiment results of the chip in Table 1. Comparing the theoretical values with experiment results, we can see that the absolute errors are below 5 mV, which is within the error tolerance.

3.2. Two-step-scan mode

After analyzing the one-step-scan method, it is found that the one-step-scan method could meet the basic request; but it is not good enough because of its low-resolution.

In order to resolve the problem mentioned above, a new method, the two-step-scan, in which a rough-scan is followed by a fine-scan, is put forward, and the test results indicate that the two-step-scan driving circuit can not only preserve the high scanning speed but also hugely reduces the pixel size, thus achieving a higher resolution. The simulation results of the power consumption of each pixel are shown in Fig. 7. The above part of the graph is the integral-voltage, and the lower part of the graph is the corresponding power consumption during the charging process. The difference of the power consumption is several tenths of mW and the maximum is only 78 mW. Obviously, it is tiny.

Figure 8(a) shows the curve of the driving voltages, which are calculated according to the reflectivity of MQW SLM. The resolution of the driving voltage is 256.

Figure 8(b) demonstrates the curve of the driving voltages, which are generated by the chip according to the data bits converted from the software preprocessing unit, 16-pixels and 16 rows output one by one in each row, while the 256 driving voltages output altogether. The curve of the driving voltages in Fig. 8(b) corresponds to Fig. 8(a), which means

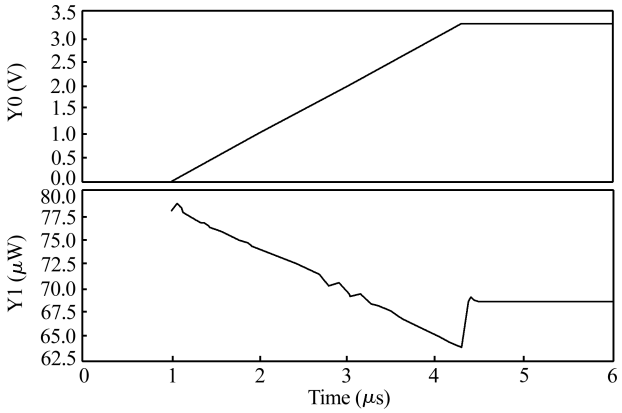

Fig. 7. Simulation of the power consumption of each pixel.

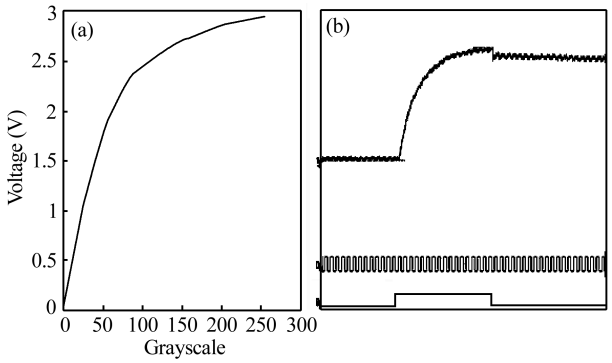

Fig. 8. Test results using the software preprocessing unit.

that the driving circuit and software preprocessing unit work normally. And the resolution of the voltage could reach up to 256.

4. Conclusion

The programmable MQW SLM driving circuit offers programmable non-linear photoelectric-conversion-controlling signals. It adopts a new method of a rough-scan followed by a fine-scan, which not only ensures the high scanning speed and voltage resolution, but also effectively reduces the size of the pixel driving circuit. By adjusting the switching network of the driving circuit, the switching noise is reduced and the output precision is improved. The experiment results show that the chip offers the swing of the driving voltage from 0 up to V_{DD}, and the resolution of the driving voltage from 0 to 256. Besides, a pixel size is only 65×65 μm^2, which can be integrated with MQW SLM by flip-chip bonding.

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